Product Specification

PE42821

UltraCMOS® SPDT RF Switch
100–2700 MHz

Features

- High power handling
  - 45 dBm @ 850 MHz, 32W
  - 44 dBm @ 2 GHz, 25W
- High linearity
  - 82 dBm IIP3 @ 850 MHz
  - 76 dBm IIP3 @ 2.7 GHz
- Low insertion loss
  - 0.35 dB @ 850 MHz
  - 0.60 dB @ 2 GHz
- Fast switching time of 4 µs (bypass mode)
- Wide supply range of 2.3–5.5V
- +1.8V control logic compatible
- ESD performance
  - 1.5 kV HBM on all pins
- External negative supply option

Product Description

The PE42821 is a HaRP™ technology-enhanced high power reflective SPDT RF switch designed for use in mobile radio, relay replacement and other high performance wireless applications.

This switch is a pin-compatible faster switching version of the PE42820. It maintains high linearity and power handling from 100 MHz through 2.7 GHz. PE42821 also features low insertion loss and is offered in a 32-lead 5 × 5 mm QFN package. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE42821 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

Peregrine's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 2. Package Type
32-lead 5 × 5 mm QFN

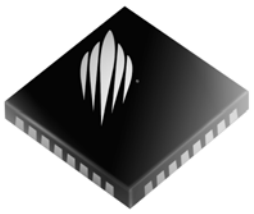


Figure 1. Functional Diagram

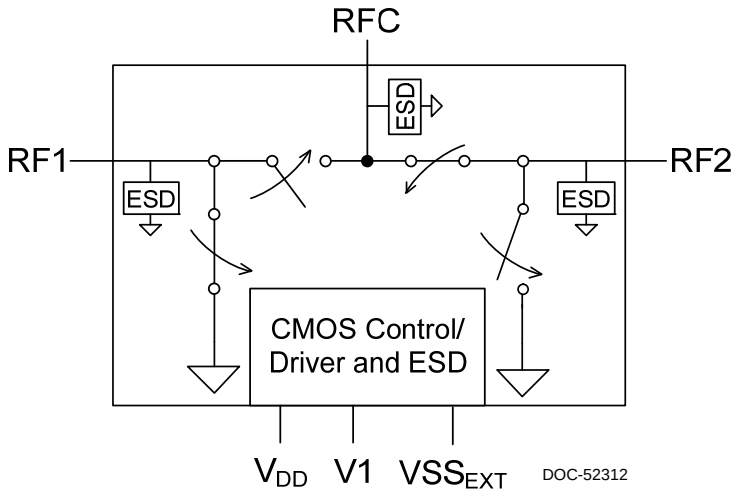


Table 1. Electrical Specifications @ +25 °C (Z_S = Z_L = 50Ω), unless otherwise noted
Normal mode[1]: V_{DD} = 3.3V, V_{SS_EXT} = 0V or Bypass mode[2]: V_{DD} = 3.3V, V_{SS_EXT} = –3.3V

Parameter	Path	Condition	Min	Typ	Max	Unit
Insertion loss[3]	RFC–RFX	100 MHz–1 GHz		0.40	0.55	dB
		1–2 GHz		0.60	0.80	dB
		2–2.7 GHz		0.80	1.05	dB
Isolation	RFX–RFX	100 MHz–1 GHz	33	35		dB
		1–2 GHz	26	28		dB
		2–2.7 GHz	22	24		dB
Unbiased isolation	RFC–RFX	V_{DD}, V1 = 0V, +27 dBm		6		dB
Return loss[3]	RFX	100 MHz–1 GHz		20		dB
		1–2 GHz		13		dB
		2–2.7 GHz		14		dB
Harmonics	RFC–RFX	2fo: +45 dBm pulsed @ 1GHz, 50Ω		–82	–78	dBc
		3fo: +45 dBm pulsed @ 1GHz, 50Ω		–85	–81	dBc
Input IP3	RFC–RFX	850 MHz		82		dBm
		2700 MHz		76		dBm
Input 0.1 dB compression point[4]	RFC–RFX	100 MHz–2 GHz		45.5		dBm
		2–2.7 GHz		44.5		dBm
Switching time in normal mode[1]		50% CTRL to 90% or 10% RF		7	11	µs
Switching time in bypass mode[2]		50% CTRL to 90% or 10% RF		4		µs
Settling time		50% CTRL to harmonics within specifications[5]		15	25	µs

Notes: 1. Normal mode: single external positive supply used.
2. Bypass mode: both external positive supply and external negative supply used.
3. Performance specified with external matching. Refer to *Evaluation Kit* section for additional information.
4. The input 0.1dB compression point is a linearity figure of merit. Refer to *Table 3* for the operating RF input power (50Ω).
5. See harmonics specs above.

Figure 3. Pin Configuration (Top View)

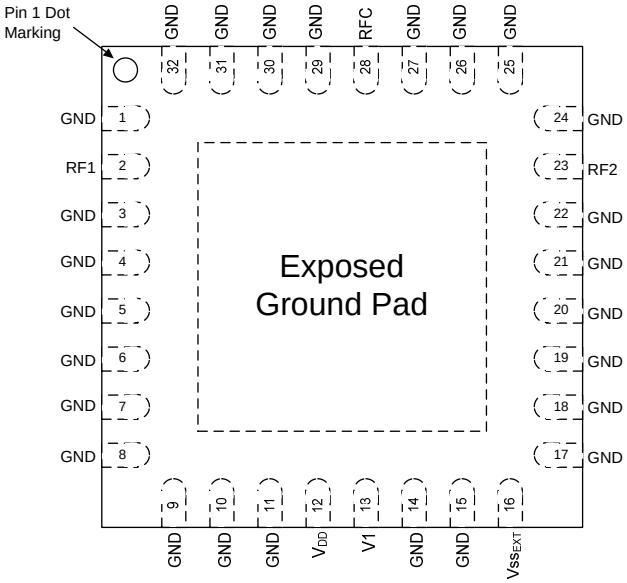


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1, 3–11, 14, 15, 17–22, 24–27, 29–32	GND	Ground
2	RF1[1]	RF port
12	V_{DD}	Supply voltage (nominal 3.3V)
13	V1	Digital control logic input 1
16	V_{SS_EXT}[2]	External V_{SS} negative voltage control
23	RF2[1]	RF port
28	RFC[1]	RF common
Pad	GND	Exposed pad: ground for proper operation

Notes: 1. RF pins 2, 23 and 28 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Use V_{SS_EXT} (pin 16, $V_{SS\_EXT} = -V_{DD}$) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 16, V_{SS_EXT} = GND) to enable internal negative voltage generator.

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Normal mode[1]					
Supply voltage	V_{DD}	2.3		5.5	V
Supply current	I_{DD}		130	200	µA
Bypass mode[2]					
Supply voltage	V_{DD}		3.3	5.5	V
Supply current	I_{DD}		50	80	µA
Negative supply voltage	V_{SS_EXT}	–3.6		–3.2	V
Negative supply current	I_{SS}	–40	–16		µA
Normal or Bypass mode					
Digital input high (V1)	V_{IH}	1.17		3.6[3]	V
Digital input low (V1)	V_{IL}	–0.3		0.6	V
RF input power, CW 100 MHz–2 GHz >2–2.7 GHz	$P_{MAX,CW}$			 43 42	 dBm dBm
RF input power, pulsed[4] 100 MHz–2 GHz >2–2.7 GHz	$P_{MAX,PULSED}$			 45 44	 dBm dBm
RF input power, unbiased	$P_{MAX,UNB}$			27	dBm
Operating temperature range (Case)	T_{OP}	–40		+85	°C
Operating junction temperature	T_J			+140	°C

Notes: 1. Normal mode: connect pin 16 to GND to enable internal negative voltage generator.
2. Bypass mode: apply a negative voltage to V_{SS_EXT} (pin 16) to bypass and disable internal negative voltage generator.
3. Maximum V_{IH} voltage is limited to V_{DD} and cannot exceed 3.6V.
4. Pulsed, 10% duty cycle of 4620 µs period, 50Ω.

Table 4. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	–0.3	5.5	V
Digital input voltage (V1)	V_{CTRL}	–0.3	3.6	V
Maximum input power 100 MHz–2 GHz >2–2.7 GHz	$P_{MAX,ABS}$		 45.5 44.5	 dBm dBm
Storage temperature range	T_{ST}	–65	+150	°C
Maximum case temperature	T_{CASE}		+85	°C
Peak maximum junction temperature (10 seconds max)	T_J		+200	°C
ESD voltage HBM[1], all pins	$V_{ESD,HBM}$		1500	V
ESD voltage MM[2], all pins	$V_{ESD,MM}$		200	V
ESD voltage CDM[3], all pins	$V_{ESD,CDM}$		250	V

Notes: 1. Human Body Model (MIL-STD 883 Method 3015)
2. Machine Model (JEDEC JESD22-A115)
3. Charged Device Model (JEDEC JESD22-C101)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the 32-lead 5x5 mm QFN package is MSL3.

Table 5. Control Logic Truth Table

Path	CTRL
RFC–RF1	H
RFC–RF2	L

Optional External V_{SS} Control (V_{SS_EXT})

For applications that require a faster switching rate or spur-free performance, this part can be operated in bypass mode. Bypass mode requires an external negative voltage in addition to an external V_{DD} supply voltage.

As specified in *Table 3*, the external negative voltage (V_{SS_EXT}) when applied to pin 16 will disable and bypass the internal negative voltage generator.

Switching Frequency

The PE42821 has a maximum 25 kHz switching rate in normal mode (pin 16 = GND). A faster switching rate is available in bypass mode (pin 16 = V_{SS_EXT}). The rate at which the PE42821 can be switched is then limited to the switching time as specified in *Table 1*.

Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Spurious Performance

The typical low-frequency spurious performance of the PE42821 in normal mode is –137 dBm (pin 16 = GND). If spur-free performance is desired, the internal negative voltage generator can be disabled by applying a negative voltage to V_{SS_EXT} (pin 16).

Hot Switching Capability

The typical hot switching capability of the PE42821 is +30 dBm. Hot switching occurs when RF power is applied while switching between RF ports.

Typical Performance Data @ +25 °C, V_{DD} = 3.3V, V_{SS_EXT} = 0V, unless otherwise noted

Figure 4. Insertion Loss vs. Temp (RFC–RFX)

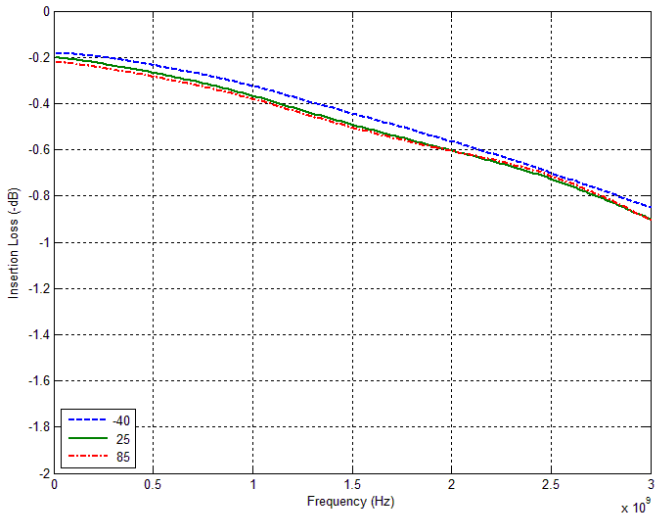


Figure 5. Insertion Loss vs. V_{DD} (RFC–RFX)

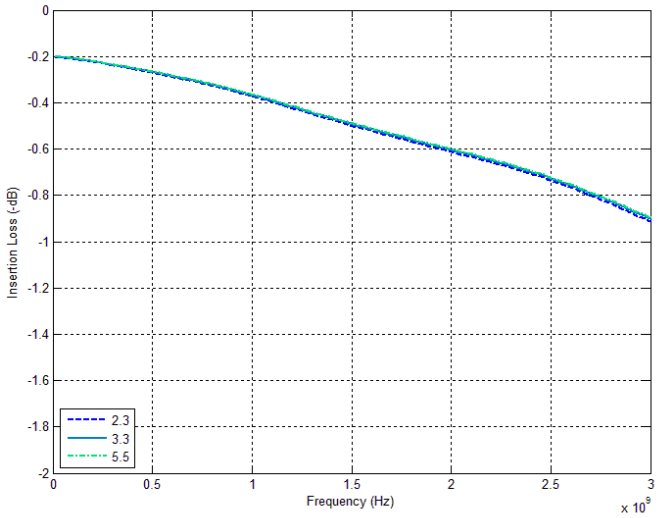


Figure 6. RFC Port Return Loss vs. Temp (RF1 Active)

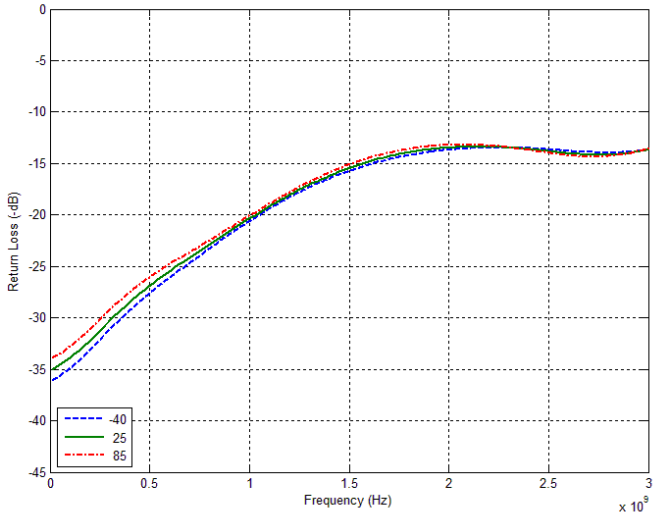
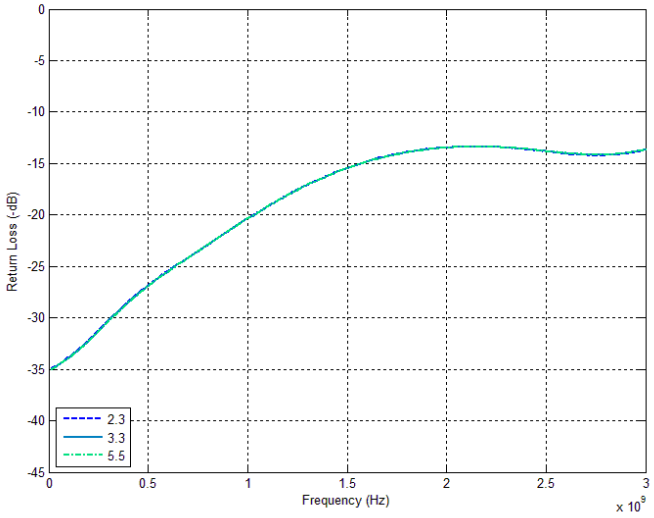


Figure 7. RFC Port Return Loss vs. V_{DD} (RF1 Active)



Typical Performance Data @ +25 °C, V_{DD} = 3.3V, V_{SS_EXT} = 0V, unless otherwise noted

Figure 8. Active Port Return Loss vs. Temp (RF1 Active)

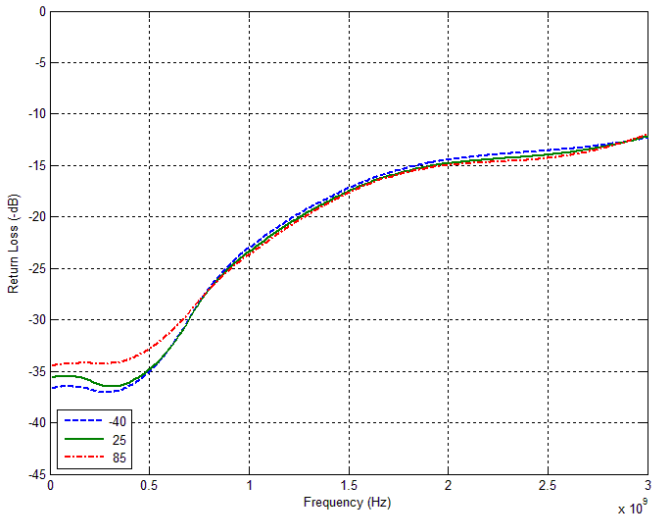


Figure 9. Active Port Return Loss vs. V_{DD} (RF1 Active)

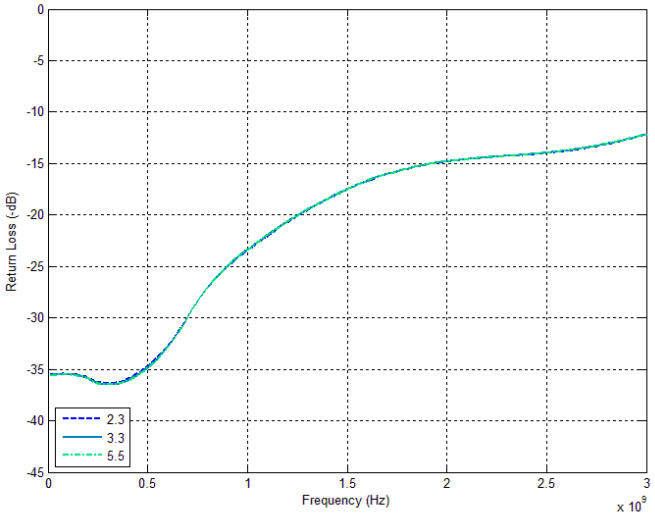


Figure 10. Isolation vs. Temp (RFC–RFX, RFX Active)

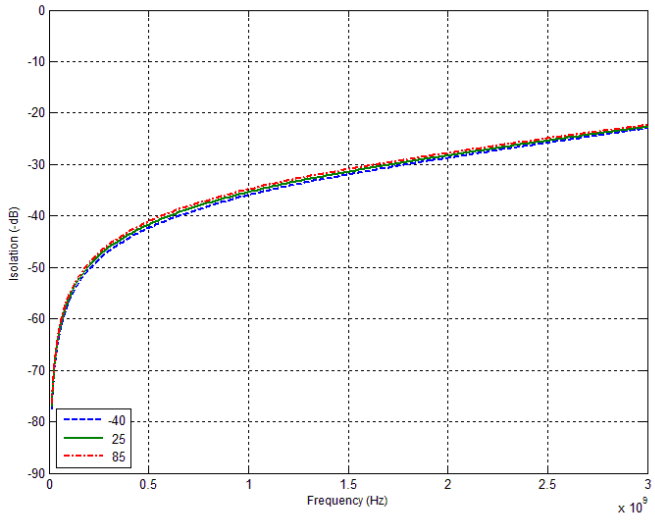
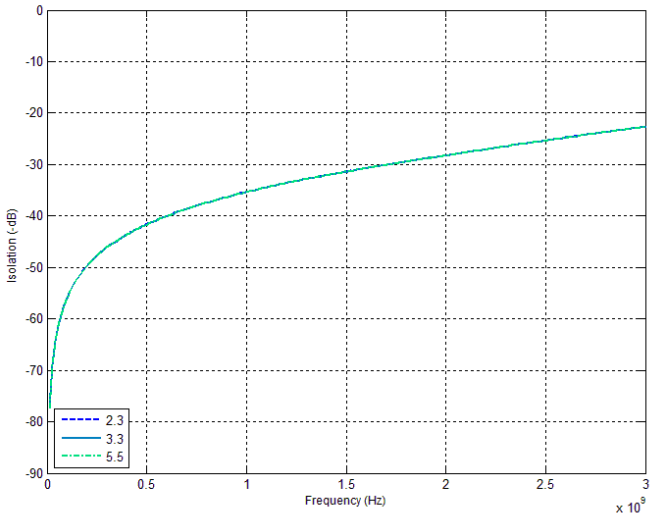


Figure 11. Isolation vs. V_{DD} (RFC–RFX, RFX Active)



Typical Performance Data @ +25 °C, V_{DD} = 3.3V, V_{SS_EXT} = 0V, unless otherwise noted

Figure 12. Isolation vs. Temp (RFX–RFX, RFX Active)

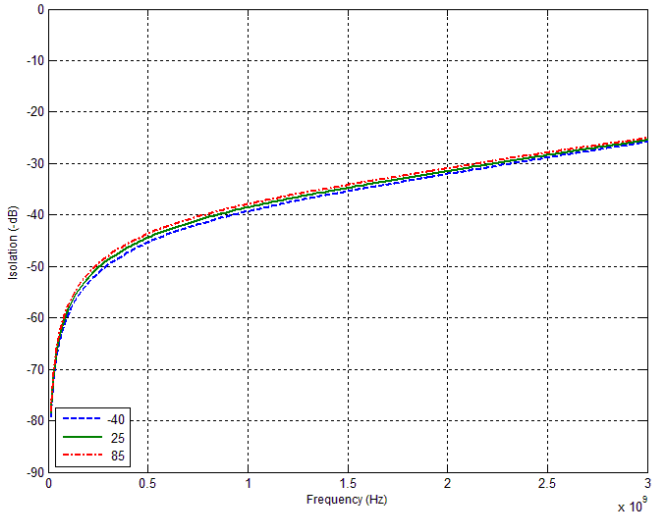
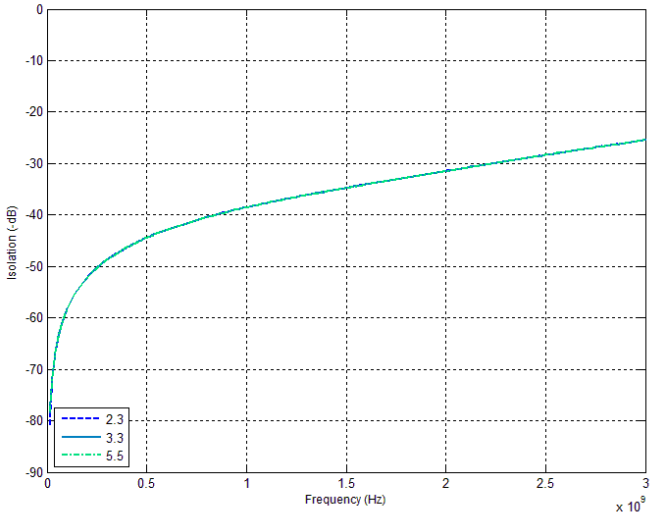


Figure 13. Isolation vs. V_{DD} (RFX–RFX, RFX Active)



Thermal Data

Though the insertion loss for this part is very low, when handling high power RF signals, the junction temperature rises significantly.

VSWR conditions that present short circuit loads to the part can cause significantly more power dissipation than with proper matching.

Special consideration needs to be made in the design of the PCB to properly dissipate the heat away from the part and maintain the 85°C maximum case temperature. It is recommended to use best design practices for high power QFN packages: multi-layer PCBs with thermal vias in a thermal pad soldered to the slug of the package. Special care also needs to be made to alleviate solder voiding under the part.

Table 6. Theta JC

Parameter	Min	Typ	Max	Unit
Theta JC (+85 °C)		20		°C/W

Evaluation Kit

The PE42821 Evaluation Kit board was designed to ease customer evaluation of the PE42821 RF switch.

The evaluation board in *Figure 14* was designed to test the part. DC power is supplied through J10, with VDD on pin 9, and GND on the entire lower row of even numbered pins. To evaluate a switch path, add or remove jumpers on V1 (pin 3) using *Table 5*.

The ANT port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1 and RF2 paths are also connected through 50Ω transmission lines via SMA connectors as J2 and J3. A 50Ω through transmission line is available via SMA connectors J5 and J6. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. An open-ended 50Ω transmission line is also provided at J4 for calibration if needed.

Narrow trace widths are used near each part to improve impedance matching. The shunt C1 on RFC port is to provide for high frequency impedance matching.

Figure 14. Evaluation Board Layout

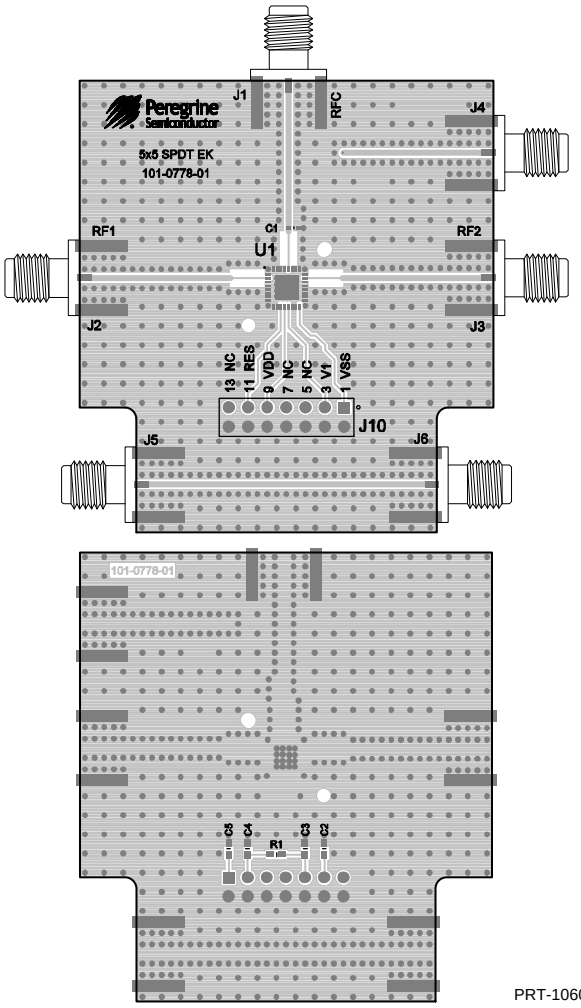


Figure 15. Evaluation Board Schematic

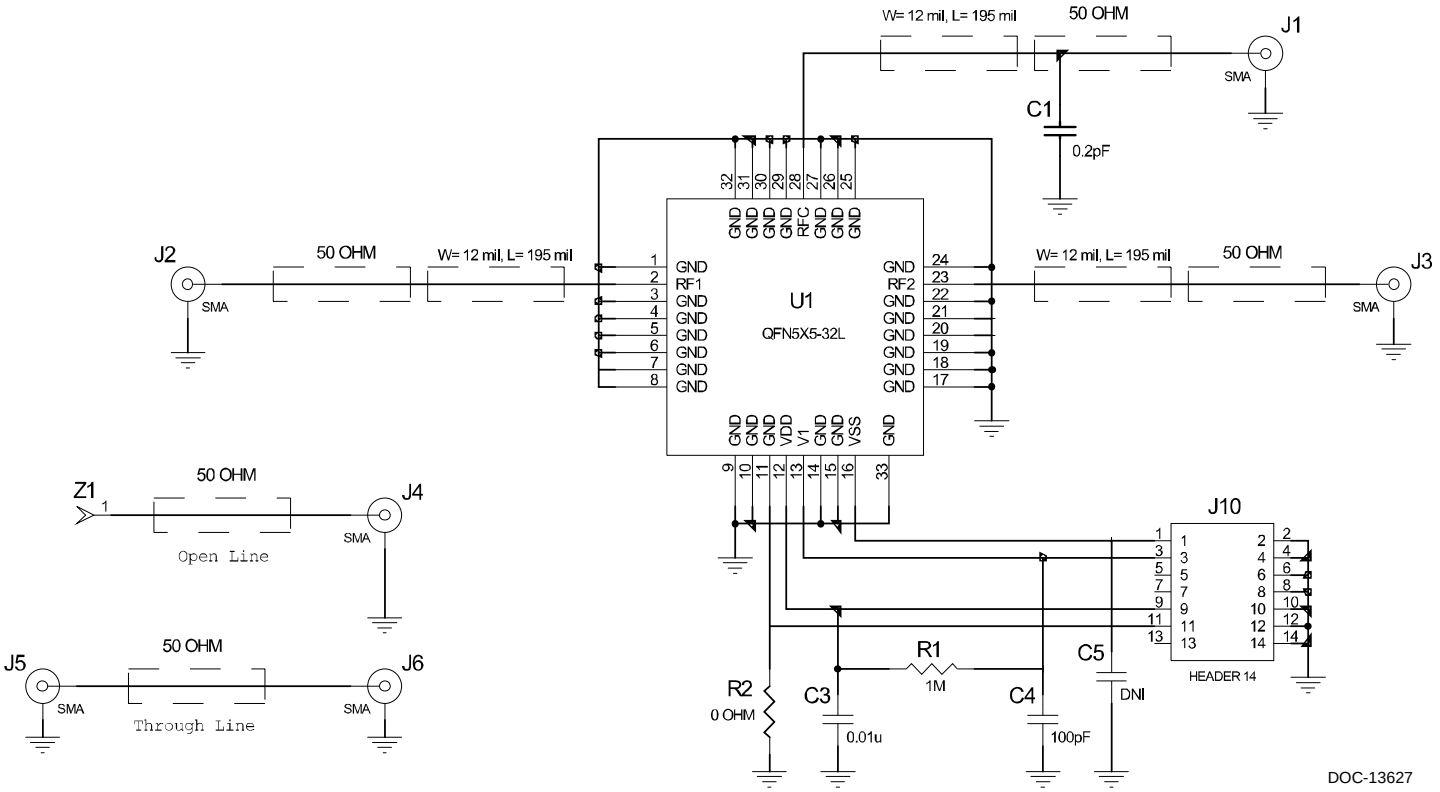


Figure 16. Package Drawing

32-lead 5x5 mm QFN

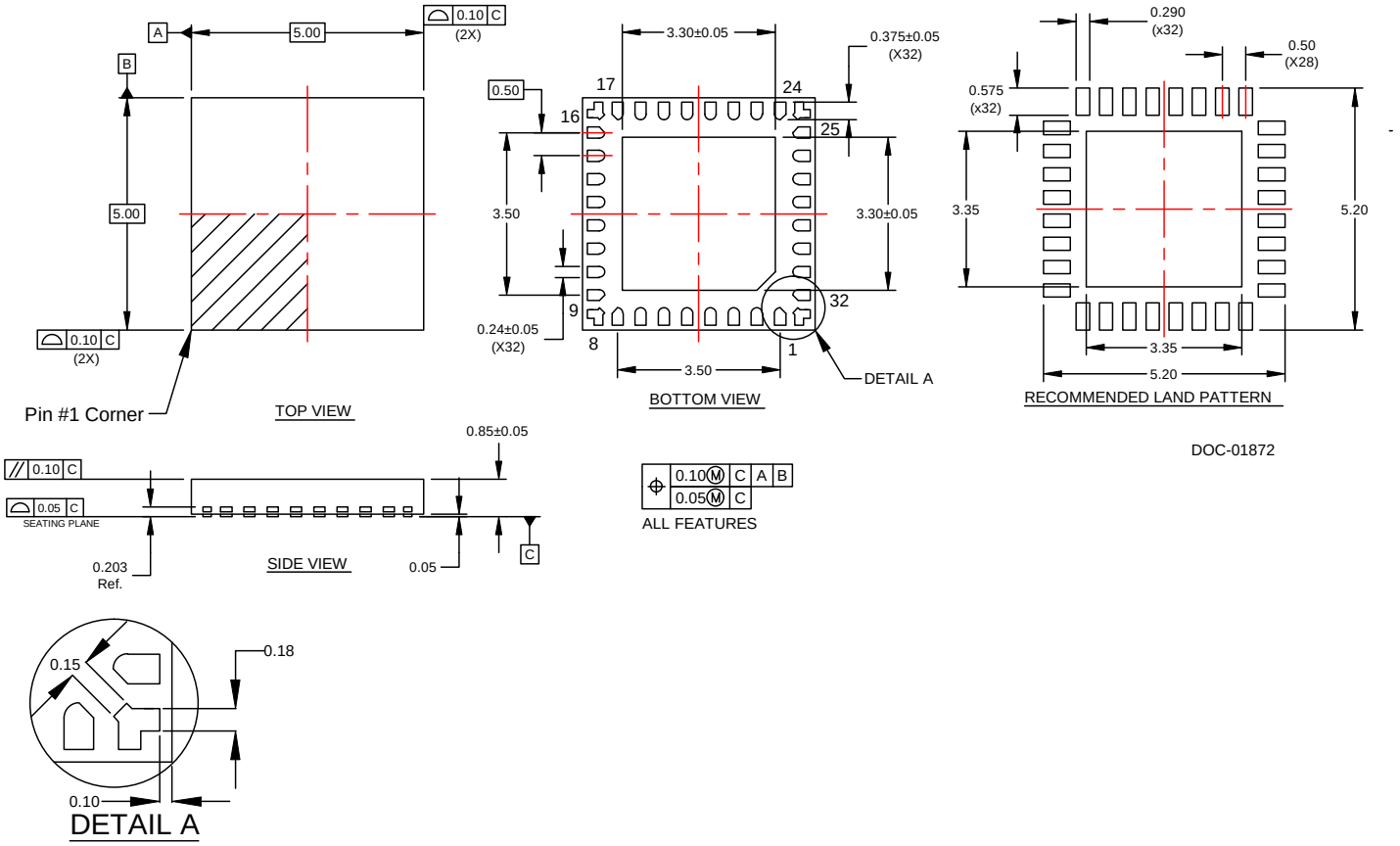
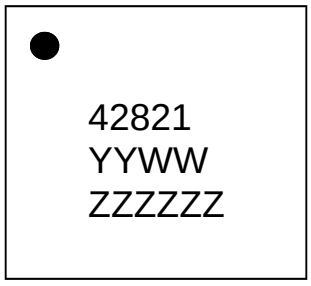


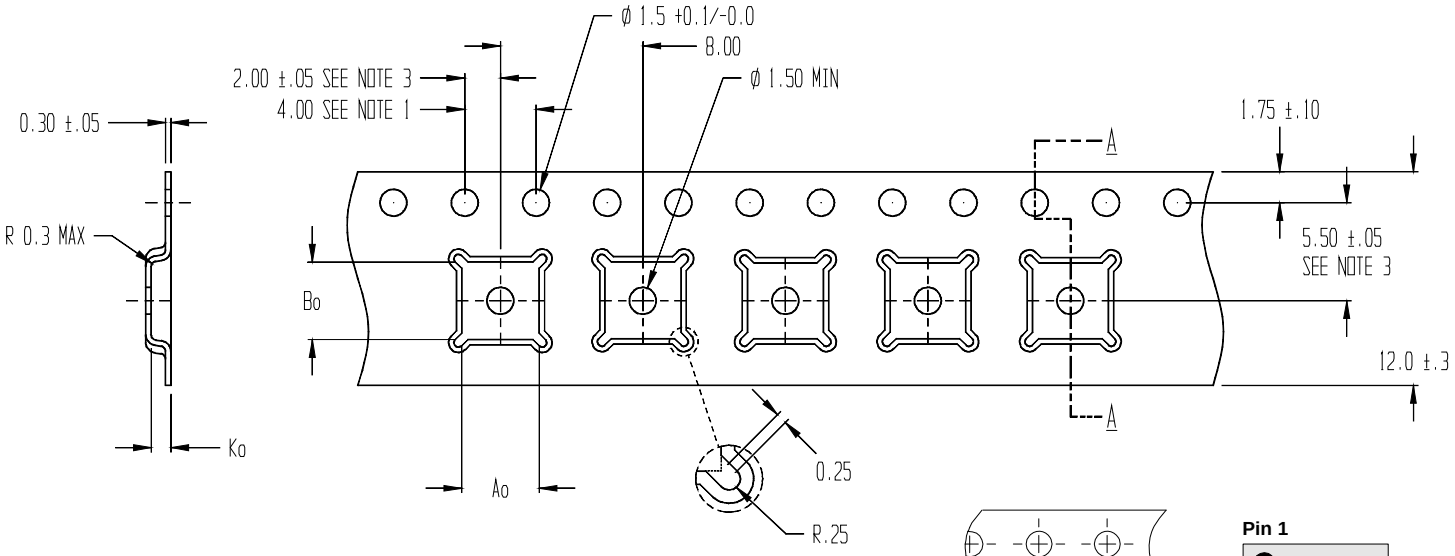
Figure 17. Top Marking Specification



17-0085

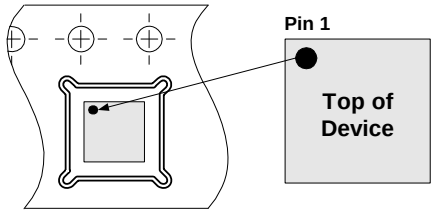
● = Pin 1 indicator
YYWW = Date code, last two digits of the year and work week
ZZZZZZ = Six digits of the lot number

Figure 18. Tape and Reel Specs



Notes:
1. 10 sprocket hole pitch cumulative tolerance ± 0.2.
2. Camber in compliance with EIA 481.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Ao = 5.25 ± 0.1 mm
Bo = 5.25 ± 0.1 mm
Ko = 1.10 ± 0.1 mm



Device Orientation in Tape

Table 7. Ordering Information

Order Code	Description	Package	Shipping Method
PE42821MLBA-X	PE42821 SPDT RF switch	Green 32-lead 5 × 5 mm QFN	500 units/T&R
EK42821-02	PE42821 Evaluation kit	Evaluation kit	1/Box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

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