

PE4270

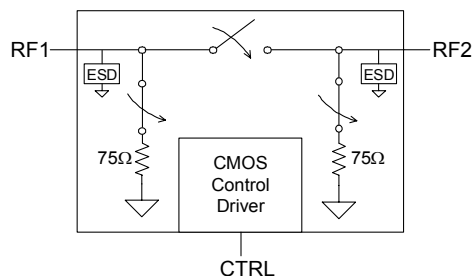
Product Description

The PE4270 is a high-isolation Switch designed for CATV applications, covering a broad frequency range from 1 to 3000 MHz. This single-supply SPST switch offers a single-pin CMOS control interface with industry leading CTB performance. It also provides low insertion loss, high isolation and extremely low bias requirements while operating on a single 3-volt supply. In a typical CATV application, the PE4270 provides for a cost effective and manufacturable solution vs. mechanical relays.

The PE4270 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

Peregrine Specification 71/0010



SPST CATV UltraCMOS™ Switch 1 - 3000 MHz

Features

- Integrated 0.25 watt terminations
- CTB performance of 90 dBc
- High isolation: 90 dB at 5 MHz, 63 dB at 1000 MHz
- Low insertion loss: 0.5 dB at 50 MHz, 0.70 dB at 1000 MHz
- High input IP2: >80 dBm
- CMOS/TTL single-pin control
- Single +3-volt supply operation
- Extremely low bias: 8 μ A @ 3 V
- Available in a 6-lead DFN package

Figure 2. Package Type

6-lead DFN

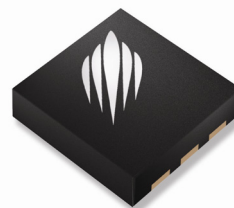


Table 1. Electrical Specifications @ +25 °C ($Z_S = Z_L = 75 \Omega$)

Parameter	Condition	Minimum	Typical	Maximum	Units
Operating Frequency ¹		1		3000	MHz
Insertion Loss	1 – 50 MHz 1000 MHz		0.50 0.70	0.65 0.85	dB
Isolation	1 – 50 MHz 1000 MHz	85 60	90 63		dB
Return Loss	5 - 1000 MHz, $V_{CTRL} = 3.0V$	15	16		dB
1 dB Compression ^{2,4}	1000 MHz	28	30		dBm
CTB / CSO	77 & 110 channels; PO = 44 dBmV		-90		dBc
Input IP2 ²	1000 MHz	80			dBm
Input IP3 ²	1000 MHz	50			dBm
Video Feedthrough ³				15	mV _{pp}
Switching Time			2		μ S

Notes: 1. Device linearity will begin to degrade below 1 MHz.

2. Measured in a 50 Ω system.

3. Measured with a 1 ns risetime, 0/3 V pulse and 500 MHz bandwidth.

4. Note Absolute Maximum ratings in Table 3.

Figure 3. Pin Configuration

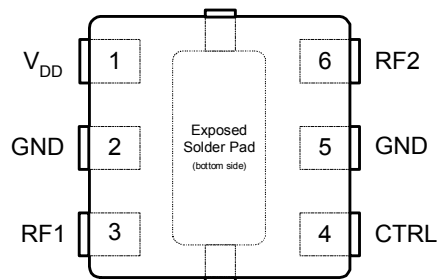


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V _{DD}	Nominal 3 V supply connection.
2	GND	Ground connection. ²
3	RF1	RF port. ¹
4	CTRL	CMOS or TTL logic level: High = RF1 to RF2 signal path Low = RF1 isolated from RF2
5	GND	Ground connection. ³
6	RF2	RF port. ¹

Notes: 1. Both RF pins must be held at 0 V_{DC} or require external DC blocking capacitors

2. The exposed pad must be soldered to the ground plane for proper switch performance.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V _{DD}	Power supply voltage	-0.3	4.0	V
V _I	Voltage on CTRL input	-0.3	5.5	V
T _{ST}	Storage temperature	-65	150	°C
P _{IN}	Input power (50 Ω), CTRL=1/CTRL=0		33/24	dBm
V _{ESD}	ESD voltage (Human Body Model)		500	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE4270 in the 6-lead 3x3 DFN package is MSL1.

Table 4. Operating Ranges

Parameter	Min	Typ	Max	Unit
V _{DD} Power Supply	2.7	3.0	3.3	V
I _{DD} Power Supply Current (V _{DD} = 3V, V _{CTRL} = 3V)		8	20	μA
T _{OP} Operating temperature	-40		85	°C
Control Voltage High	0.7xV _{DD}		5	V
Control Voltage Low	0		0.3xV _{DD}	V

Table 5. Control Logic Truth Table

Control Voltage (CTRL)	Signal Path (RF1 to RF2)
High ¹	ON
Low	OFF

Notes: 1. CTRL accepts both CMOS and TTL voltage levels.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Device Description

The PE4270 high isolation SPST CATV Switch is designed to support CATV applications such as premise disconnect of a CATV signal path. This function is typically performed by bulky and expensive mechanical relays. The high isolation characteristics, high compression point, and integrated 75-ohm terminations make the PE4270 an ideal, cost effective and manufacturable product of choice.

The control logic input pin (CTRL) is typically driven by a 3-volt CMOS logic level signal, and has a threshold of 50% of V_{DD}. For flexibility to support systems that have 5-volt control logic drivers, the control logic input has been designed to handle a 5-volt logic HIGH signal. (A minimal current will be sourced out of the V_{DD} pin when the control logic input voltage level exceeds V_{DD}.)

Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)
(75 Ω impedance except as indicated)

Figure 4. Insertion Loss - RF1 to RF2

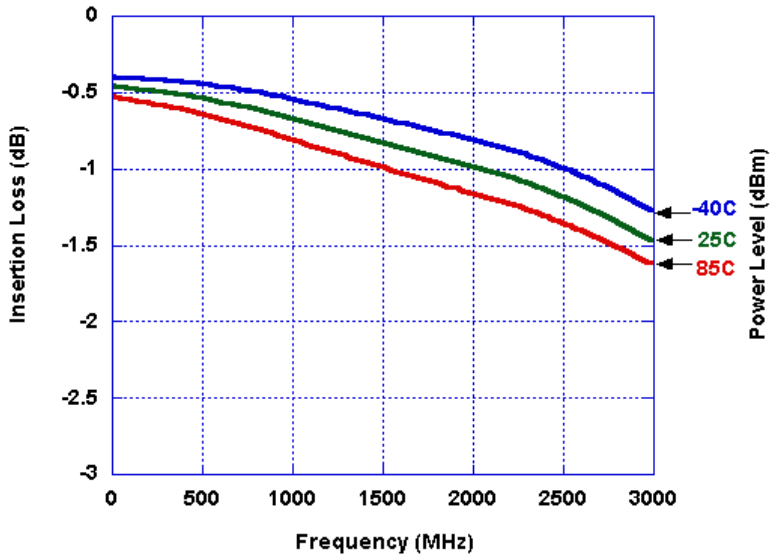


Figure 5. 1dB Compression & 3rd Order Intercept Point (T = 25°C)

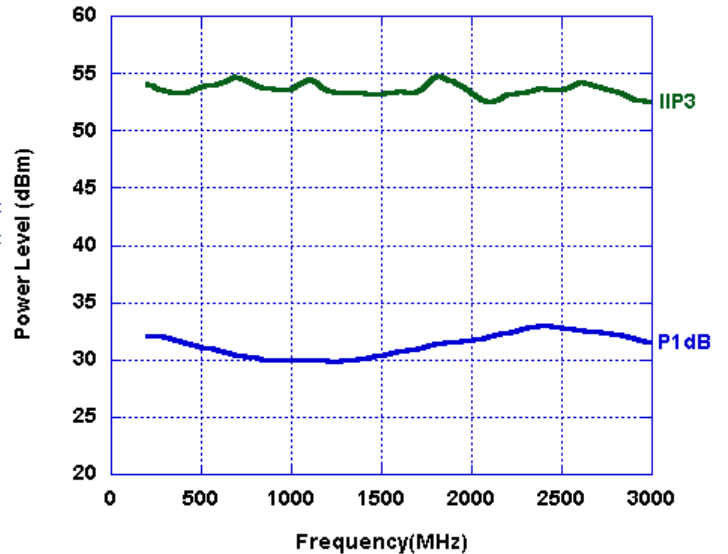
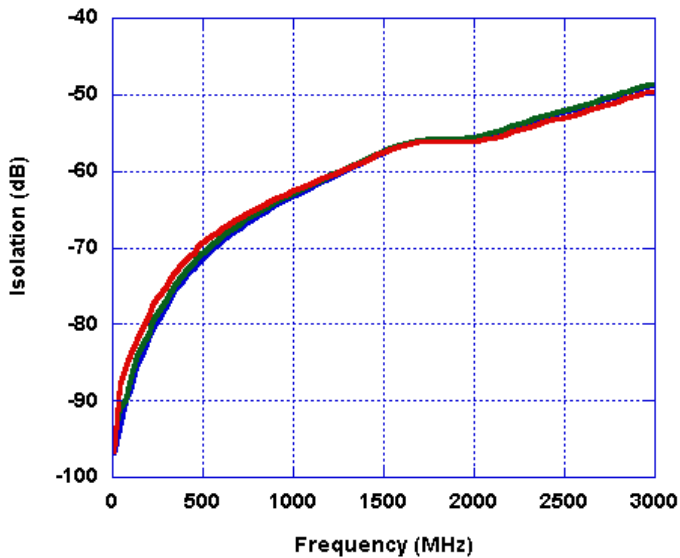


Figure 6. Isolation - RF1 to RF2



Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)
(75-ohm impedance)

Figure 7. RF1 Return Loss (Switch = ON)

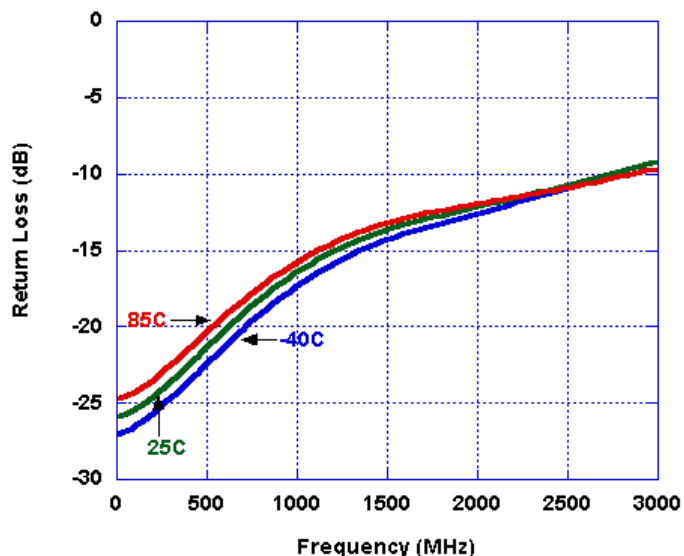


Figure 8. RF1 Return Loss (Switch = OFF)

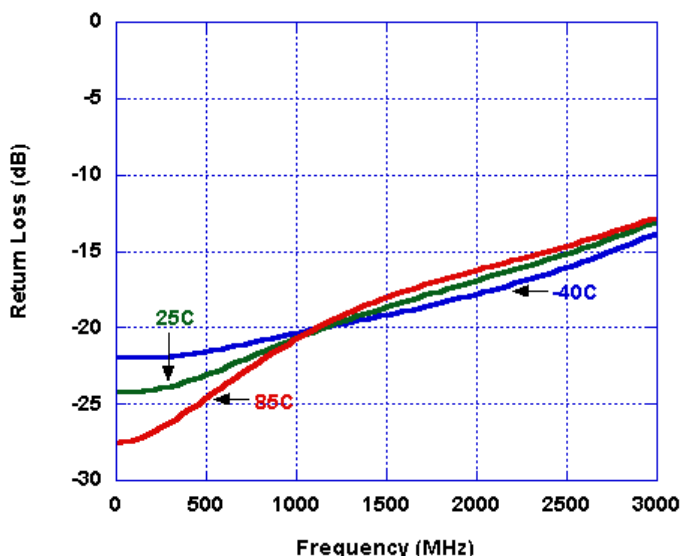


Figure 9. RF2 Return Loss (Switch = ON)

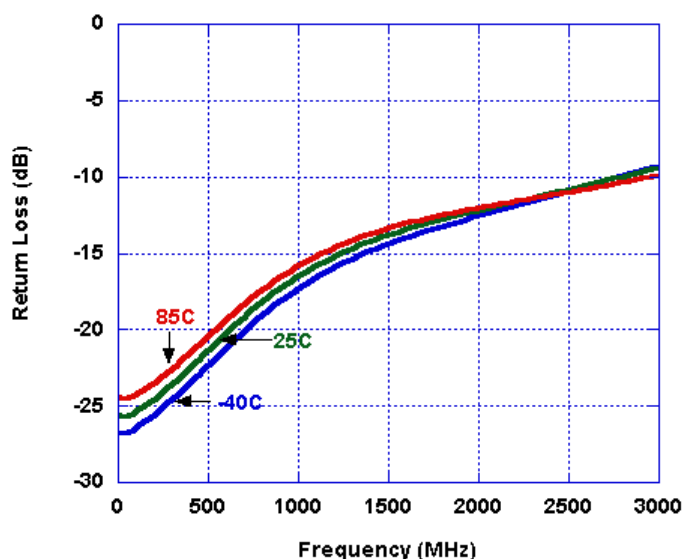
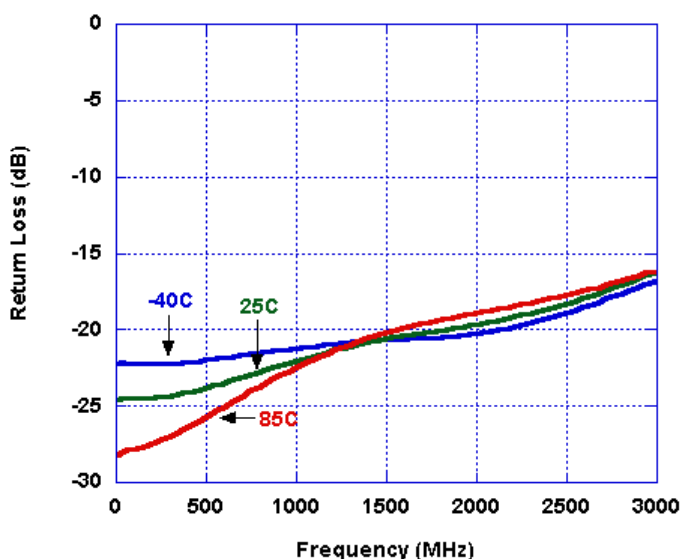


Figure 10. RF2 Return Loss (Switch = OFF)



Evaluation Kit

The *PE4270* EK board was designed to ease customer evaluation of Peregrine's high performance SPST CATV MOSFET switch. RF1 is connected through a 75 Ω transmission line via the top left F connector, J1. RF2 is connected through a 75 Ω transmission line via the top right F connector, J2. A 75 Ω through transmission line is available via F connectors J3 and J4. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. V_{DD} is supplied via J6-2, while the control logic voltage is supplied via J5-2. It is the responsibility of the customer to determine proper supply decoupling for their design application. It has been observed that by removing C1 and C2 from the evaluation board has not shown to degrade RF performance.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide model with trace width of 0.021", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ϵ_r of 4.6. Note that the predominate mode for these transmission lines is coplanar waveguide with a ground plane.

Figure 11. Evaluation Board Layouts

Peregrine Specification 101/0167 (with F connectors)

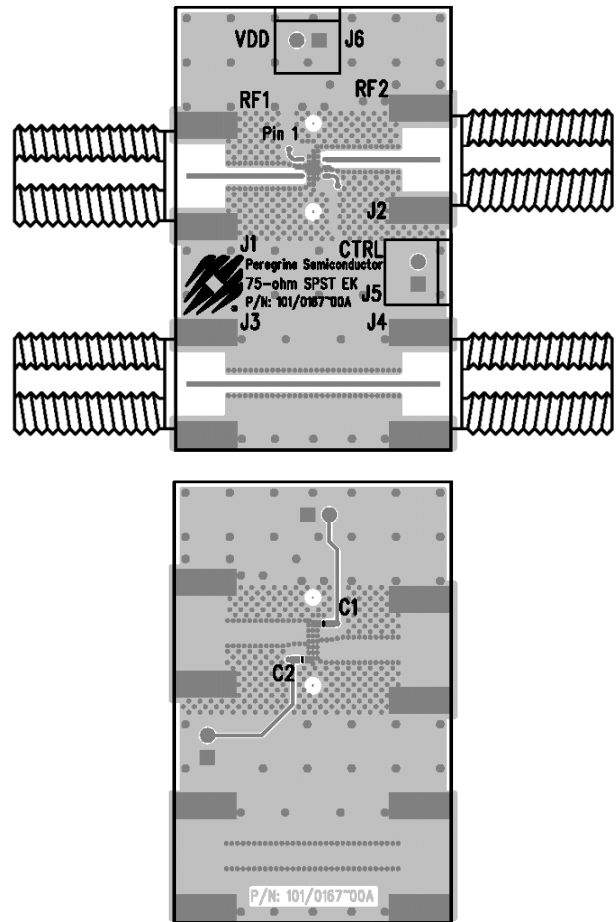


Figure 12. Evaluation Board Schematic

Peregrine Specification 102/0224

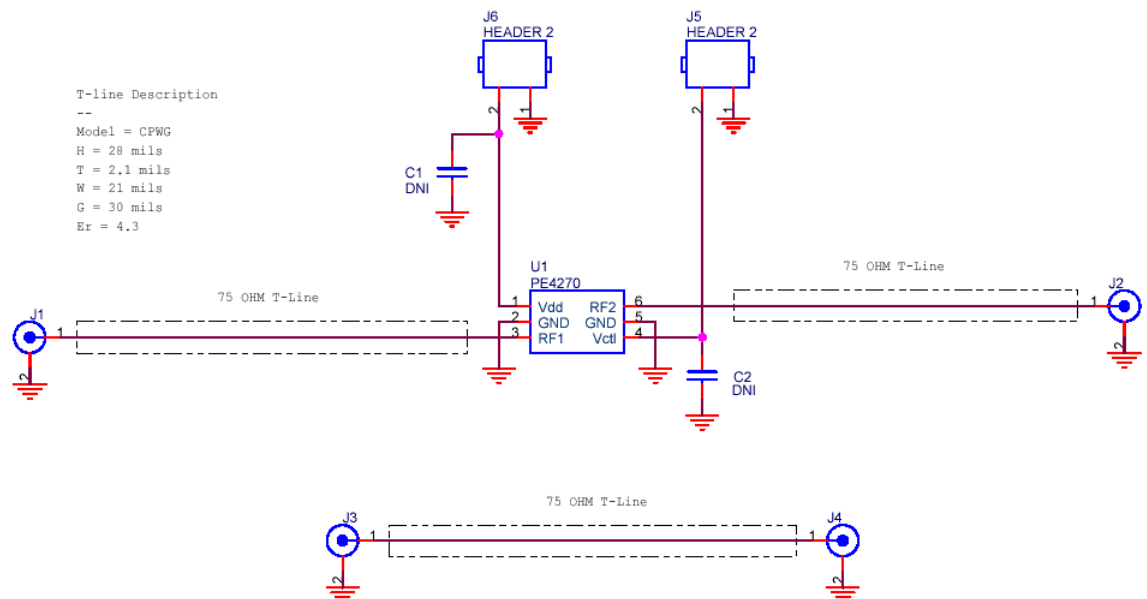
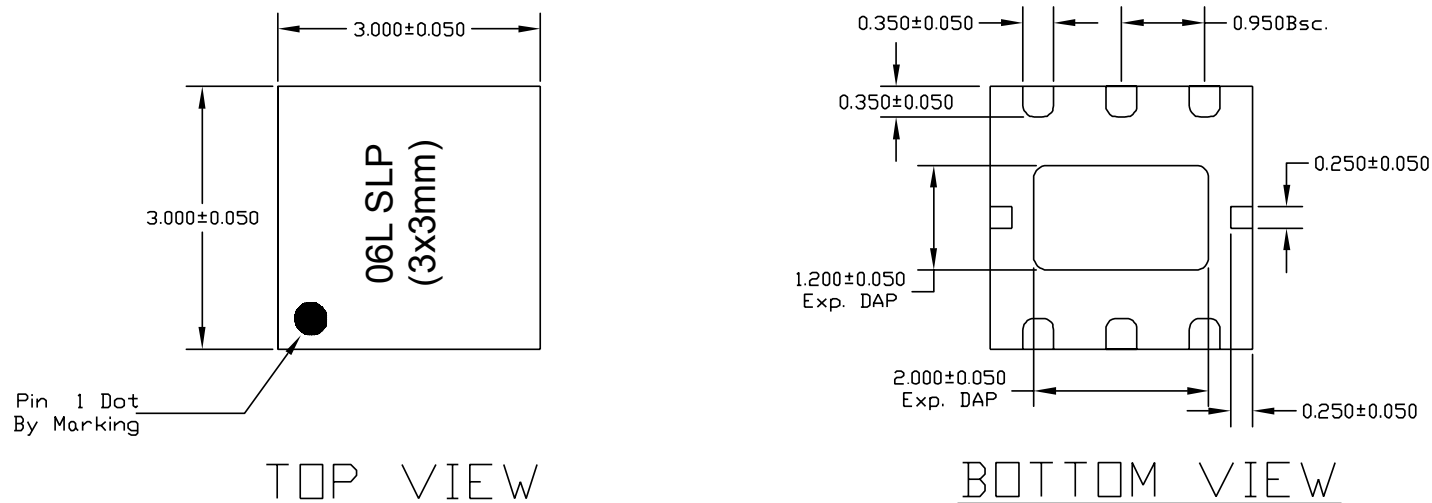


Figure 13. Package Drawing

6-lead DFN



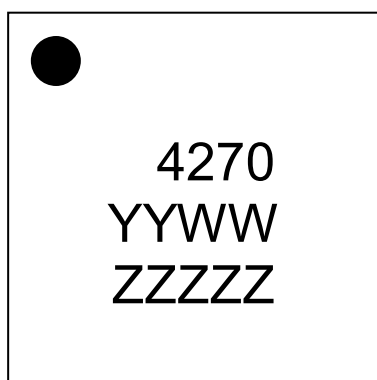
NOTE:

1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

NOTE: The exposed solder pad (on the bottom of the package) is not electrically connected to any other pin (isolated).

Figure 14. Marking Specifications



YYWW = Date Code (last two digits of year and work week)
ZZZZZ = Last five digits of Lot Number

6-lead DFN



Note: R7 = 7 inch Lock Reel, R13 = 13 inch Lock Reel

Order Code	Part Marking	Description	Package	Shipping Method
4270-51	4270	PE4270G-06DFN 3x3mm-12800F	Green 6-lead 3x3 mm DFN	Tape or loose
4270-52	4270	PE4270G-06DFN 3x3mm-3000C	Green 6-lead 3x3 mm DFN	3000 units / T&R
4270-00	PE4270-EK	PE4270-06DFN 3x3mm-EK	Evaluation Kit	1 / Box

NOTES:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
2. CAMBER IN COMPLIANCE WITH ETA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Sales Offices

The Americas

Peregrine Semiconductor Corporation

9380 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe

Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-4741-9173
Fax : +33-1-4741-9173

High-Reliability and Defense Products

Americas

San Diego, CA, USA
Phone: 858-731-9475
Fax: 848-731-9499

Europe/Asia-Pacific

Aix-En-Provence Cedex 3, France
Phone: +33-4-4239-3361
Fax: +33-4-4239-7227

Peregrine Semiconductor, Asia Pacific (APAC)

Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

Peregrine Semiconductor, Korea

#B-2607, Kolon Tripolis, 210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-943 South Korea
Tel: +82-31-728-3939
Fax: +82-31-728-3940

Peregrine Semiconductor K.K., Japan

Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

For a list of representatives in your area, please refer to our Web site at: www.psemi.com

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS, HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp.