

Product Specification PE4263 DIE

SP6T UltraCMOS[™] 2.6 V Switch 100 – 3000 MHz

Figure 1. Functional Diagram



Figure 2. Die Top View



Features

- Three pin CMOS logic control with integral decoder/driver
- Low TX insertion loss: 0.55 dB at 900 MHz, 0.65 dB at 1900 MHz
- TX RX Isolation of 48 dB at 900 MHz, 40 dB at 1900 MHz
- Low harmonics: $2f_o = -85 \text{ dBc}$ and $3f_o = -72 \text{ dBc}$
- 1500 V HBM ESD tolerance all ports
- 41 dBm P1dB
- No blocking capacitors required

Product Description

The PE4263 SP6T RF UltraCMOS[™] Switch addresses the specific design needs of the Quad-Band GSM Handset Antenna Switch Module Market. On-chip CMOS decode logic facilitates three-pin low voltage CMOS control. High ESD tolerance of 1500 V at all ports, no blocking capacitor requirements and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ruggedness.

The PE4263 UltraCMOS[™] RF Switch is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.



Parameter	Conditions	Typical	Units	
Operational Frequency			MHz	
	ANT - TX - 850 / 900 MHz	0.55	dB	
Incention Land	ANT - TX - 1800 / 1900 MHz	0.65	dB	
Insertion Loss	ANT - RX - 850 / 900 MHz	0.90	dB	
	ANT - RX - 1800 / 1900 MHz	1.00	dB	
	TX - RX - 850 / 900 MHz	48	dB	
	TX - RX - 1800 / 1900 MHz	40	dB	
	TX - TX - 850 / 900 MHz	29	dB	
Isolation	TX - TX - 1800 / 1900 MHz	25	dB	
	ANT - TX - 850 / 900 MHz	31	dB	
	ANT - TX - 1800 / 1900 MHz	25	dB	
Datamatana	850 / 900 MHz	22	15	
Return Loss	1800 / 1900 MHz	23	aв	
2nd Harmonic	35 dBm TX Input - 850 / 900 MHz	-85		
	33 dBm TX Input - 1800 / 1900 MHz	-81	dBc	
3rd Harmonic	35 dBm TX Input - 850 / 900 MHz	-72	in	
	33 dBm TX Input - 1800 / 1900 MHz -66		dBC	
Switching Time	(10-90%) (90-10%) RF	2	μs	

Table 1. Electrical Specifications @ +25 °C, V_{DD} = 2.6 V ($Z_S = Z_L = 50 \Omega$)

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1²	ANT	RF Common – Antenna
2 ²	TX1	RF I/O - TX1
3 ¹	GND	Ground (Requires two bond wires)
4 ²	TX2	RF I/O – TX2
51	GND	Ground
6 ¹	GND	Ground
7	V _{DD}	Supply
8	V3	Switch control input, CMOS logic level
9 ¹	GND	Ground
10	V2	Switch control input, CMOS logic level
11	V1	Switch control input, CMOS logic level
12¹	GND	Ground
13¹	GND	Ground
14 ²	RX4	RF I/O – RX4
15 ¹	GND	Ground
16 ²	RX3	RF I/O – RX3
17 ¹	GND	Ground
18 ²	RX2	RF I/O – RX2
19 ¹	GND	Ground
20 ²	RX1	RF I/O – RX1

Notes: 1. Bond wires should be physically short and connected to ground plane for best performance.

2. Blocking capacitors needed only when non-zero DC voltage present.

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Figure 3. Pin Configuration (Top View)



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Table 3.	Absolute	Maximum	Ratings
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Symbol	Parameter/Conditions	Min	Max	Units	
V _{DD}	Power supply voltage	-0.3	4.0	V	
Vı	Voltage on any input	-0.3	V _{DD} + 0.3	V	
T_{ST}	Storage temperature range	-65	+150	°C	
T _{OP}	Operating temperature range	-40	+85	°C	
_	TX input power (50 Ω) ¹		+38	3	
P _{IN}	RX input power (50 Ω) ¹		+23	dBm	
	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		1500	V	
V _{ESD}	ESD Voltage (MM, JEDEC, JESD22-A114-B)		100	V	
	ESD Voltage (CDM, JEDEC, JESD22-C101-A)		2000	V	
	ESD Voltage at ANT Port (IEC 61000-4-2)		1700	V	

Note: 1. Max RF specified with V_{DD} applied

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the DC Electrical Specifications table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 4. DC Electrical Specifications

Parameter	Min	Тур	Max	Units
V _{DD} Supply Voltage	2.4	2.6	2.8	V
I_{DD} Power Supply Current ($V_{DD} = 2.6V$)		13	20	μA
Control Voltage High	0.7 x V _{dd}			V
Control Voltage Low			$0.3 \text{ x V}_{\text{DD}}$	V

Table 5. Truth Table

Path	V3	V2	V1
ANT – RX1	0	0	0
ANT – RX2	0	0	1
ANT – RX3	0	1	0
ANT – RX4	0	1	1
ANT - TX1	1	0	х
ANT - TX2	1	1	х

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS[™] device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS[™] devices are immune to latch-up.

 Table 6. Ordering Information

Order Code	Die ID	Description	Package	Shipping Method
4263-92	C9797_3	PE4263-DIE-D	Film Frame	Wafer (Gross Die / Wafer Quantity)
4263-98	C9797_3	PE4263-DIE-400G	Waffle Pack	400 Dice / Waffle Pack
4263-10	C9797_3	PE4263-DIE-1H	Evaluation Kit	1/ box



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Data Sheet Identification

Advance Information

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Preliminary Specification

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Product Specification

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