

PE4256

Document category: Product Specification

75 Ω SPDT CATV UltraCMOS® Switch, 5 MHz–3 GHz



Features

- 75 Ω characteristic impedance
- Integrated 75 Ω terminations
- CTB performance of –90 dBc
- High isolation: 65 dB at 1000 MHz
- Low insertion loss:
 - 0.5 dB at 5 MHz, typ.
 - 0.9 dB at 1000 MHz, typ.
- High input IP3: >50 dBm
- CMOS two-pin control
- Single +3V supply operation
- Low current consumption: 8 μ A
- Unique all-off terminated mode
- Package: 4 x 4 mm QFN

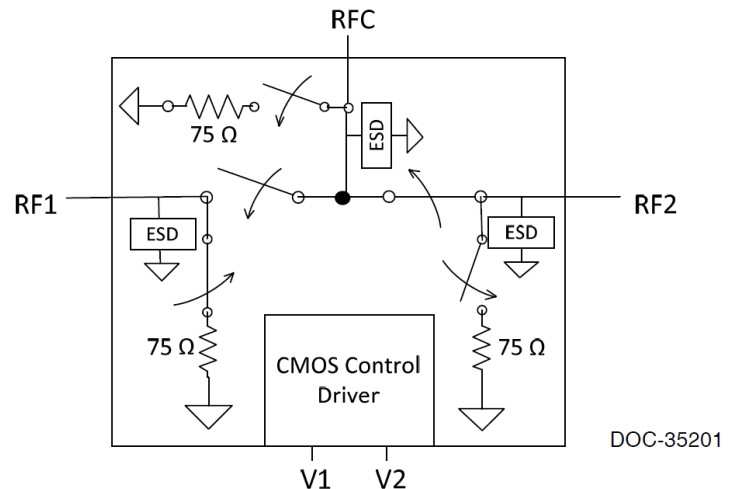



Figure 1. PE4256 functional diagram

Product description


The PE4256 is an UltraCMOS® Switch designed for CATV applications, covering a broad frequency range from 5 MHz up to 3 GHz. This single-supply SPDT switch integrates a two-pin CMOS control interface. It also provides low insertion loss with extremely low bias requirements while operating on a single 3-volt supply. In a typical CATV application, the PE4256 provides a cost-effective and manufacturable solution when compared to mechanical relays.

The PE4256 is manufactured on pSemi's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute maximum ratings

 Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

 When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE4256 absolute maximum ratings

| Symbol | Parameter or condition | Min | Max | Unit |
|------------------|--------------------------------|------|-----------------------|------|
| V _{DD} | Power supply voltage | -0.3 | 4.0 | V |
| V _I | Voltage on CTRL input | -0.3 | V _{DD} + 0.3 | V |
| P _{RF} | RF CW power | – | 24 | dBm |
| T _{ST} | Storage temperature | -65 | +150 | °C |
| T _{OP} | Operating temperature | -40 | +85 | °C |
| V _{ESD} | ESD voltage (Human Body Model) | – | 1000 | V |

Electrical specifications

Table 2 lists the PE4256 key electrical specifications at +25 °C, $V_{DD} = +3V$ ($Z_S = Z_L = 75\Omega$), unless otherwise specified.

Table 2. PE4256 electrical specifications

| Parameter | Condition | Min | Typ | Max | Unit |
|---------------------------------------|---|----------------------|--------------------------|---------------------------|------------------|
| Operating frequency ⁽¹⁾ | – | 5 | – | 3000 | MHz |
| Insertion loss | 5–250 MHz 250–750 MHz 750–1000 MHz 1000–2200 MHz | – | 0.5 0.8 0.9 1.1 | 0.6 0.95 1.1 1.3 | dB |
| Isolation | 5–250 MHz 250–750 MHz 750–1000 MHz 1000–2200 MHz | 75 65 62 49 | 80 70 65 52 | – | dB |
| Input IP2 ⁽²⁾ | 5–1000 MHz | – | 80 | – | dBm |
| Input IP3 ⁽²⁾ | 5–1000 MHz | 50 | 55 | – | dBm |
| Input 1-dB compression ⁽²⁾ | 1000 MHz | 29 | 31 | – | dBm |
| CTB/CSO | 77 and 110 channels; Power out = 44 dBmV | – | -90 | – | dBc |
| Switching time | 50% CTRL to 10/90% RF | – | 2 | – | μs |
| Video feedthrough ⁽³⁾ | 51000 MHz | – | – | 15 | mV _{pp} |



1. Device linearity begins to degrade below 5 MHz.
2. Measured in a 50Ω system.
3. Measured with a 1-ns rise time, 0/3V pulse, and 500 MHz bandwidth.

Table 3 lists the PE4256 DC electrical specifications at +25 °C, unless otherwise specified.

Table 3. PE4256 DC electrical specifications

| Parameter | Min | Typ | Max | Unit |
|---|--------------|-----|--------------|------|
| V_{DD} power supply | 2.7 | 3.0 | 3.3 | V |
| I_{DD} power supply current ($V_{DD} = 3V$, $V_{CNTL} = 3V$) | – | 8 | 20 | μA |
| Control voltage high | 70% V_{DD} | – | – | V |
| Control voltage low | – | – | 30% V_{DD} | V |

SPDT control logic

Table 4 lists the RF path truth table.

Table 4. RF path truth table


| C1 | C2 | RFc-RF1 | RFc-RF2 |
|------|------|--------------------|--------------------|
| Low | Low | OFF | OFF |
| Low | High | OFF | ON |
| High | Low | ON | OFF |
| High | High | N/A ^(*) | N/A ^(*) |

 * The PE4256 operation is not supported in the C1 = VDD and C2 = VDD state.

Table 5 lists the termination truth table.

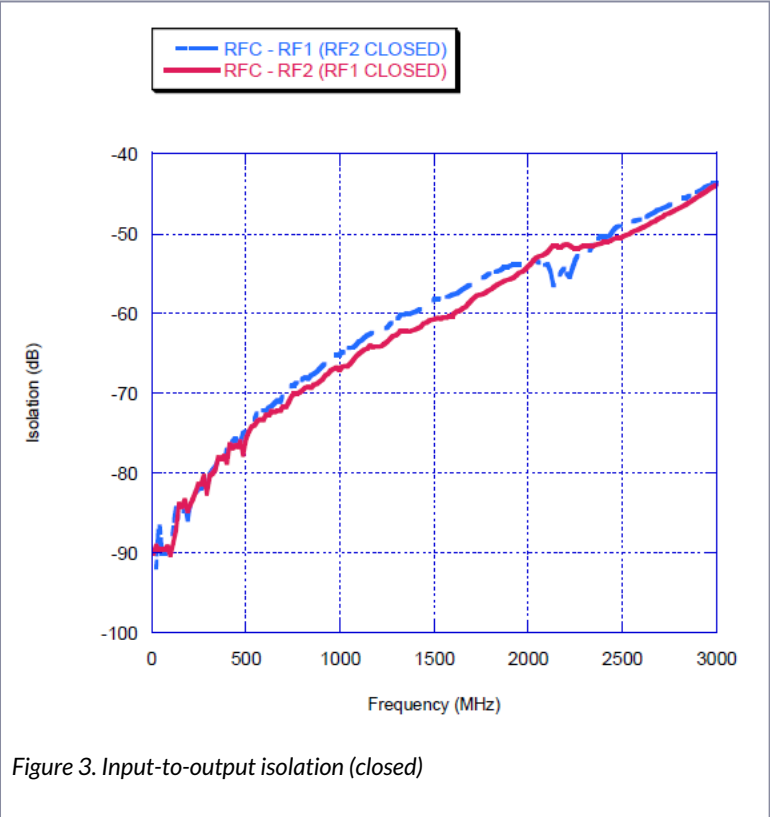
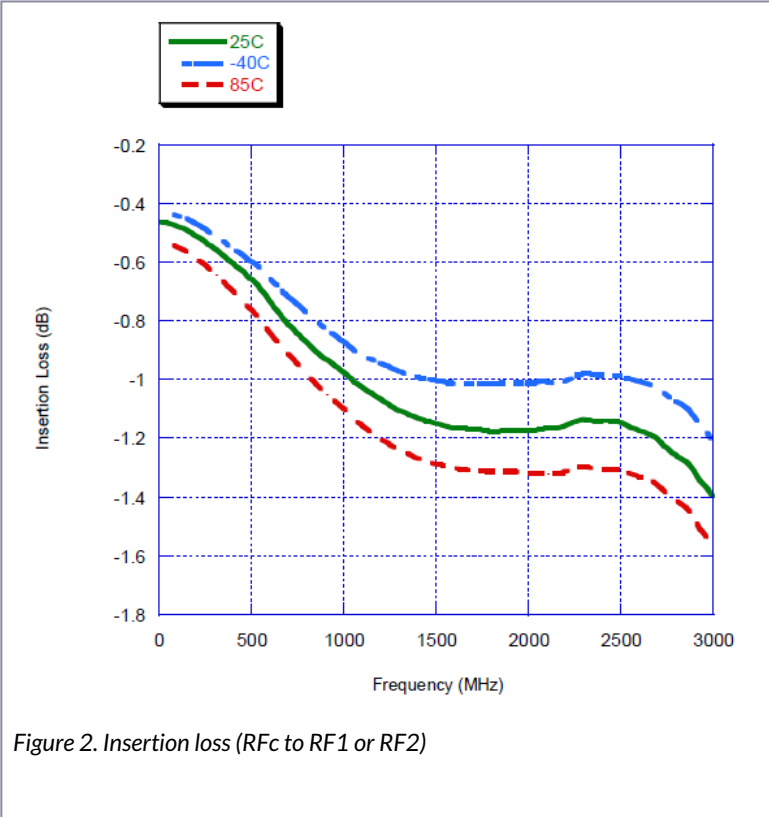
Table 5. Termination truth table

| C1 | C2 | RFc-75Ω | RF1-75Ω | RF2-75Ω |
|------|------|--------------------|--------------------|--------------------|
| Low | Low | X ⁽²⁾ | X ⁽²⁾ | X ⁽²⁾ |
| Low | High | - | X ⁽²⁾ | - |
| High | Low | - | - | X ⁽²⁾ |
| High | High | N/A ⁽¹⁾ | N/A ⁽¹⁾ | N/A ⁽¹⁾ |

-  1. The PE4256 operation is not supported in the C1 = V_{DD} and the C2 = V_{DD} state.
2. "X" denotes termination enabled.

Typical performance data

Figure 2–Figure 9 show the typical performance data from -40 °C to +85 °C, 75Ω impedance, unless otherwise specified.



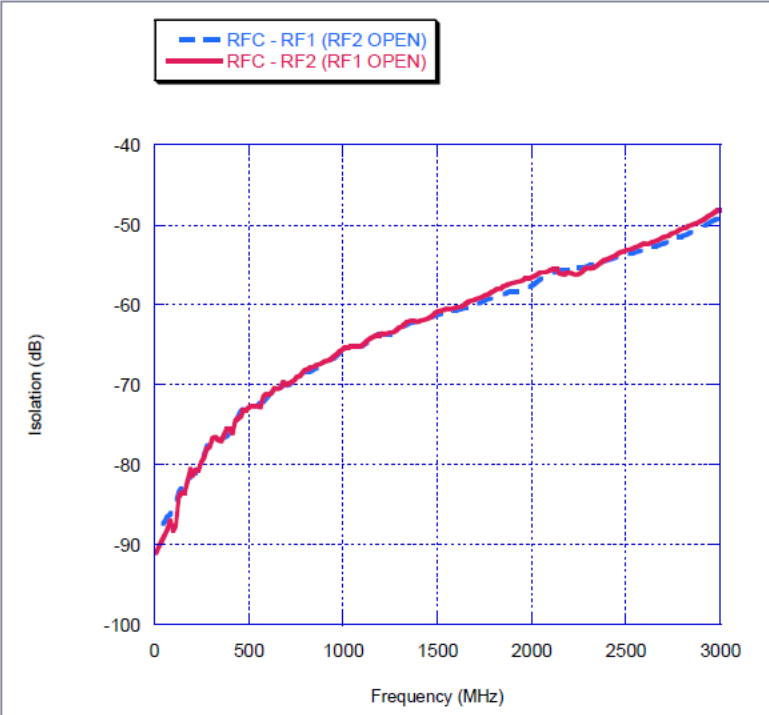


Figure 4. Input-to-output isolation (open)

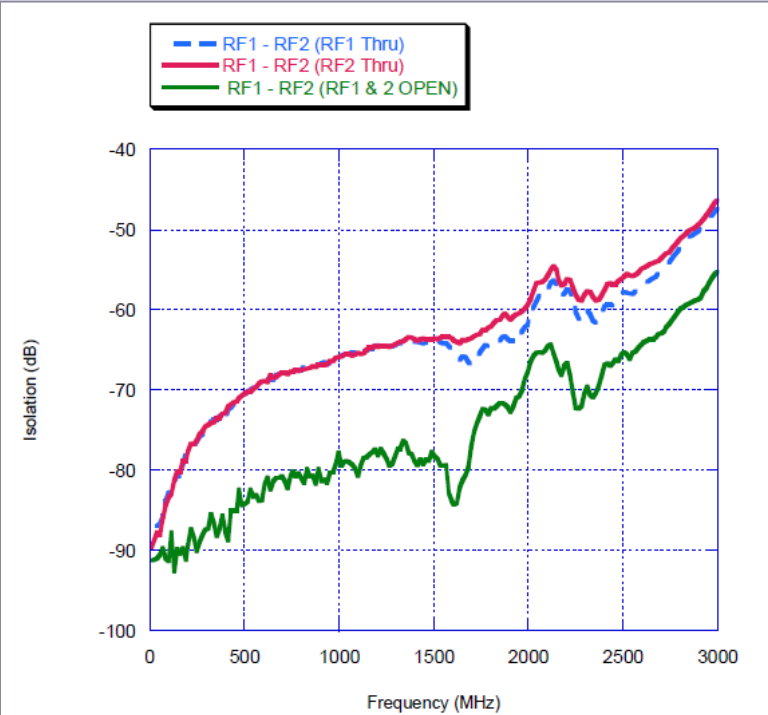


Figure 5. Isolation – RF1 to RF2

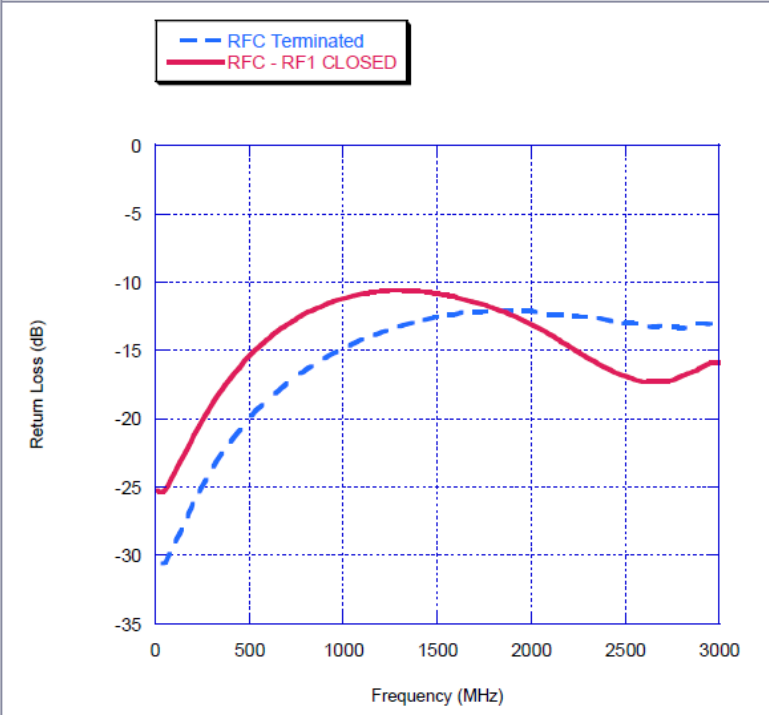


Figure 6. RFC return loss

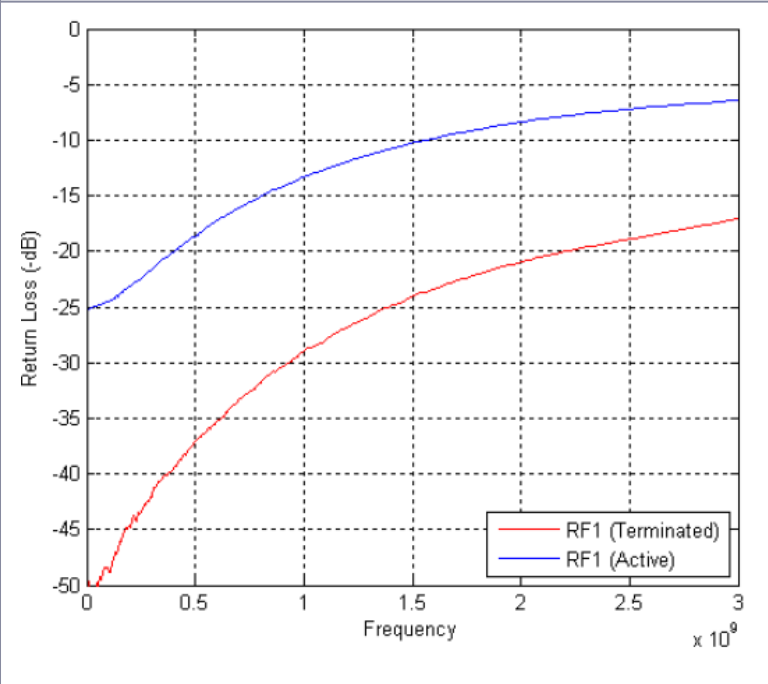


Figure 7. RF1 return loss

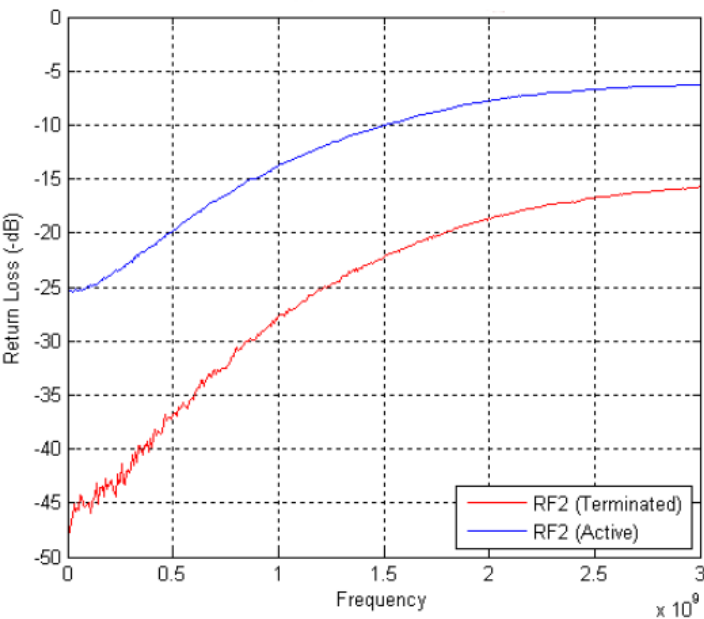


Figure 8. RF2 return loss

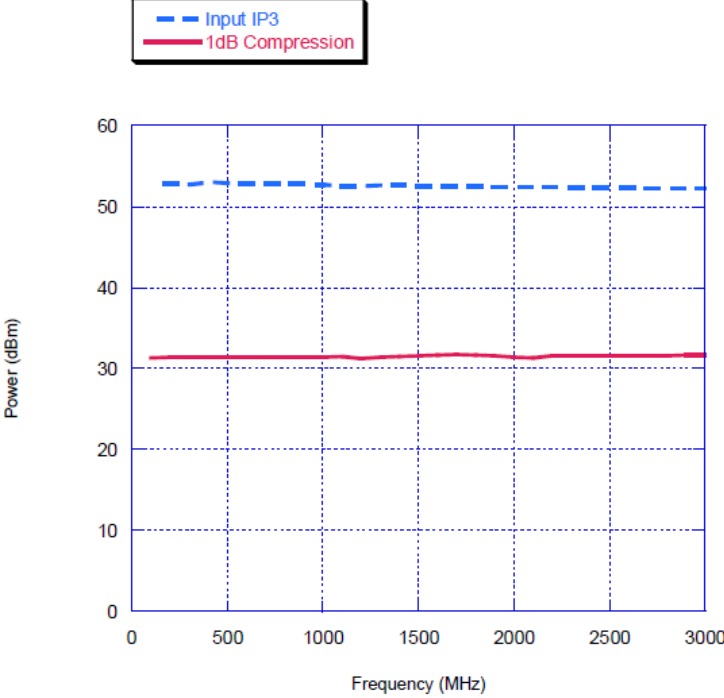


Figure 9. Linearity (50Ω system impedance)

Evaluation kit

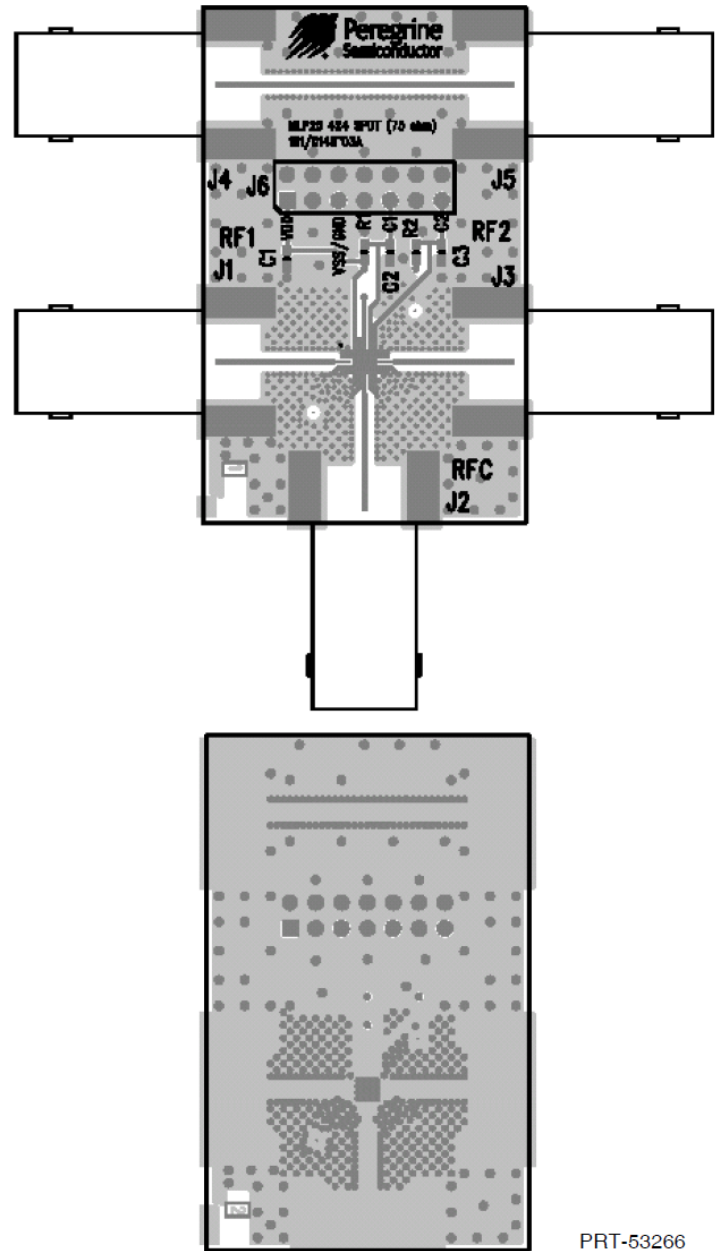
The SPDT Switch Evaluation Kit was designed to ease customer evaluation of the PE4256 SPDT switch. The RF common port (RFC) is connected through a 75Ω transmission line to J2. Ports 1 and 2 connect through 75Ω transmission lines to J1 and J3. A through transmission line connects F connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed with four metal layers in FR4 material with a total thickness of 0.062". The transmission lines were designed using a coplanar waveguide with ground plane (28-mil core, 21-mil width, 30-mil gap).

J6 provides a means for controlling DC and digital inputs to the device. The provided jumpers short the package pin to ground for logic low. When the jumper is removed, the pin is pulled up to V_{DD} for logic high.

When the jumper is in place, 3 μA of current flows through the 1 MΩ pull-up resistor. Do not attribute this extra current to the device.

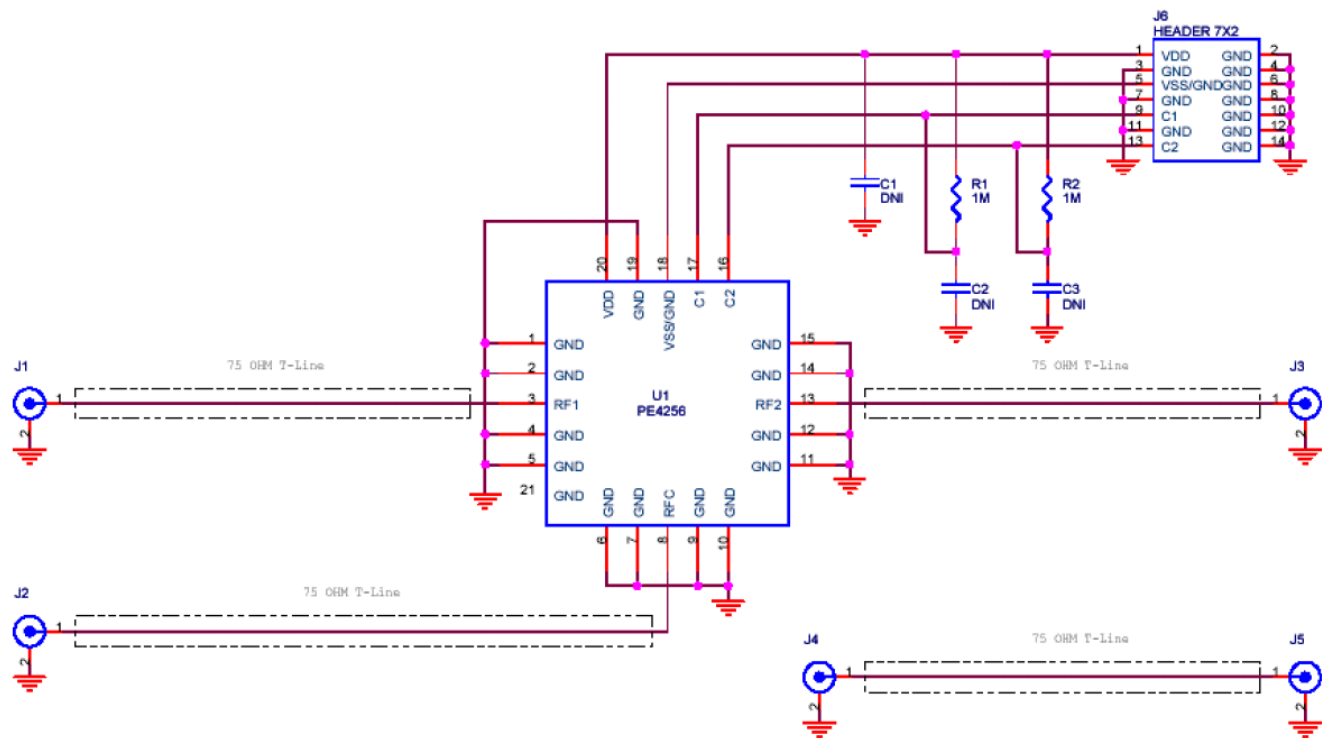
Proper PCB design is essential for full isolation performance. This evaluation board demonstrates good trace and ground management for minimum coupling and radiation.



PRT-53266

Figure 10. Evaluation board layouts

Evaluation board schematic



DOC-40738

Figure 11. Evaluation board schematic

Pin information

Figure 12 shows the PE4256 pin map for the 20-lead 4 x 4 mm QFN package, and Table 6 lists the description for each pin.

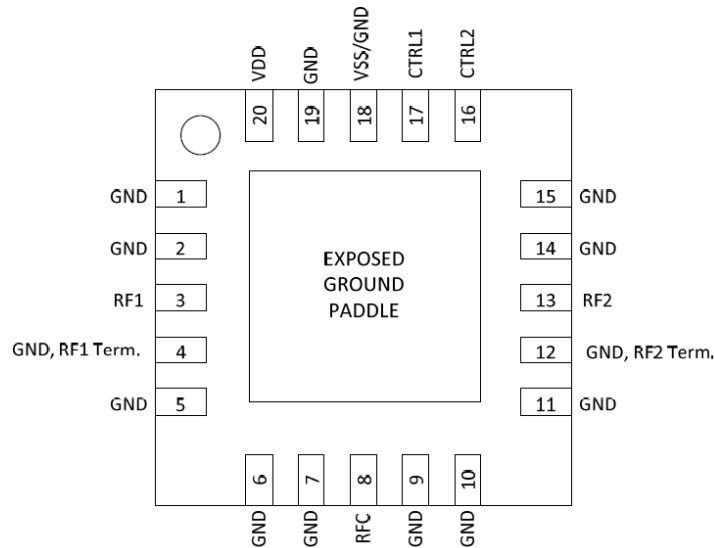


Figure 12. Pin configuration (top view)



- 1. Pins 3, 8, and 13 must be at 0 VDC. The RF pins do not required blocking capacitors if the 0 VDC requirement is met.
- 2. Pins 16 and 17 are the CMOS controls that set the three operating states.
- 3. To enable the internal negative voltage generator, connect pin 18 to GND (the PE4256 has a maximum 25 kHz switching rate when the internal negative voltage generator is used). To bypass and disable the internal negative voltage generator, connect pin 18 to V_{SS} (-3V).
- 4. You can add external resistance to ground to change the termination resistance.

Table 6. PE4256 pin descriptions

| Pin no. | Pin name | Description |
|-------------------|----------|------------------------|
| 1 | GND | Ground |
| 2 | GND | Ground |
| 3 ⁽¹⁾ | RF1 | RF I/O |
| 4 ⁽⁴⁾ | GND | Ground |
| 5 | GND | Ground |
| 6 | GND | Ground |
| 7 ⁽⁴⁾ | GND | Ground |
| 8 ⁽¹⁾ | RFC | RF common |
| 9 ⁽⁴⁾ | GND | Ground |
| 10 | GND | Ground |
| 11 | GND | Ground |
| 12 ⁽⁴⁾ | GND | Ground |
| 13 ⁽¹⁾ | RF2 | RF I/O |
| 14 | GND | Ground |
| 15 | GND | Ground |
| 16 ⁽²⁾ | C2 | Control 2 |
| 17 ⁽²⁾ | C1 | Control 1 |
| 18 ⁽³⁾ | VSS/GND | Negative supply option |
| 19 | GND | Ground |
| 20 | VDD | Supply |
| Paddle | GND | Exposed ground paddle |

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE4256 moisture sensitivity level rating for the 20-lead 4 x 4 mm QFN package is MSL1.

Package drawing

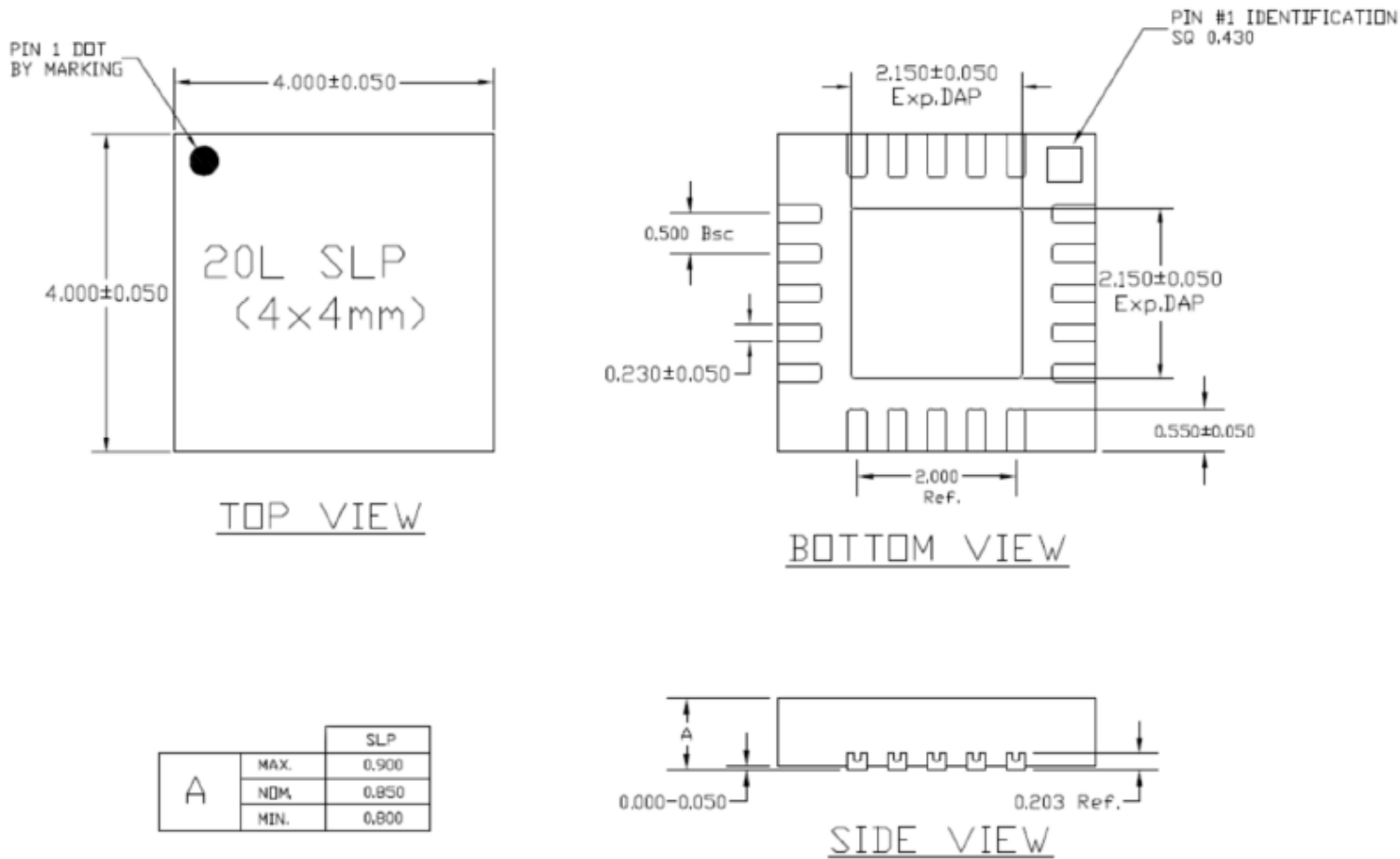
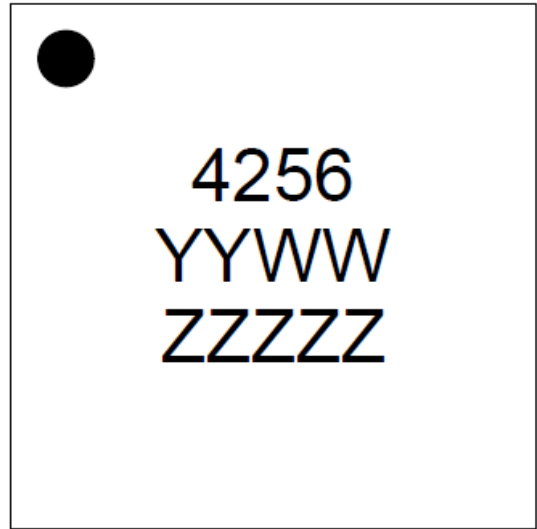


Figure 13. Package mechanical drawing for the 20-lead 4 x 4 mm QFN package

Top-marking specification



YYWW = Date Code
ZZZZZ = Last five digits of PSC Lot Number

Figure 14. PE4256 package marking specification

Tape and reel specification

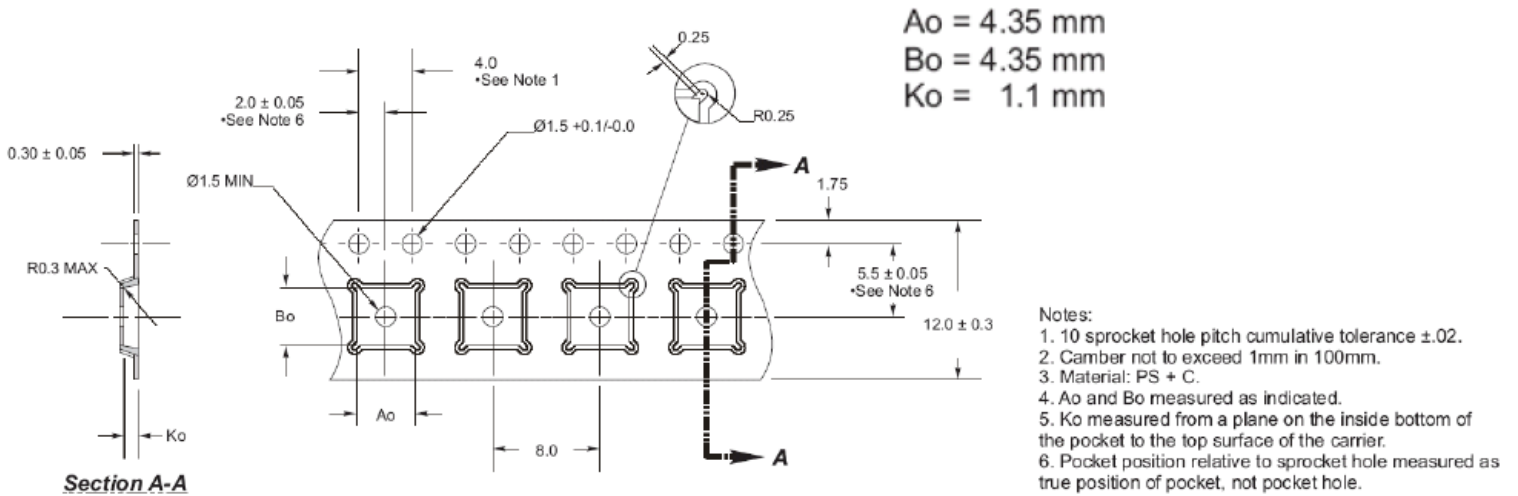


Figure 15. Tape and reel specification for the 20-lead 4 x 4 mm QFN package

Ordering information

| Order code | Description | Packaging | Shipping method |
|---------------|----------------------------|---|-----------------|
| PE4256MLIAA-Z | PE4256-20QFN 4 x 4 mm-3000 | Green 20-lead 4 x 4 mm QFN, NiPdAu Lead Finish | 3000 units/T&R |
| EK4256-01 | PE4256-20QFN 4 x 4 mm-EK | Evaluation kit | 1/box |

Document categories

| | |
|----------------------------------|---|
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