PE42452

Document category: Product Specification

UltraCMOS® SP5T RF Switch, 450–4000 MHz

Features

- Five symmetric, absorptive RF ports
- High isolation:
  - 61 dB @ 900 MHz
  - 55 dB @ 2100 MHz
  - 52 dB @ 2700 MHz
  - 44 dB @ 4000 MHz
- High linearity:
  - IIP2: 96 dBm
  - IIP3: 57 dBm
- 1.8V control logic compatible
- Operating temperature: 105°C
- Fast switching time: 265 ns
- Three-pin CMOS logic control
- External negative supply option
- ESD performance:
  - 4 kV HBM on RF pins to GND
  - 1.5 kV HBM on all pins
- Package: 24-lead 4 × 4 mm QFN

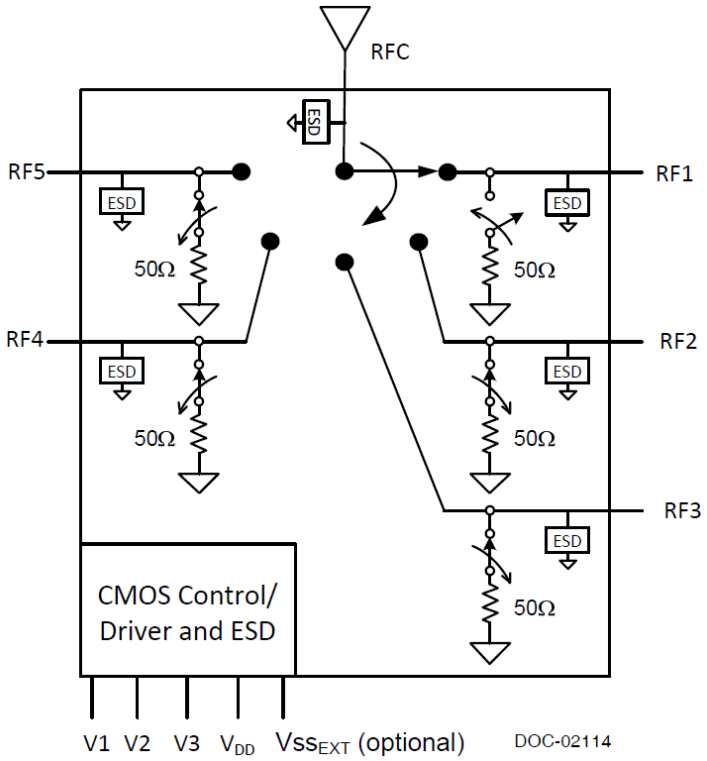


Figure 1. PE42452 functional diagram

Product description

The PE42452 is a HaRP™ technology-enhanced absorptive SP5T RF switch designed for use in 3G/4G wireless infrastructure and other high performance RF applications.

This switch is a pin-compatible upgraded version of the PE42451 with 1.8V control logic. It consists of five symmetric RF ports and has extremely high isolation. An integrated CMOS decoder facilitates a three-pin low voltage CMOS control interface and an external negative supply option. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE42452 is manufactured using the pSemi UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

The pSemi HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS® process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE42452 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Voltage on any DC input	V_I	-0.3	3.6	V
Maximum input power	$P_{MAX,ABS}$	–	34	dBm
Storage temperature range	T_{ST}	-60	+150	°C
ESD voltage HBM[1]: All pins RF pins to GND	$V_{ESD,HBM}$	–	 1500 4000	V
ESD voltage MM[2], all pins	$V_{ESD,MM}$	–	100	V
ESD voltage CDM[3], all pins	$V_{ESD,CM}$	–	500	V

1. Human Body Model (MIL_STD 883 Method 3015)
2. Machine Model (JEDEC JESD22-A115)
3. Charged Device Model (JEDEC JESD22-C101D)

Recommended operating conditions

Table 2 lists the PE42452 recommending operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE42452 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Normal mode[1]					
Supply voltage	V_{DD}	2.3	–	5.5	V
Supply current	I_{DD}	–	110	–	µA
Bypass mode[2]					
Supply voltage	V_{DD}	2.7	–	5.5	V
Supply current	I_{DD}	–	50	–	µA
Negative supply voltage	VSS_{EXT}	-3.6	–	-3.2	V
Normal or bypass mode					
Digital input high (V1, V2, V3)	V_{IH}	1.17	–	3.6	V
Digital input low (V1, V2, V3)	V_{IL}	-0.3	–	0.6	V
Digital input current[3]	I_{CTRL}	–	–	1	µA
RF input power, CW	$P_{MAX,CW}$	–	–	33	dBm
RF input power into terminated ports, CW	$P_{MAX,TERM}$	–	–	24	dBm
Operating temperature range	T_{OP}	-40	–	+105	°C

1. Normal mode: To enable the internal negative voltage generator, connect pin 20 to GND.
2. Bypass mode: To bypass and disable the internal negative voltage generator, apply a negative voltage to VSSEXT (pin 20).
3. The pull-down resistor in the evaluation board schematic (Figure 16) can increase the control current.

Electrical specifications

Table 3 lists the PE42452 key electrical specifications at +25 °C (Z_S = Z_L = 50Ω), unless otherwise specified.

- Normal mode: V_{DD} = 3.3V, VSS_{EXT} = 0V, using a single external positive supply.
- Bypass mode: V_{DD} = 3.3V, VSS_{EXT} = -3.3V, using an external positive supply and an external negative supply.

Table 3. PE42452 electrical specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	450	–	4000	MHz
Insertion loss	RFC–RFx	450–900 MHz 900–2100 MHz 2100–2700 MHz 2700–4000 MHz	–	0.95 1.15 1.30 1.60	1.15 1.35 1.55 1.90	dB
Isolation	RFC–RFx	450–900 MHz 900–2100 MHz 2100–2700 MHz 2700–4000 MHz	56 52 49 41	61 55 52 44	–	dB
Isolation	RFx–RFx	450–900 MHz 900–2100 MHz 2100–2700 MHz 2700–4000 MHz	56 51 49 41	60 53 52 42	–	dB
Return loss (active port)	RFx	450–4000 MHz	–	16	–	dB
Return loss (terminated port)	RFx	450–4000 MHz	–	23	–	dB
Input 0.1 dB compression point(1)	RFC–RFx	1950 MHz	–	35	–	dBm
Input IP2	RFC–RFx	1950 MHz	–	96	–	dBm
Input IP3	RFC–RFx	1950 MHz	–	57	–	dBm
Switching time(2)	–	50% control to 10% or 90% RF	–	265	345	ns

1. The input 0.1 dB compression point is a linearity figure of merit. For the operating RF input power (50Ω), see Table 2.
2. The switching frequency describes the time duration between switching events. The switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value. The PE42452 has a maximum 25 kHz switching rate in normal mode (pin 20 = GND). A faster switching rate is available in bypass mode (pin 20 = VSS_{EXT}).

Optional external VSS control (VSS_{EXT})

For applications that require a faster switching rate or spur-free performance, the PE42452 can be operated in bypass mode. Bypass mode requires an external negative voltage in addition to an external VDD supply voltage.

As specified in Table 2, applying the external negative voltage (VSS_{EXT}) to pin 20 disables and bypasses the internal negative voltage generator.

Spurious performance

The typical PE42452 low-frequency spurious performance in normal mode is –120 dBm (pin 20 = GND). For spur-free performance, you can disable the internal negative voltage generator by applying a negative voltage to VSS_{EXT} (pin 20).

SP5T control logic

Table 4. PE42452 truth table

Mode	V3	V2	V1
All off	0	0	0
RF1 on	0	0	1
RF2 on	0	1	0
RF3 on	0	1	1
RF4 on	1	0	0
RF5 on	1	0	1
All off	1	1	0
Unsupported(*)	1	1	1

* Do not use the unsupported 111 logic state.

Typical performance data

Figure 2–Figure 14 show the typical performance data at +25 °C and V_{DD} = 3.3V, unless otherwise specified.

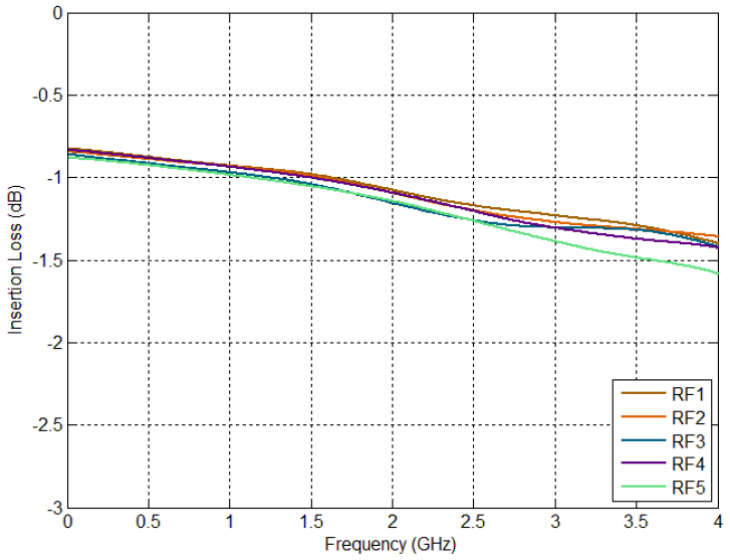


Figure 2. Insertion loss (all paths)

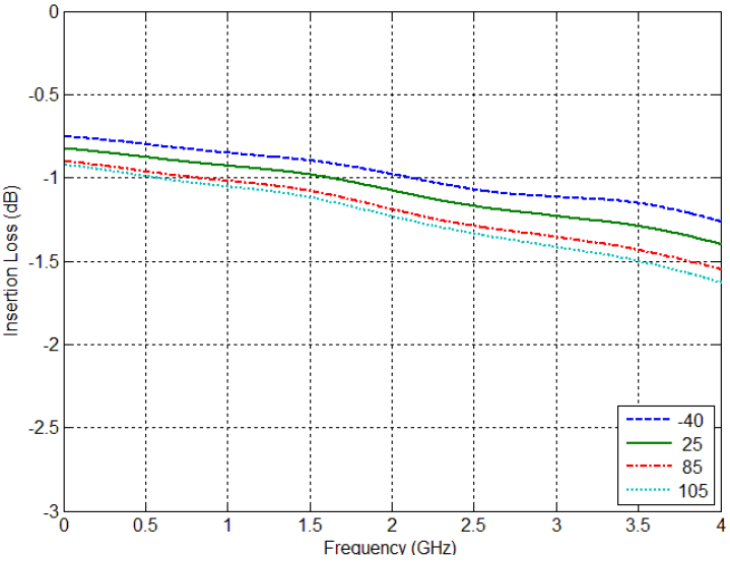


Figure 3. Insertion loss vs. temperature (RFC–RFx)

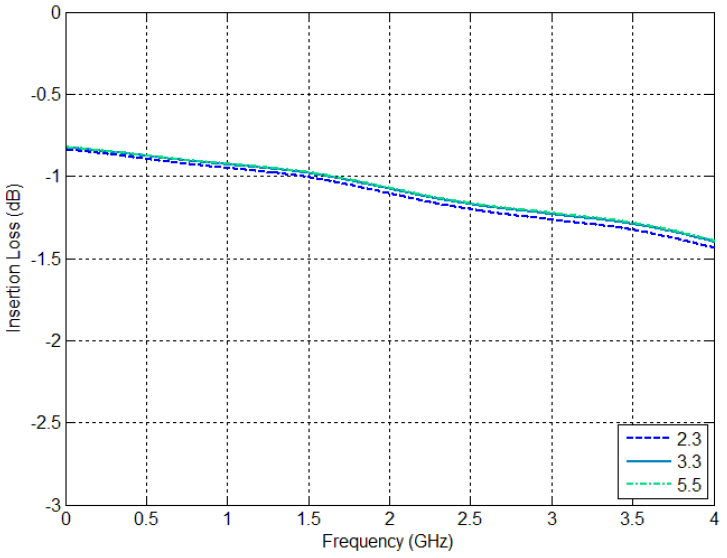


Figure 4. Insertion loss vs. V_{DD} (RFC–RFx)

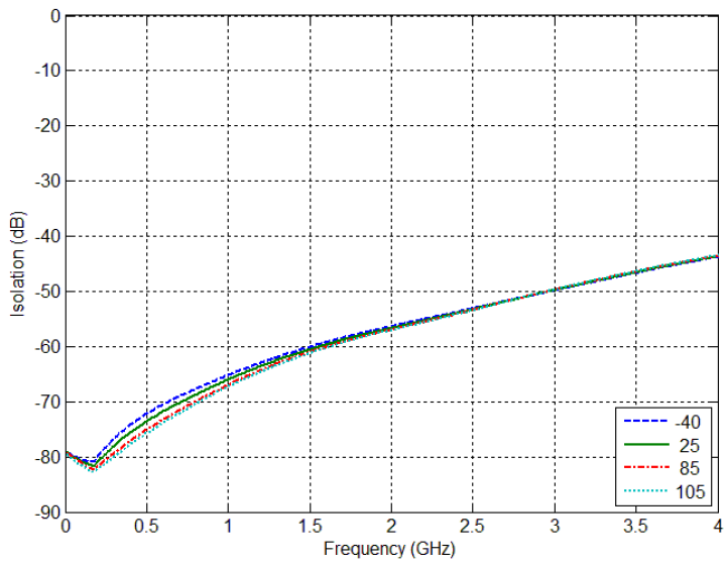


Figure 5. Isolation vs. temperature (RFC–RFx)

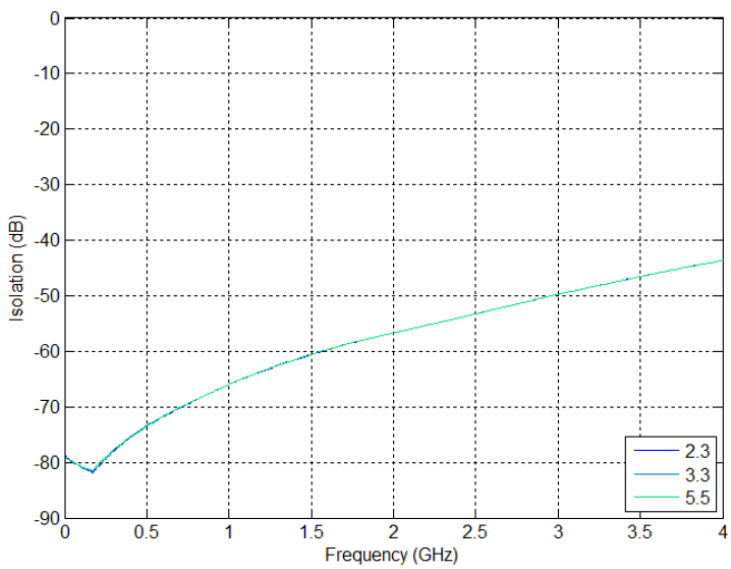


Figure 6. Isolation vs. V_{DD} (RFC–RFx)

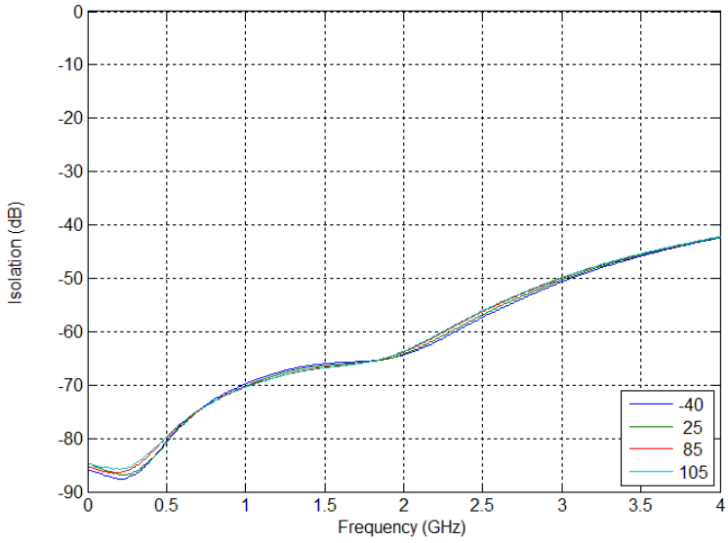


Figure 7. Isolation vs. temperature (RFx–RFx)

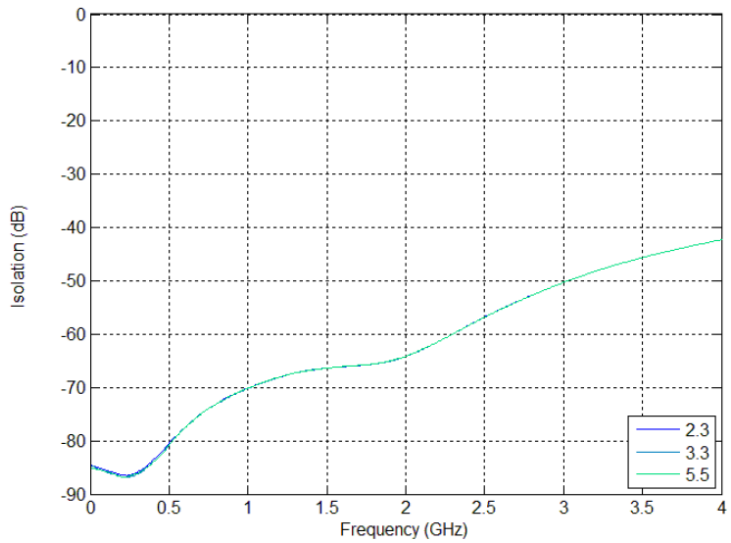


Figure 8. Isolation vs. V_{DD} (RFx–RFx)

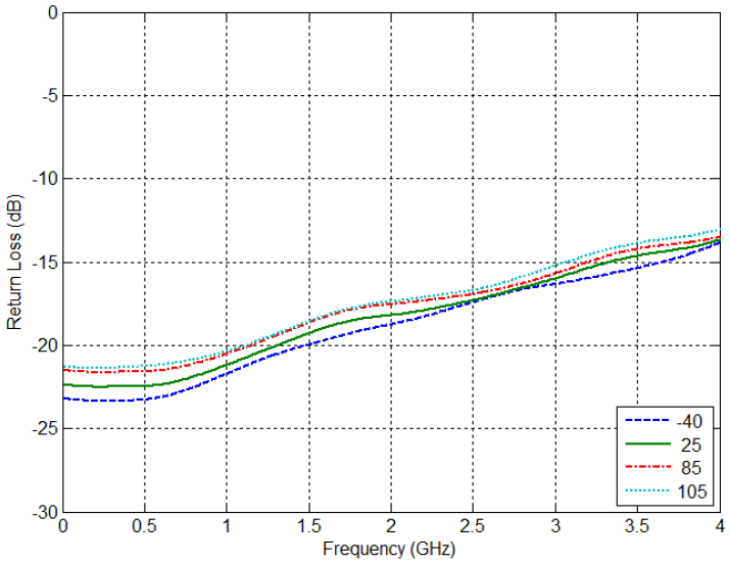


Figure 9. Active port return loss vs. temperature

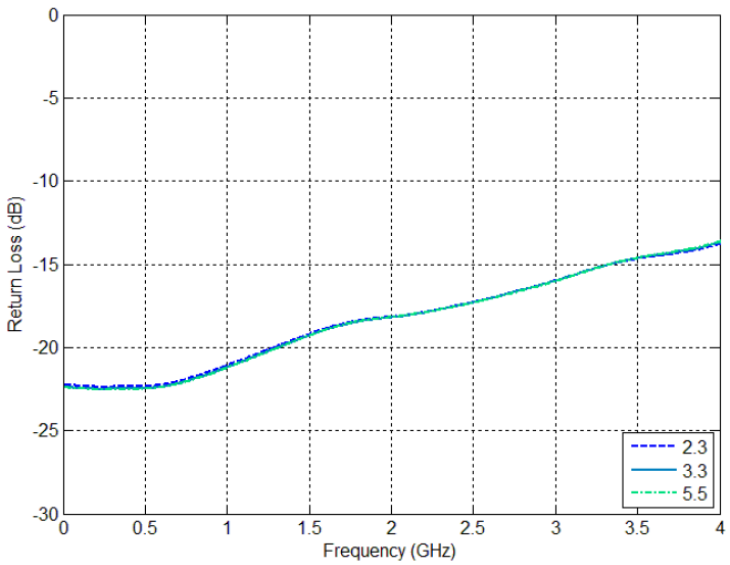


Figure 10. Active port return loss vs. V_{DD}

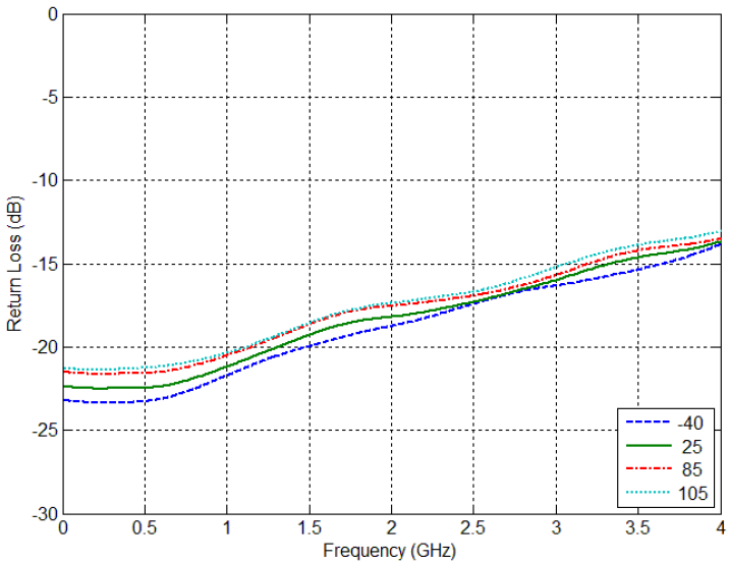


Figure 10. RFC port return loss vs. temperature

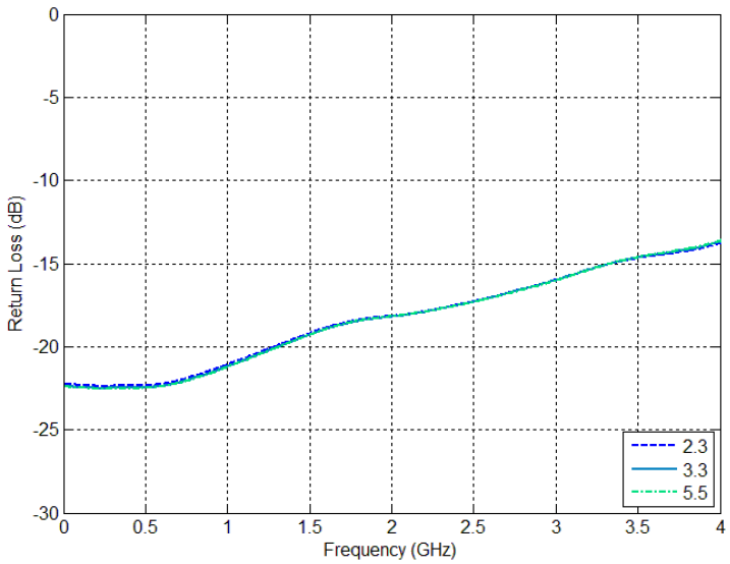


Figure 11. RFC port return loss vs. V_{DD}

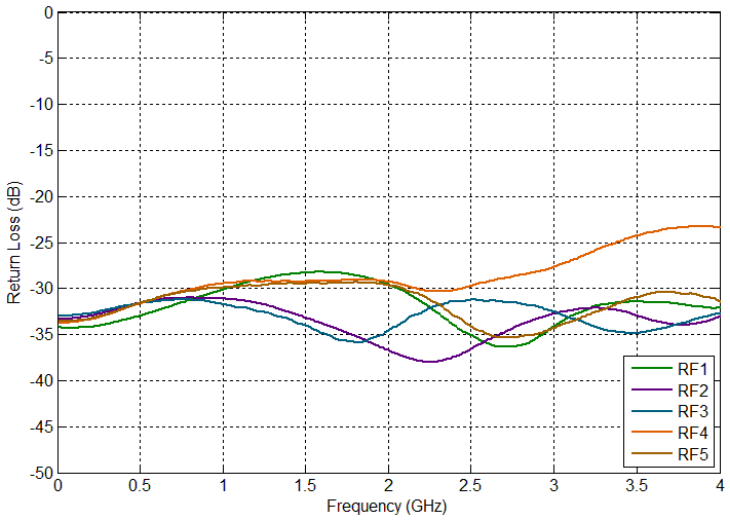


Figure 13. Return loss (all ports terminated)

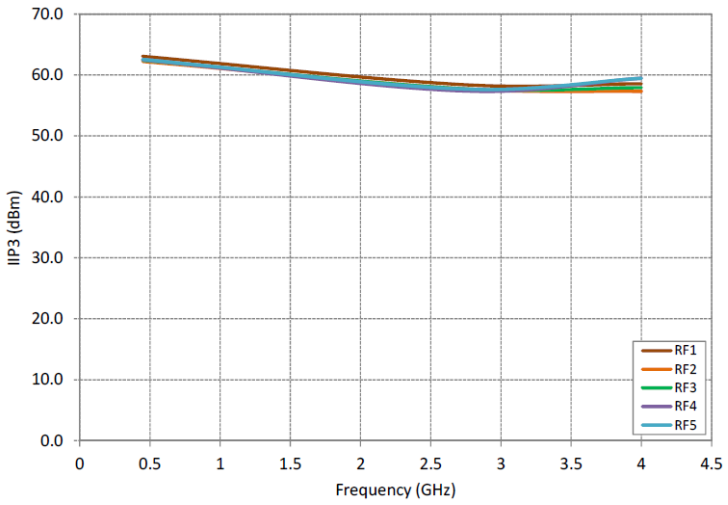


Figure 14. IIP3 vs. frequency

Evaluation kit

pSemi designed the SP5T switch evaluation board to ease your evaluation of the pSemi PE42452. The RF common port is connected through a 50Ω transmission line via the top SMA connector. RF1, RF2, RF3, RF4, and RF5 are connected through 50Ω transmission lines via side SMA connectors. A through 50Ω transmission is available via SMA connectors RFCAL1 and RFCAL2. You can use this transmission line to estimate the loss of the PCB over the environmental conditions being evaluated.

The EVK board is constructed with four metal layers on dielectric materials of Rogers 4003C and 4450 with a total thickness of 32 mils. Layer 1 and layer 3 provide ground for the 50Ω transmission lines. The 50Ω transmission lines are designed in layer 2 for high isolation purpose and use a stripline waveguide design with a trace width of 9.4 mils and trace metal thickness of 1.8 mils. The board stack up for 50Ω transmission lines has 8 mil thickness of Rogers 4003C between layer 1 and layer 2, and 10 mil thickness of Rogers 4450 between layer 2 and layer 3. See the manufacturer's guidelines for the proper board material properties in your application. The PCB must be designed so that RF transmission lines and sensitive DC I/O traces such as VSS_{EXT} are heavily isolated from one another, otherwise the true performance of the PE42452 will not be yielded.

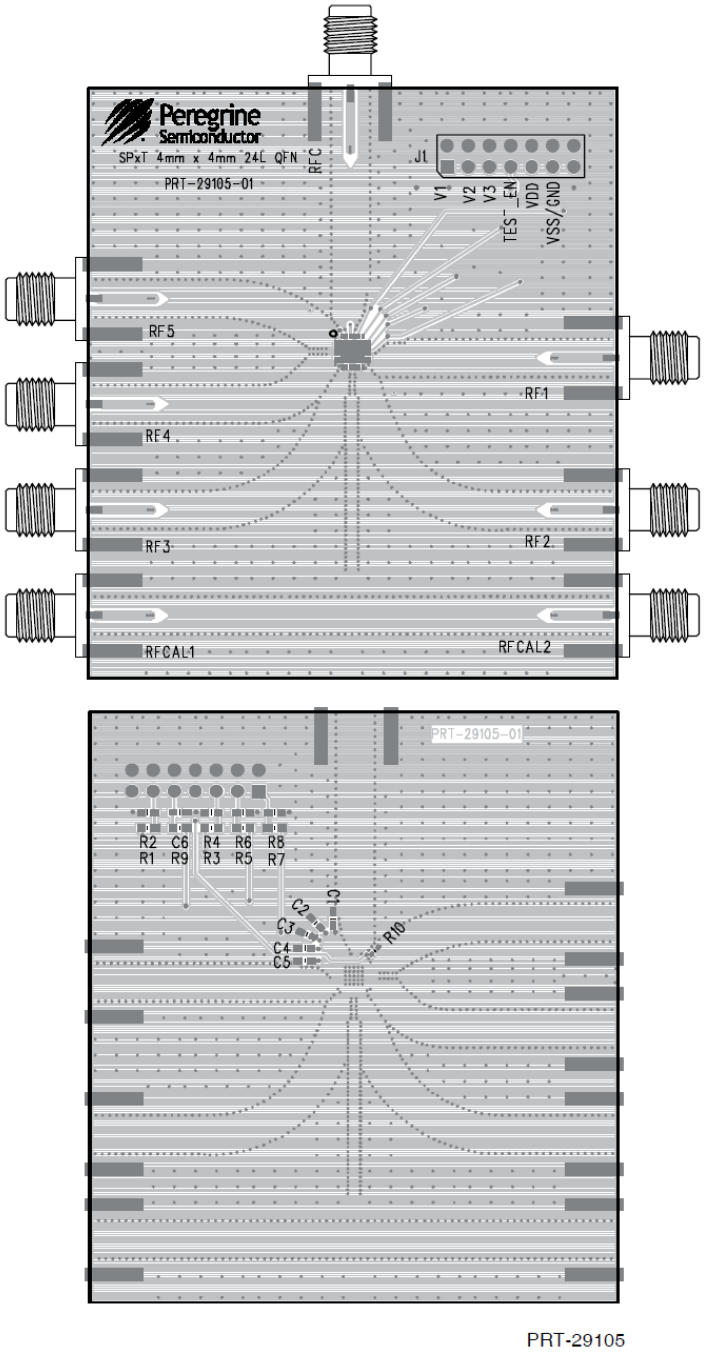


Figure 15. Evaluation board layouts

Evaluation board schematic

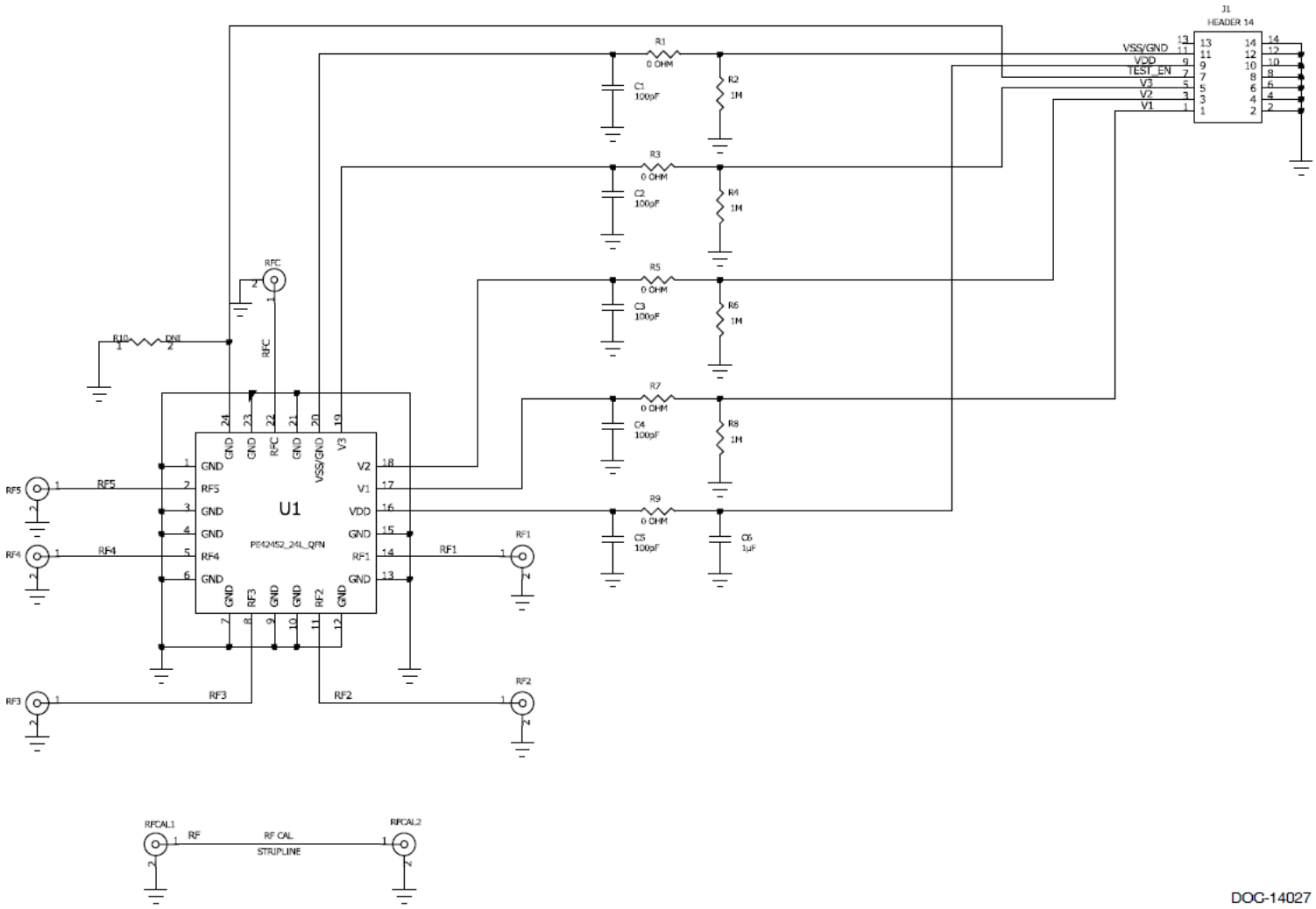


Figure 16. Evaluation board schematic

Pin information

Figure 17 shows the PE42452 pin map for the 24-lead 4 × 4 mm QFN package, and Table 5 lists the description for each pin.

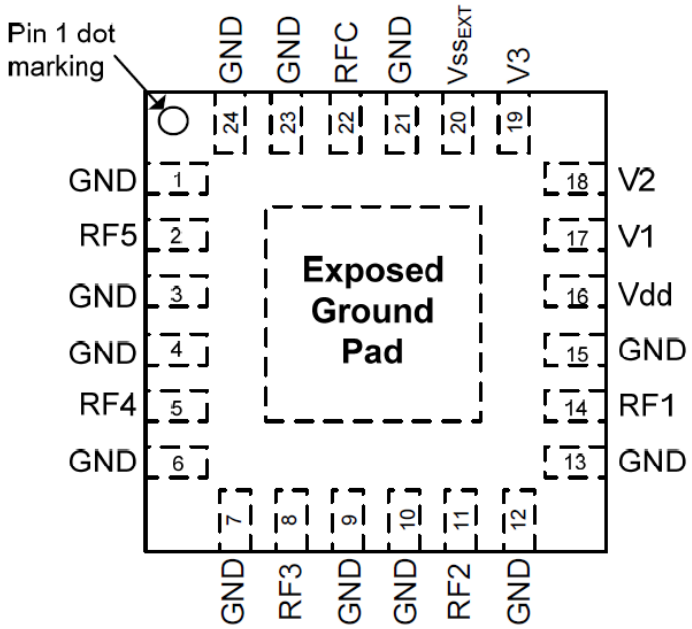


Figure 17. Pin configuration (top view)

Table 5. PE42452 pin descriptions

Pin no.	Pin name	Description
1	1, 3, 4, 6, 7, 9, 10, 12, 13, 15, 21, 23, 24	Ground
2[1]	RF5	RF port 5
5[1]	RF4	RF port 4
8[1]	RF3	RF port 3
11[1]	RF2	RF port 2
14[1]	RF1	RF port 1
16	V_{DD}	Supply voltage
17	V1	Digital control logic input 1
18	V2	Digital control logic input 2
19	V3	Digital control logic input 2
20[2]	VSS_{EXT}	External VSS negative voltage control/ground
22[1]	RFC	RF common
Pad	GND	Exposed pad. Ground for proper operation.

1. RF pins 2, 5, 8, 11, 14, and 22 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. To enable the internal negative voltage generator, connect pin 20 to GND. To bypass and disable the internal negative voltage generator, apply a negative voltage to VSS_{EXT} (pin 20). For more information, see Table 2.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE42452 moisture sensitivity level rating for the 24-lead 4 × 4 mm QFN package is MSL1.

Package drawing

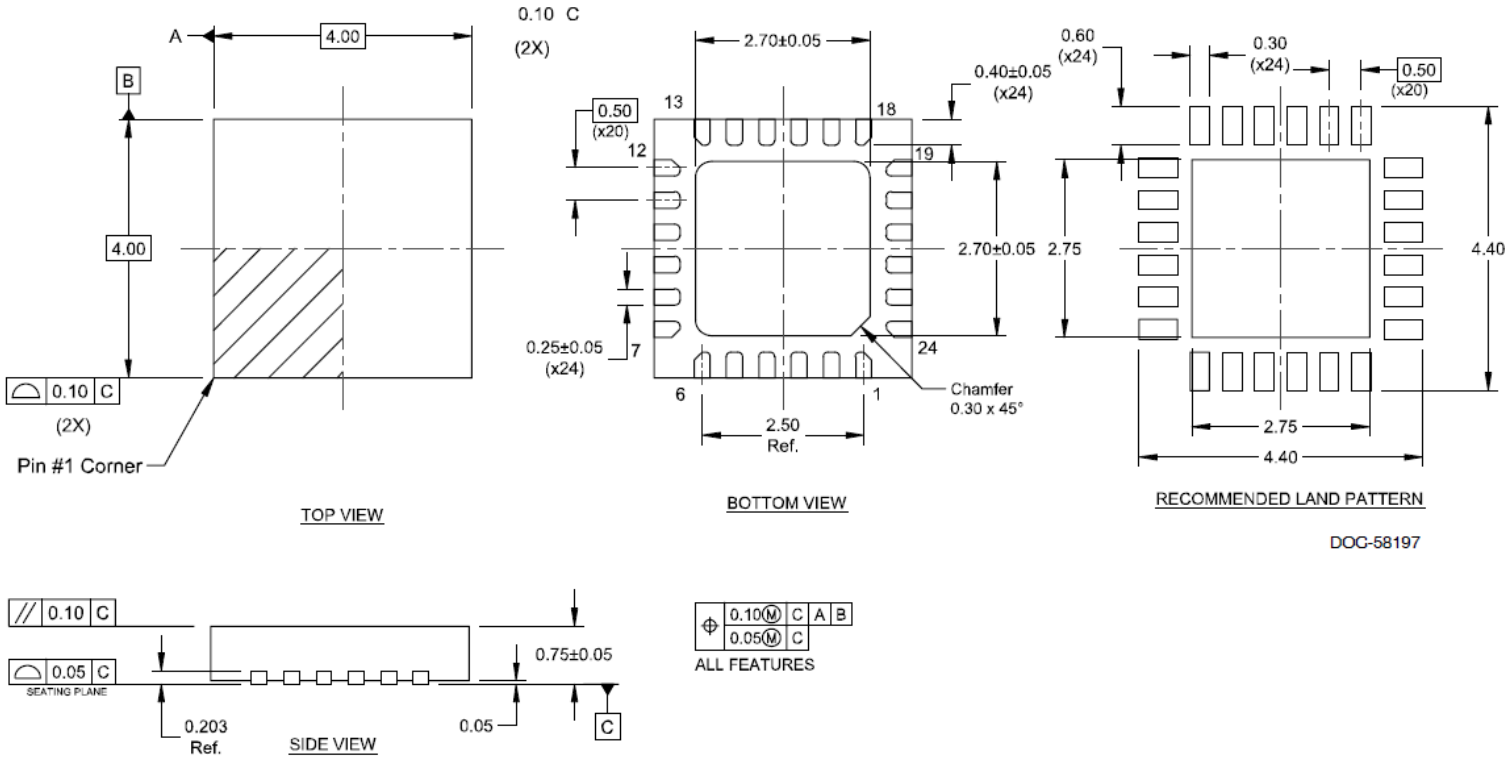
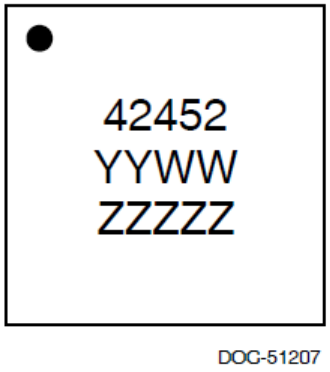


Figure 18. Package mechanical drawing for the 24-lead 4 × 4 mm QFN package

Top-marking specification



● = Pin 1 designator
YYWW = Date code
ZZZZZ = Las five digits of the lot number

Figure 19. PE42452 package marking specification

Tape and reel specification

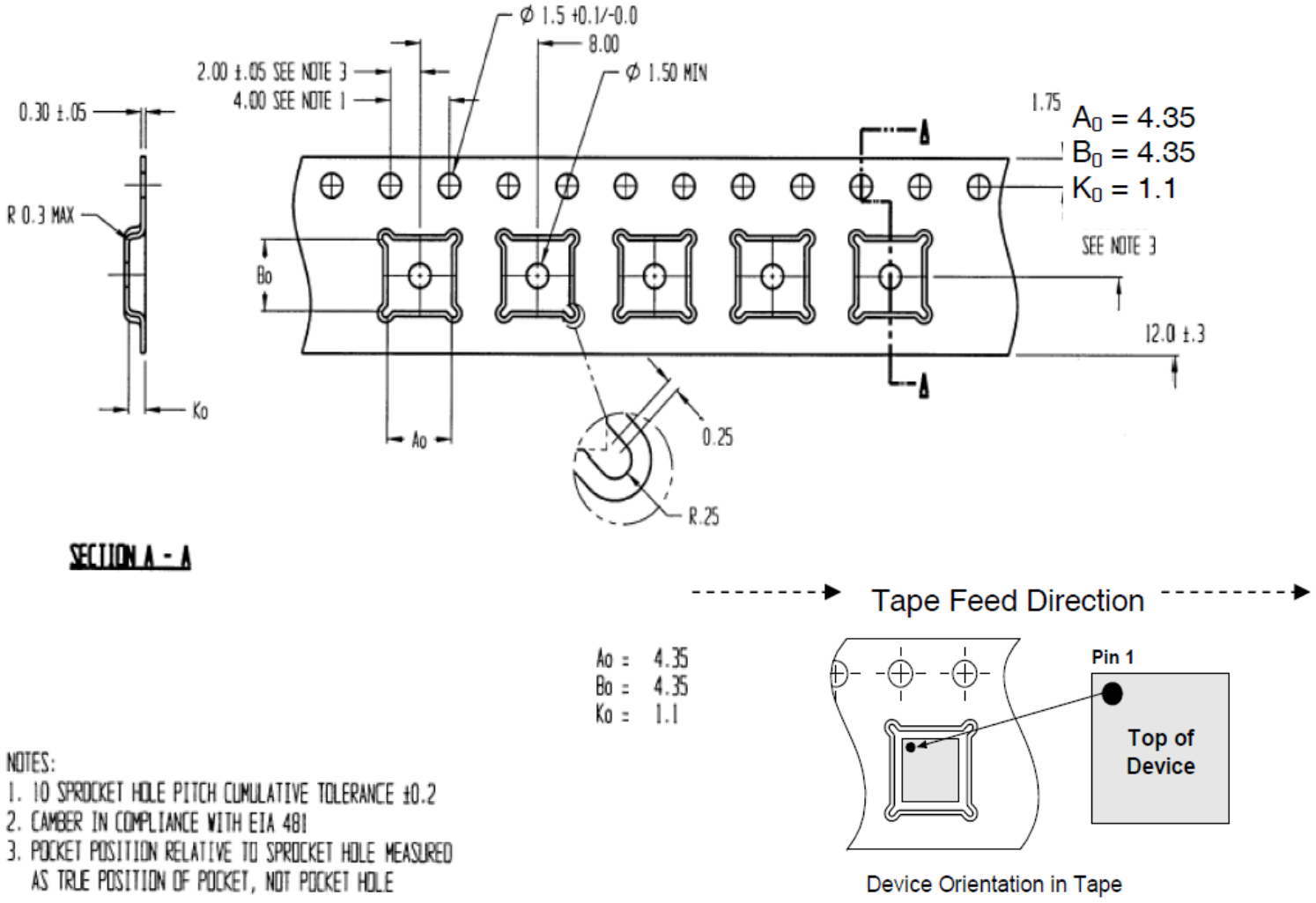


Figure 20. Tape and reel specification for the 24-lead 4 × 4 mm QFN package

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Ordering information

Order code	Description	Packaging	Shipping method
PE42452A-Z	PE42452 SP5T RF Switch	Green 24-lead 4 × 4 mm QFN	3000 units/T&R
EK42452-01	PE42452 Evaluation Kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
Product Specification	The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).
Product Brief	This document contains a shortened version of the data sheet. For the full data sheet, contact sales@psemi.com.

Contact and legal information

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