PE42421

Document category: Product Specification

UltraCMOS® SPDT RF Switch, 10–3000 MHz

Features

- Logic control inputs: Single-pin or complementary CMOS
- Low insertion loss:
  - 0.35 dB @ 1000 MHz
  - 0.5 dB @ 2000 MHz
- Isolation:
  - 30 dB @ 1000 MHz
  - 20 dB @ 2000 MHz
- Input 1 dB compression point: +33.5 dBm (typical)
- Minimum power supply voltage: 1.8V
- Packaging: 6-lead SC-70

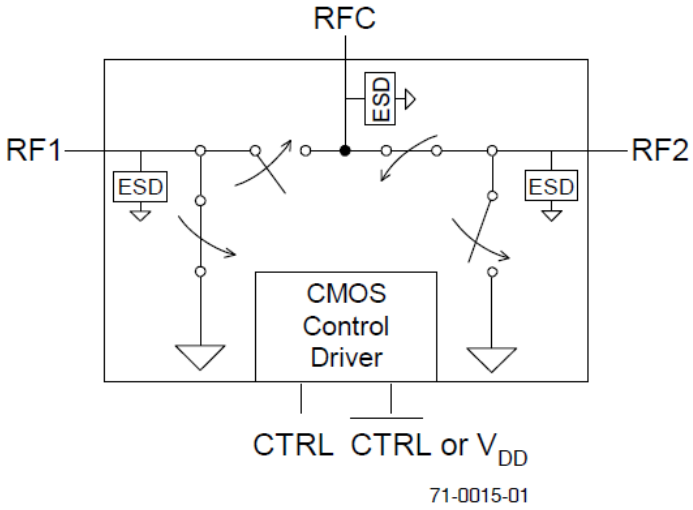

Figure 1. PE42421 functional block diagram

Product description

pSemi designed the PE42421 UltraCMOS® RF switch to cover a broad range of applications from 10 MHz through 3000 MHz. This reflective switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface which can be controlled using single-pin or complementary-pin control inputs. By using a nominal +3V power supply voltage, a typical input 1 dB compression point of +33.5 dBm can be achieved.

pSemi manufactured the PE42421 SPDT RF switch using the pSemi UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

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Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE42421 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Power supply voltage	V_{DD}	-0.3	4.0	V
Voltage on any DC input	V_I	-0.3	V_{DD} + 0.3	V
Storage temperature range	T_{ST}	-65	150	°C
Operating temperature range	T_{OP}	-40	85	°C
Input power (50Ω)[1]	P_{IN}	–	+34	dBm
ESD voltage HBM[2]	V_{ESD}	–	2000	V
ESD voltage MM[3]		–	100	V

1. To maintain the optimum system performance, do not exceed the maximum input power (P_{IN}) at the preferred operating frequency, as shown in Figure 2.
2. Human Body Model (MIL-STD-883 Method 3015.7).
3. Machine Model (JEDEC JESD22-A114-B).

Recommended operating conditions

Table 2 lists the PE42421 recommending operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE42421 operating conditions

Parameter	Min	Typ	Max	Unit
V_{DD} power supply voltage	1.8	3.0	3.3	V
I_{DD} power supply current (V_{DD} = 3V, V_{CTRL} = 3V)	–	9	20	µA
Control voltage high	0.7 × V_{DD}	–	–	V
Control voltage low	–	–	0.3 × V_{DD}	V

Electrical specifications

Table 3 lists the PE42421 key electrical specifications at +25 °C and V_{DD} = 3V (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3. PE42421 electrical specifications

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency(1)	–	10	–	3000	MHz
Insertion loss(2)	1000 MHz 2000 MHz	–	0.35 0.50	0.45 0.60	dB
Isolation	1000 MHz 2000 MHz	29 19	30 20	–	dB
Return loss(2)	1000 MHz 2000 MHz	21 24	22 27	–	dB
ON switching time	50% CTRL to 0.1 dB of final value, 1 GHz	–	1.50	–	µs
OFF switching time	50% CTRL to 25-dB isolation, 1 GHz	–	1.50	–	µs
Video feedthrough(3)	–	–	15	–	mV_{P-P}
Input 1 dB compression	1000 MHz @ 1.8–2.3V 1000 MHz @ 2.3–3.3V 2500 MHz @ 1.8–2.3V 2500 MHz @ 2.3–3.3V	29.5 31.5 28 28.5	30.5 33.5 29 30.5	–	dBm
Input IP3	1000 MHz, 20 dBm input power	–	55	–	dBm
Switching rate	–	–	–	25	kHz

1. The device linearity begins to degrade below 10 MHz.
2. To optimize the insertion loss and return loss performance, add a tuning capacitor to the application board, as shown in Figure 12.
3. The DC transient at the output of any port of the switch when the control voltage is switched from low-to-high or high-to-low in a 50Ω test setup, measured with 1 ns risetime pulses and a 500 MHz bandwidth.

SPDT control logic

Table 4. Single-pin control logic truth table

Control voltages	Signal path
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = High	RFC to RF2
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = Low	RFC to RF1

Table 5. Complementary-pin control logic truth table

Control voltages	Signal path
Pin 6 (~~CTRL~~ or V_{DD}) = low Pin 4 (CTRL) = high	RFC to RF2
Pin 6 (~~CTRL~~ or V_{DD}) = high Pin 4 (CTRL) = low	RFC to RF1

The PE42421 is a versatile RF CMOS switch with two operating control modes: *single-pin control mode* and *complementary-pin control mode*.

- *Single-pin control mode* enables the switch to operate with a single control pin (pin 4) supporting a +3V CMOS logic input and requires a dedicated +3V power supply connection on pin 6 (V_{DD}). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS microprocessor I/O port.
- *Complementary-pin control mode* allows the switch to operate using complementary control pins CTRL and ~~CTRL~~ (pins 4 and 6, respectively), that can be directly driven by +3V CMOS logic or a suitable microprocessor I/O port. This enables the PE42421 to serve as a potential alternate source for SPDT RF switch products used in positive control voltage mode and operating within the PE42421 operational limits.

Power de-rating curve

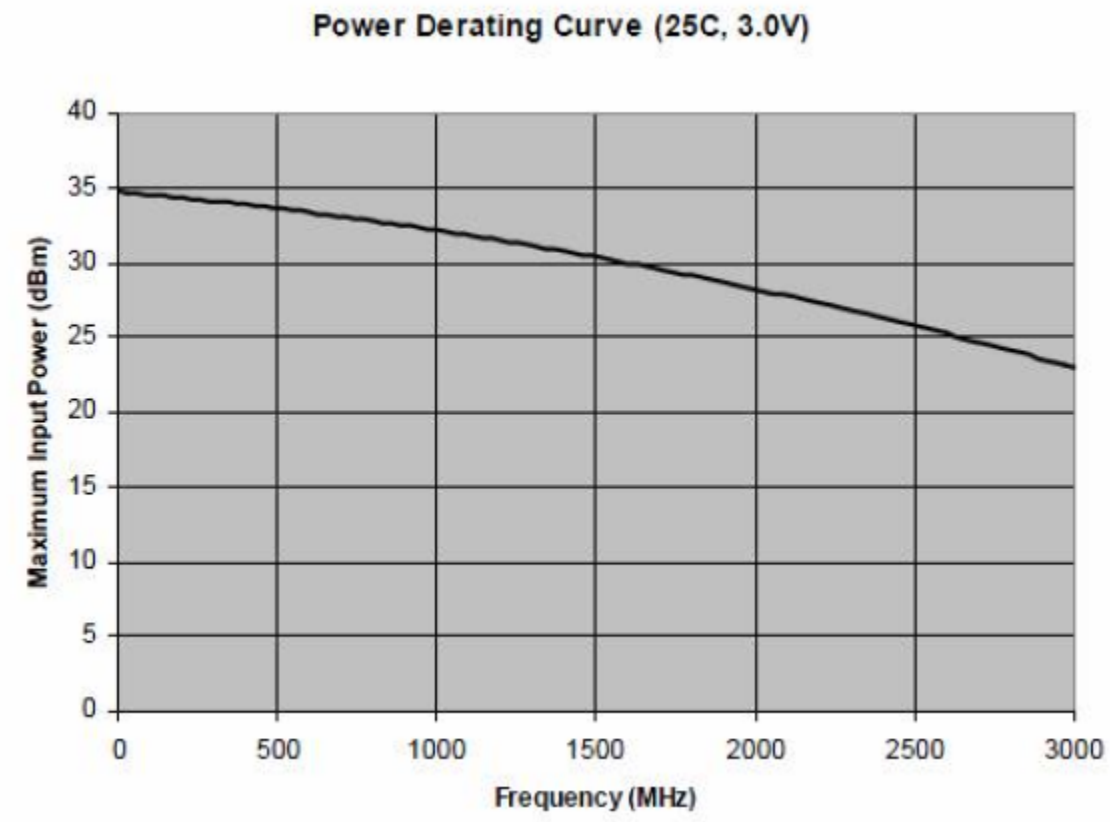

Figure 2. PE42421 power de-rating curve

Typical performance data

Figure 3–Figure 6 show the typical performance data at -40 °C to +85 °C, unless otherwise specified.

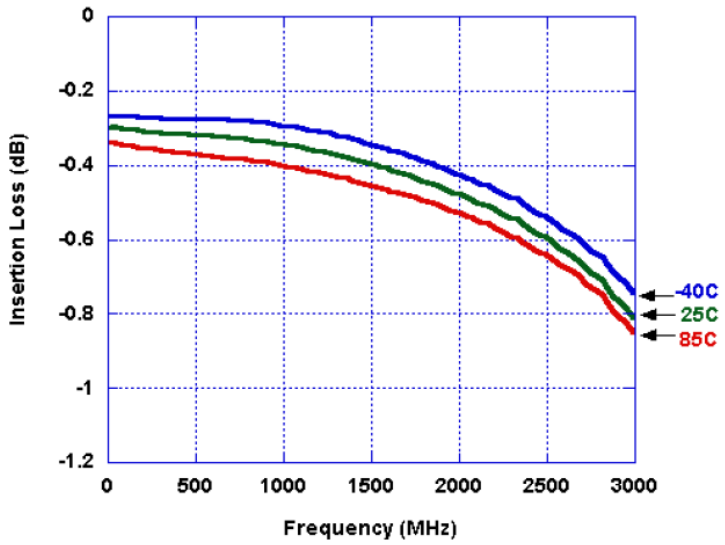

Figure 3. Insertion loss

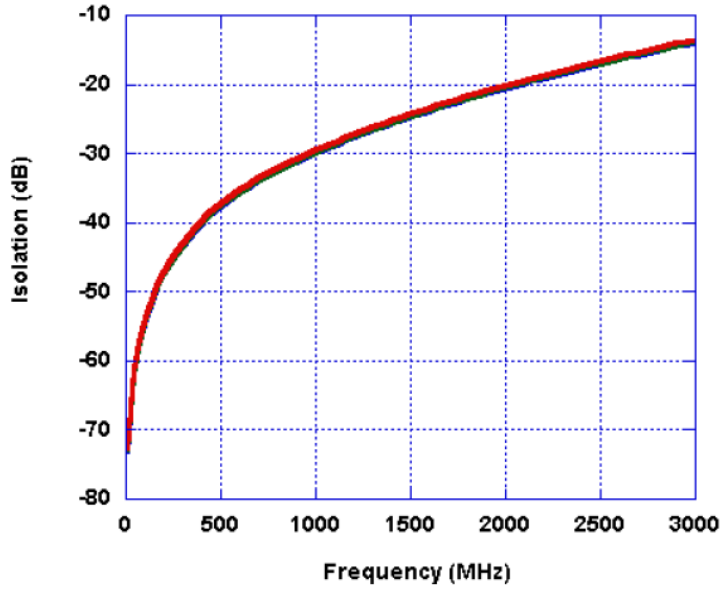

Figure 4. Isolation: Input to output

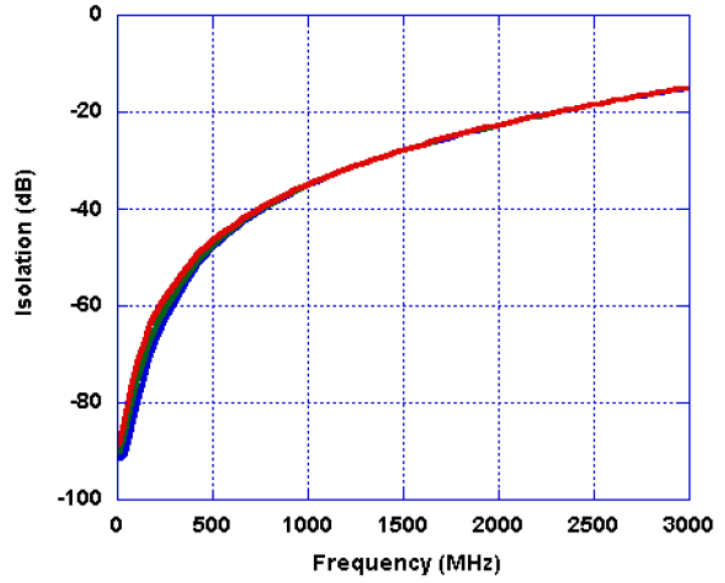

Figure 5. Isolation: Output to output

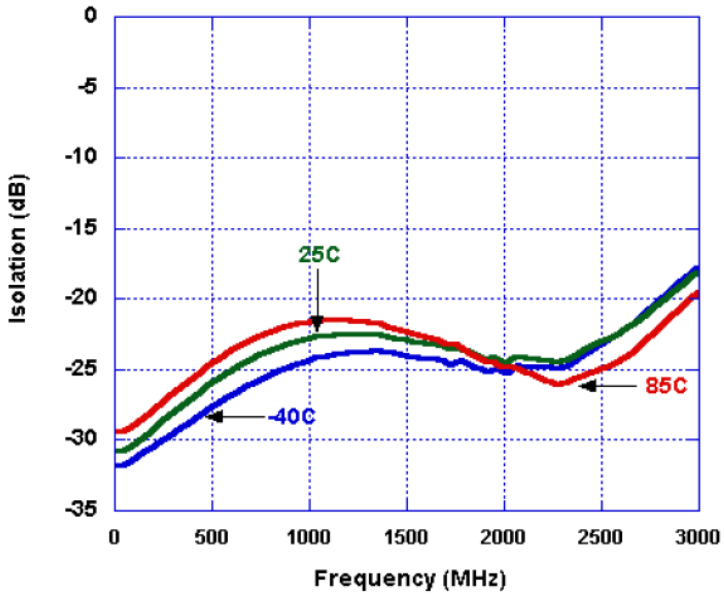

Figure 6. Return loss: Input

Figure 7–Figure 10 show the typical performance data at +25 °C and V_{DD} = 2.3V, unless otherwise specified.

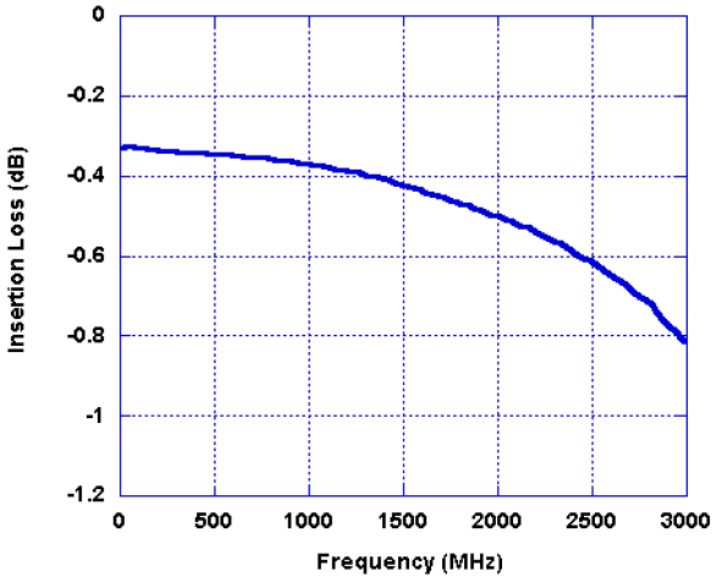

Figure 7. Insertion loss

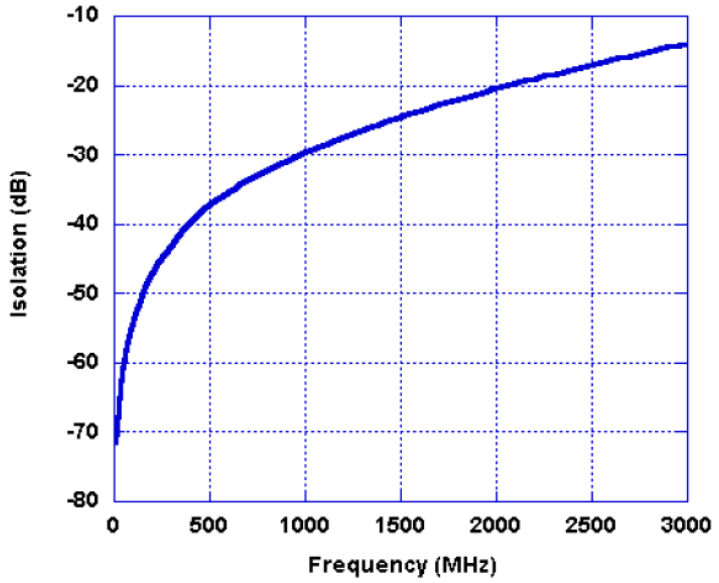

Figure 8. Isolation: Input to output

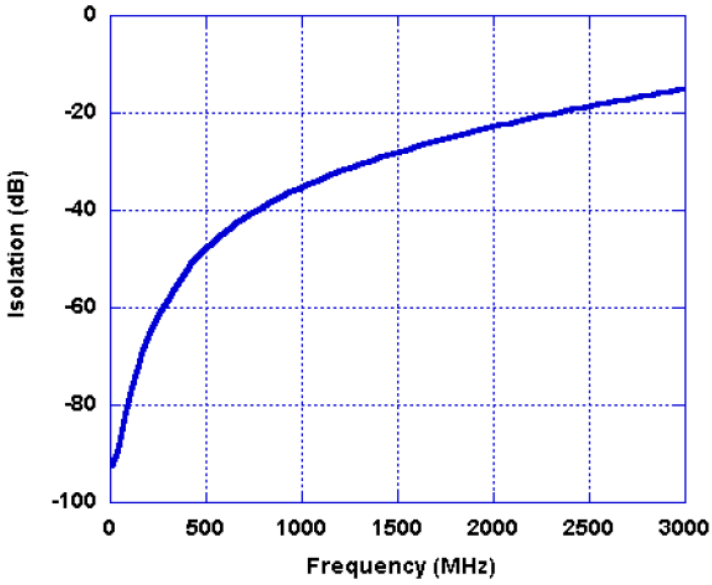

Figure 9. Isolation: Output to output

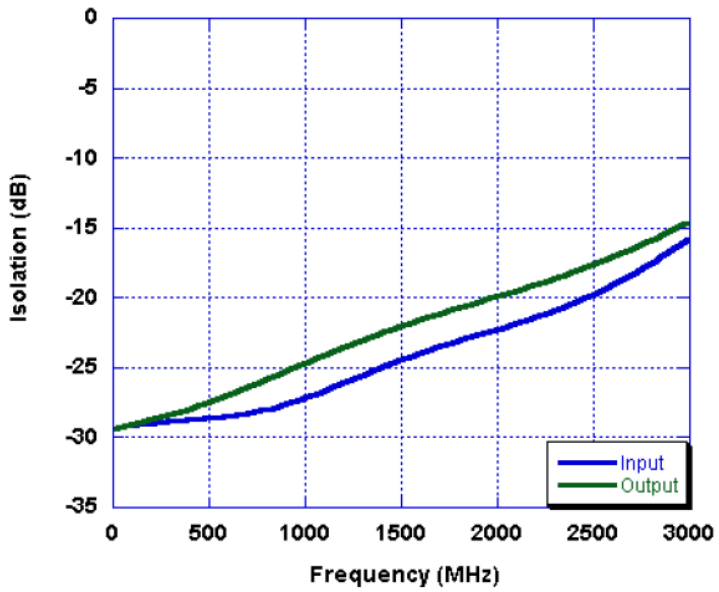

Figure 10. Return loss: Input and output

Evaluation kit

pSemi designed the SPDT switch evaluation board to ease your evaluation of the PE42421. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1 and RF2 are connected through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A through 50Ω transmission is available via SMA connectors J4 and J5. Use this transmission line to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two-layer metal FR4 material with a total thickness of 0.031". The bottom layer provides the ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021", and εr of 4.4.

J6 and J7 provide the means for controlling the DC and digital inputs to the device. J6-1 is connected to the device V_{DD} or ~~CTRL~~ input (pin 6). J7-1 is connected to the device CTRL input (pin 4).

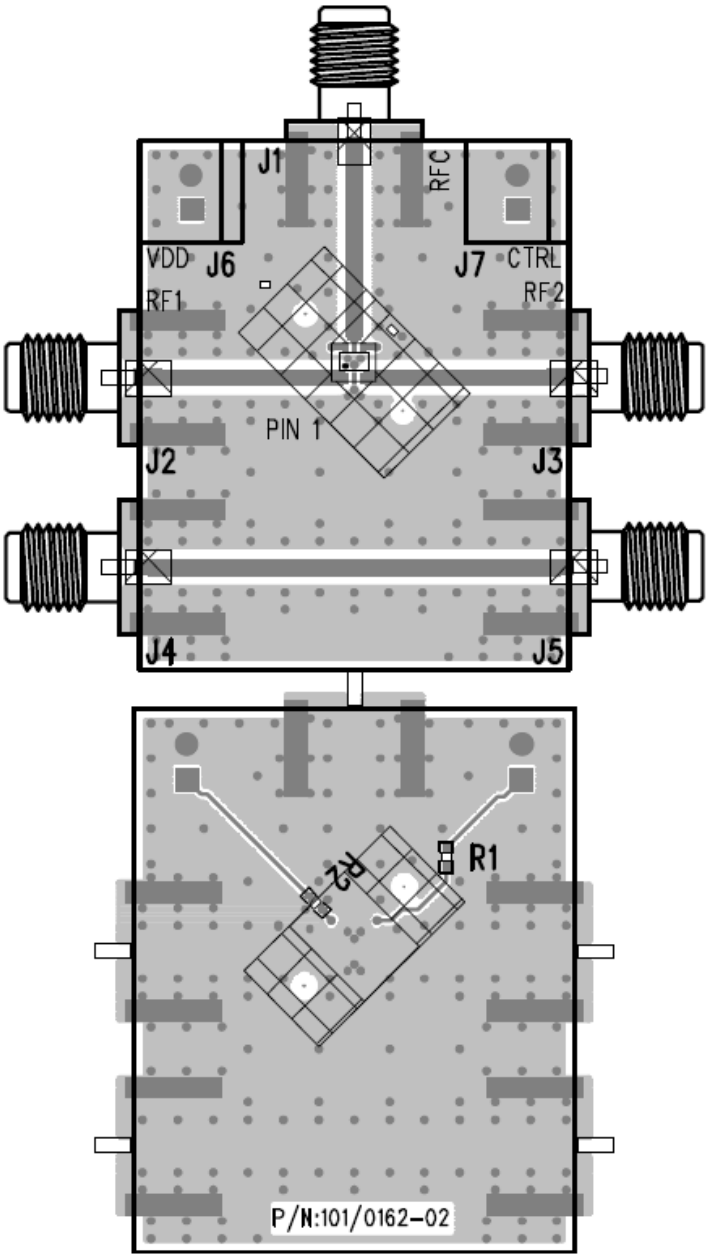

Figure 11. Evaluation board layouts

Evaluation board schematic

The pSemi evaluation board part number is 102-0756-01.

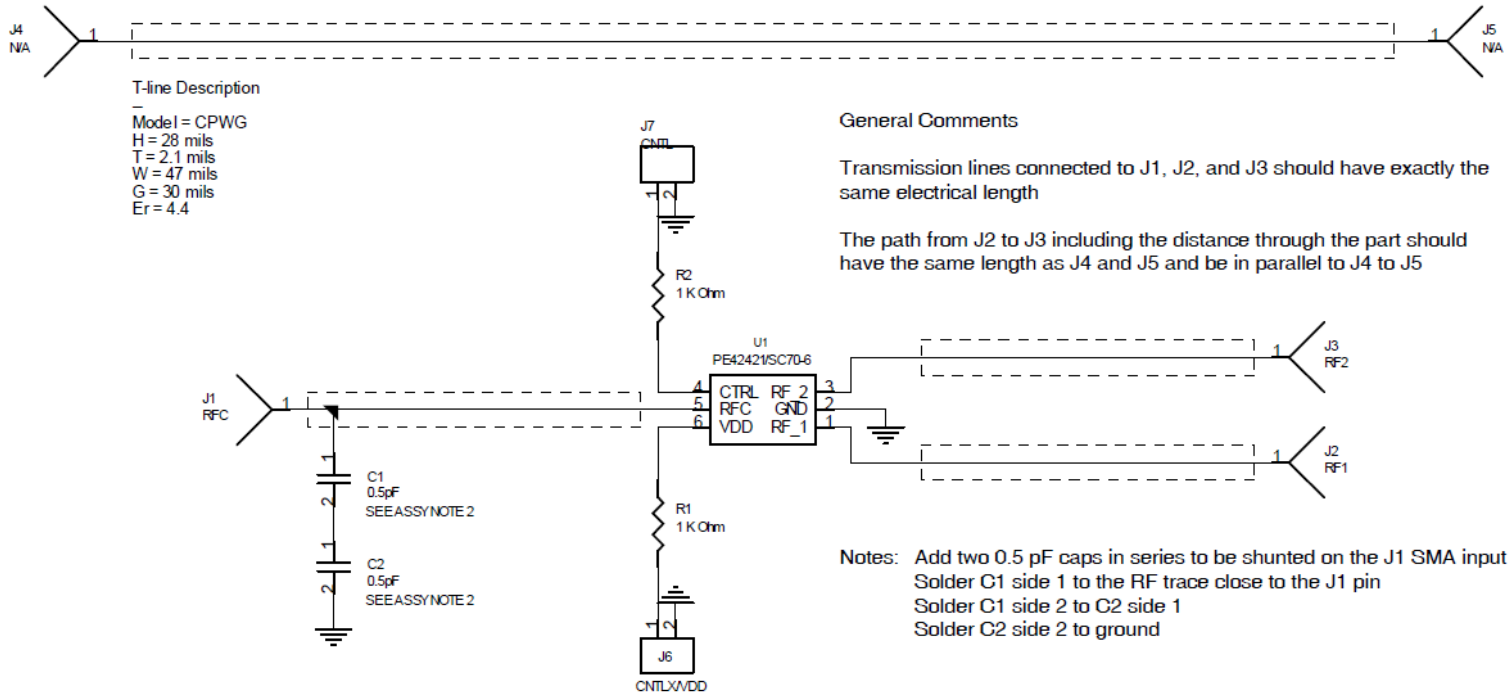

Figure 12. Evaluation board schematic

Pin information

Figure 13 shows the PE42421 pin map for the 6-led SC-70 package, and Table 6 lists the description for each pin.

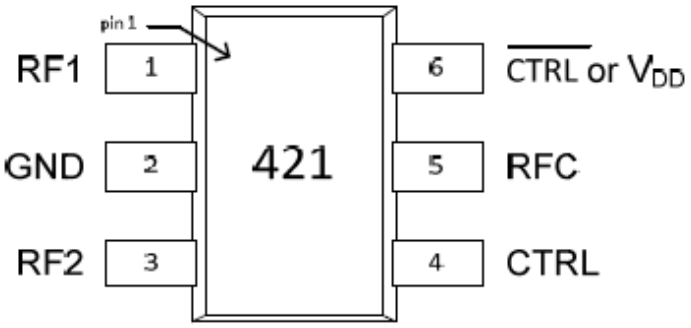

Figure 13. Pin configuration (top view)

Table 6. PE42421 pin descriptions

Pin	Pin name	Description
1(*)	RF1	RF port 1
2	GND	Ground connection. For the best performance, traces must be physically short and connected to the ground plane.
3(*)	RF2	RF port 2
4	CTRL	Switch control input, CMOS logic level
5(*)	RFC	RF common
6	~~CTRL~~ or V_{DD}	This pin supports two interface options: • *Single-pin control mode*: A nominal 3V supply connection is required. • *Complementary-pin control mode*: A complementary CMOS control signal to CTRL is supplied to this pin. Bypassing on this pin is not required in this mode.

* RF pins 1, 3, and 5 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE42421 moisture sensitivity level rating for the 6-led SC-70 package is MSL1.

Package drawing

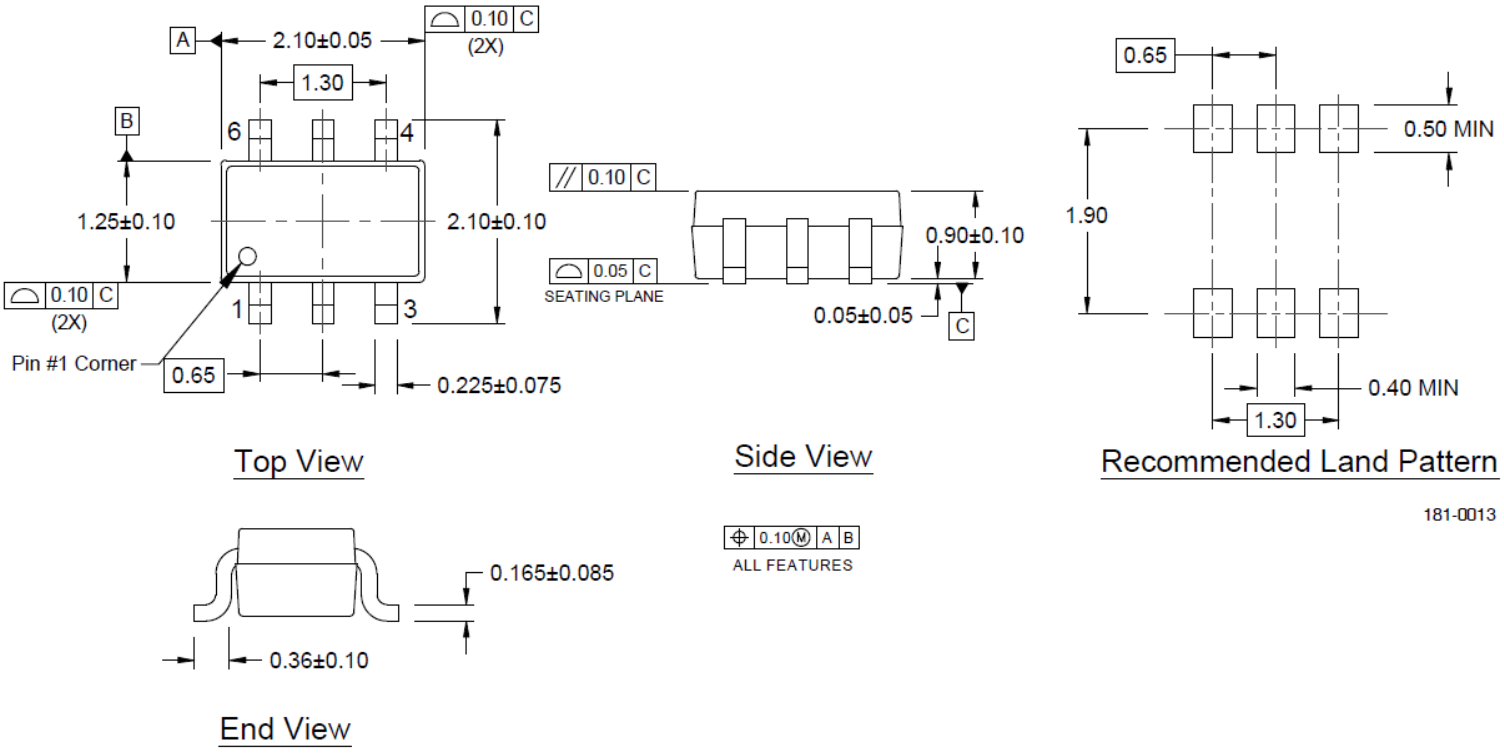

Figure 14. Package mechanical drawing for the 6-led SC-70 package

Top-marking specification

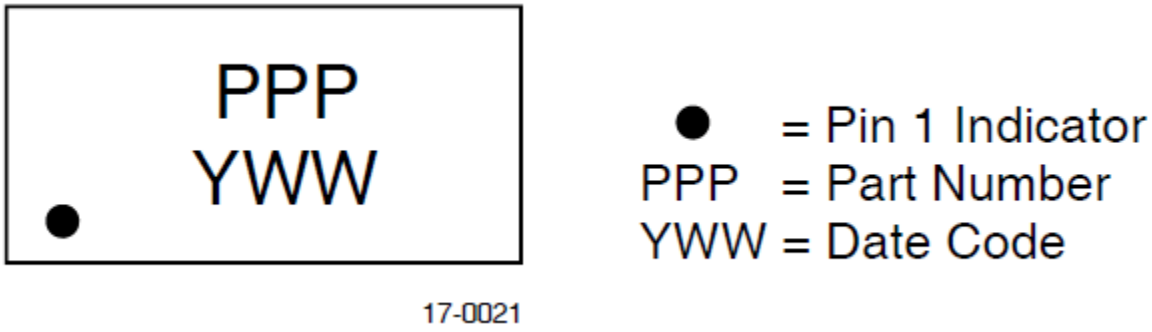

Figure 15. PE42421 package marking specification

Tape and reel specification

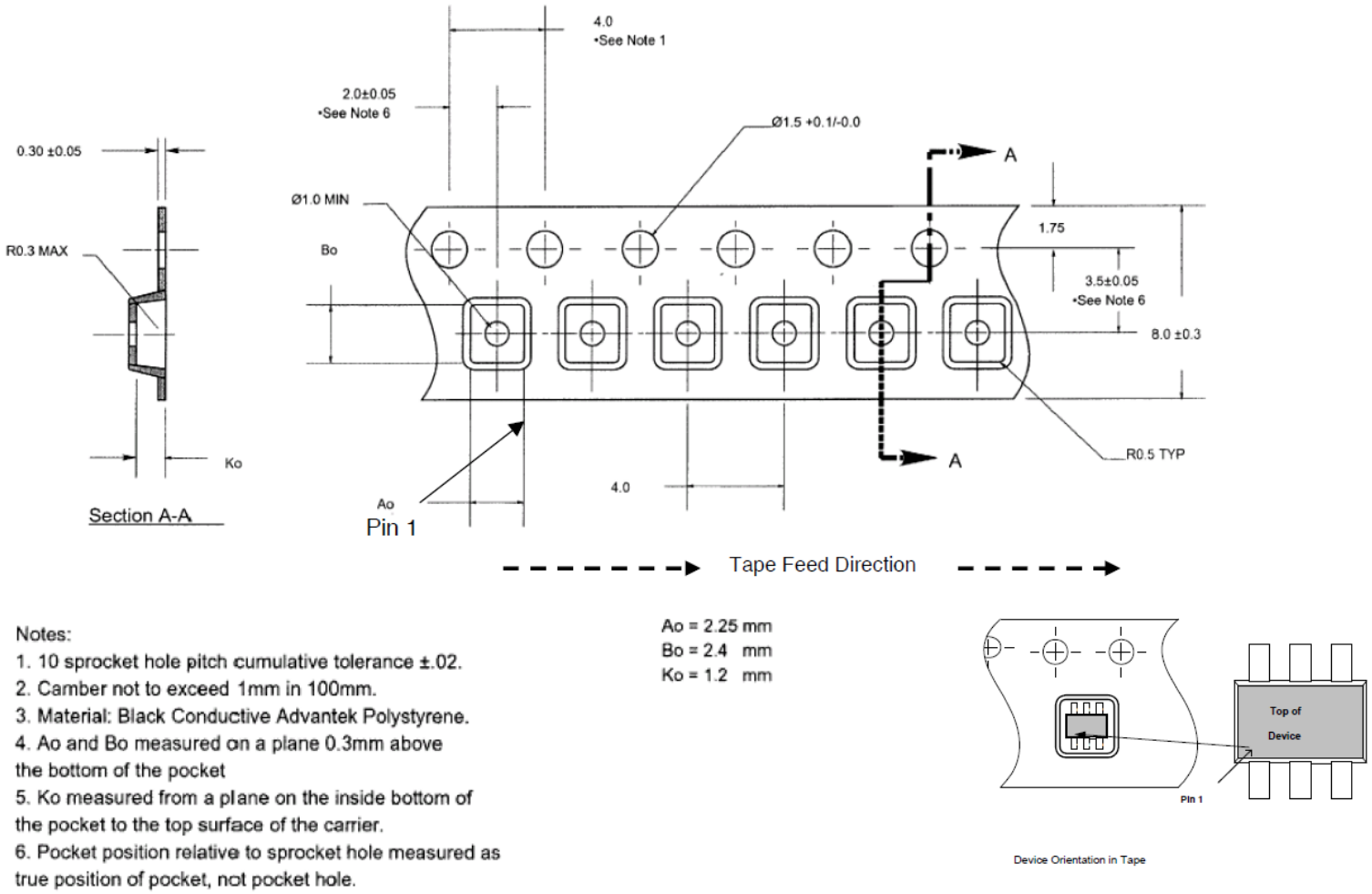

Figure 16. Tape and reel specification for the 6-led SC-70 package

Notes:

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Ordering information

Order code	Description	Packaging	Shipping method
PE42421SCAA-Z	PE42421 SPDT RF switch	Green 6-led SC-70	3000 units/T&R
EK42421-01	PE42421 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
Product Specification	The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).
Product Brief	This document contains a shortened version of the data sheet. For the full data sheet, contact sales@psemi.com.

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