

Product Specification

PE3502

3500 MHz Low Power UltraCMOS™ Divide-by-4 Prescaler

Features

- High-frequency operation: 1500 MHz to 3500 MHz
- · Fixed divide ratio of 4
- Low-power operation: 12 mA typical @ 3 V across frequency
- Small package: 8-lead MSOP

Product Description

The PE3502 is a high performance monolithic UltraCMOS™ prescaler with a fixed divide ratio of 4. Its operating frequency range is 1500 MHz to 3500 MHz. The PE3502 operates on a nominal 3 V supply and draws only 12 mA. It is packaged in a small 8-lead MSOP and is ideal for microwave PLL synthesis solutions.

The PE3502 is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi©) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram

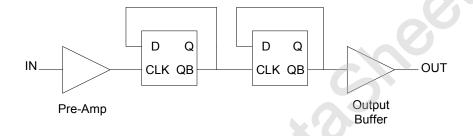


Figure 2. Package Type 8-lead MSOP



Table 1. Electrical Specifications $(Z_s = Z_L = 50 \Omega)$

 $V_{DD} = 3.0 \text{ V}$, $-40^{\circ} \text{ C} \leq T_A \leq 85^{\circ} \text{ C}$, unless otherwise specified

Parameter		Minimum	Typical	Maximum	Units
Supply Voltage		2.85	3.0	3.15	V
Supply Current			12	17	mA
Input Frequency (FIN)		1500		3500	MHz
Input Power (PIN)	1500 MHz ≤ F _{in} ≤ 3200 MHz	-10		+5	dBm
	3200 MHz < F _{in} ≤ 3500 MHz	0		+5	dBm
Output Power		-5			dBm
				Datashe	



Figure 3. Pin Configuration (Top View)

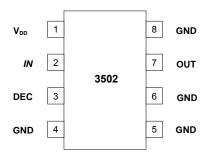


Table 2. Pin Descriptions

•				
Pin No.	Pin Name	Description		
1	V_{DD}	Power supply pin. Bypassing is required.		
2	IN	Input signal pin. Should be coupled with a capacitor (eg 15 pF)		
3	DEC	Power supply decoupling pin. Place a capacitor as close as possible and connect directly to the ground plane (eg 10 nF and 10 pF).		
4	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.		
5	GND	Ground pin.		
6	GND	Ground pin.		
7	OUT	Divided frequency output pin. This pin should be coupled with a capacitor (eg 100 pF).		
8	GND	Ground pin.		

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage		4.0	V
T _{ST}	Storage temperature range	-65	150	°C
T_OP	Operating temperature range	-40	85	°C
V _{ESD}	ESD voltage (Human Body Model)	250		V
P _{INMAX}	Maximum input power		10	dBm

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Device Functional Considerations

The PE3502 takes an input signal frequency from 1500 MHz to 3500 MHz and produces an output signal frequency one-fourth that of the supplied input. In order for the prescaler to work properly, several conditions need to be adhered to. It is crucial that pin 3 be supplied with a bypass capacitor to ground. In addition, the input and output signals (pins 2 & 7, respectively) need to be AC coupled via an external capacitor as shown in the test circuit in Figure 7.

The ground pattern on the board should be made as wide as possible to minimize ground impedance.



Typical Performance Data

Figure 4. Input Sensitivity

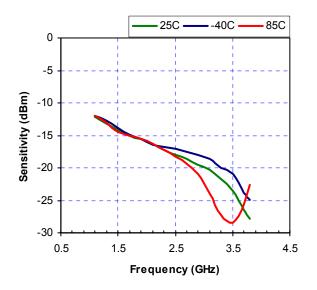


Figure 5. Device Current

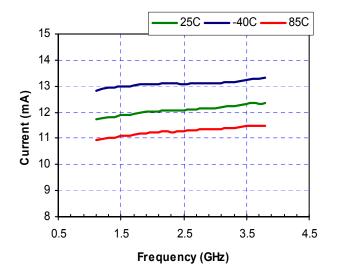


Figure 6. Output Power

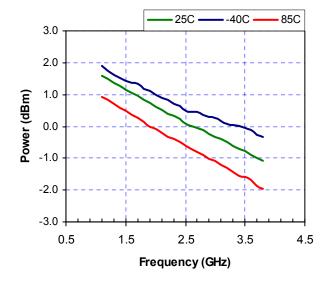




Figure 7. Test Circuit Block Diagram

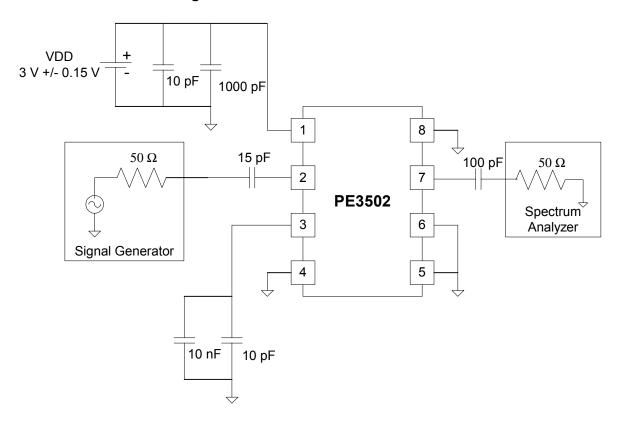
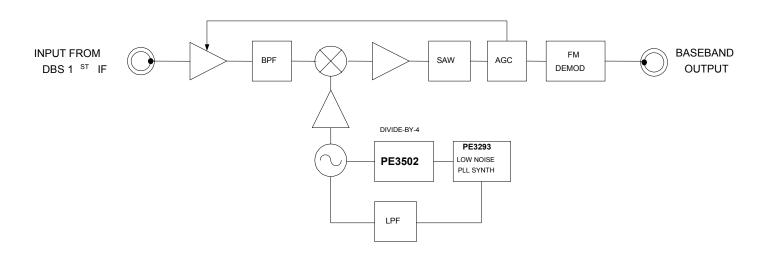


Figure 8. High Frequency System Application

The wideband frequency of operation of the PE3502 makes it an ideal part for use in a DBS downconverter system.





Evaluation Kit

Evaluation Kit Operation

The MSOP Prescaler Evaluation Board was designed to help customers evaluate the PE3502 Divide-by-4 Prescaler. On this board, the device input (pin 2) is connected to connector J1 through a 50 Ω transmission line. A series capacitor (C3) provides the necessary DC block for the device input. It is important to note that the value of this capacitance will impact the performance of the device. A value of 15 pF was found to be optimal for this board layout; other applications may require a different value.

The device output (pin 7) is connected to connector J3 through a 50 Ω transmission line. A series capacitor (C1) provides the necessary DC block for the device output. Note that this capacitor must be chosen to have a low impedance at the desired output frequency the device. The value of 100 pF was chosen to provide a wide operating range for the evaluation board.

The board is constructed of a two-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide above ground plane model with trace width of 0.030", trace gaps of 0.007", dielectric thickness of 0.028", metal thickness of 0.0014" and ϵ_r of 4.4. Note that the predominate mode for these transmission lines is coplanar waveguide. J2 provides DC power to the device. Starting from the lower left pin, the second pin to the right (J2-3) is connected to the device V_{DD} pin (1). Two decoupling capacitors (10 pF, 1000 pF) are included on this trace. It is the responsibility of the

customer to determine proper supply decoupling for their design application.

The DEC pin (3) must be connected to a low impedance AC ground for proper device operation. On the board, two decoupling capacitors (C6 = 10 nF, C4 = 10 pF), located on the back of the board, perform this function.

Applications Support

If you have a problem with your evaluation kit or if you have applications questions call (858) 731-9400 and ask for applications support. You may also contact us by fax or e-mail:

Fax: (858) 731-9499 E-Mail: help@psemi.com

Figure 9. Evaluation Board Layouts

Peregrine Specification 101/0035

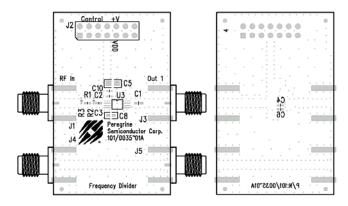


Figure 10. Evaluation Board Schematic

Peregrine Specification 102/0055

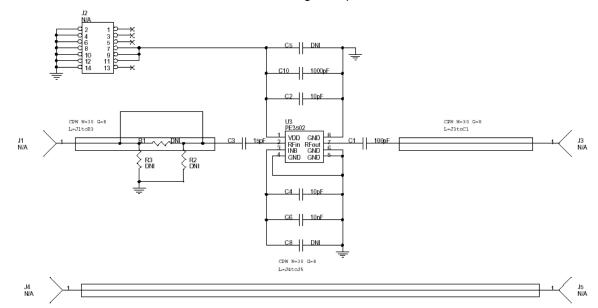




Figure 11. Package Drawing

8-lead MSOP

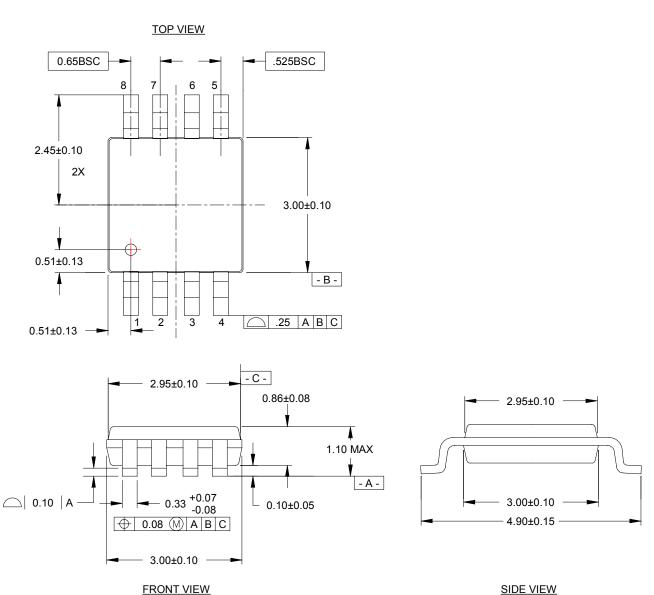


Table 4. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
3502-21	3502	PE3502-08MSOP-50A	8-lead MSOP	50 units / Tube
3502-22	3502	PE3502-08MSOP-2000C	8-lead MSOP	2000 units / T&R
3502-00	PE3502-EK	PE3502-08MSOP-EK	Evaluation Kit	1 / Box
3502-51	3502	PE3502G-08MSOP-50A	Green 8-lead MSOP	50 units / Tube
3502-52	3502	PE3502G-08MSOP-2000C	Green 8-lead MSOP	2000 units / T&R



Sales Offices

The Americas

Peregrine Semiconductor Corp.

9450 Carroll Park Drive San Diego, CA 92121 Tel 858-731-9400 Fax 858-731-9499

Europe

Peregrine Semiconductor Europe

Commercial Products:

Bâtiment Maine 13-15 rue des Quatre Vents F- 92380 Garches, France Tel: +33-1-47-41-91-73

Fax: +33-1-47-41-91-73

Space and Defense Products:

180 Rue Jean de Guiramand 13852 Aix-En-Provence cedex 3, France

Tel: +33(0) 4 4239 3361 Fax: +33(0) 4 4239 7227

North Asia Pacific

Peregrine Semiconductor K.K.

5A-5, 5F Imperial Tower 1-1-1 Uchisaiwaicho, Chiyoda-ku Tokyo 100-0011 Japan

Tel: +81-3-3502-5211 Fax: +81-3-3502-5213

South Asia Pacific

Peregrine Semiconductor

28G, Times Square, No. 500 Zhangyang Road, Shanghai, 200122, P.R. China

Tel: +86-21-5836-8276 Fax: +86-21-5836-7652

For a list of representatives in your area, please refer to our Web site at: www.psemi.com

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS is a trademark of Peregrine Semiconductor Corp.