PE24111

Document Category: Product Specification

3.3 VIN, 20A, Two-stage Buck Regulator for Low Output Voltage Applications

General Description

The PE24111 is a compact, low-profile, and ultra-high efficiency step-down DC-DC converter solution capable of delivering 20A output current from an input voltage range from 3.0–3.6V. The output voltage is set between 0.35V and 0.7V with external feedback resistors and can be adjusted by an external AVS DAC.

Based on pSemi advanced two-stage architecture, the PE24111 consists of a two-phase interleaved charge pump followed by an interleaved buck regulator stage. This power system greatly reduces the inductance necessary for high efficiency while maintaining a small solution size for small-footprint and height-constrained applications.

Features

- Proprietary architecture enabling industry-leading efficiency with ultra-low profile and footprint
- 90% peak efficiency
- Wide input voltage range, from 3.0–3.6V, that supports running off a nominal 3.3V bus supply
- Output voltage regulation accuracy better than ±1% for all line and load variations
- Output voltage set by external feedback resistors
- Output can be adjusted by an external AVS DAC
- External sync pin allows synchronization to an external clock
- Parallel up to three devices

Applications

- Low-profile point-of-load (POL) regulators
- Optical modules
- Core supplies
- ASICs
- FPGAs

Efficiency

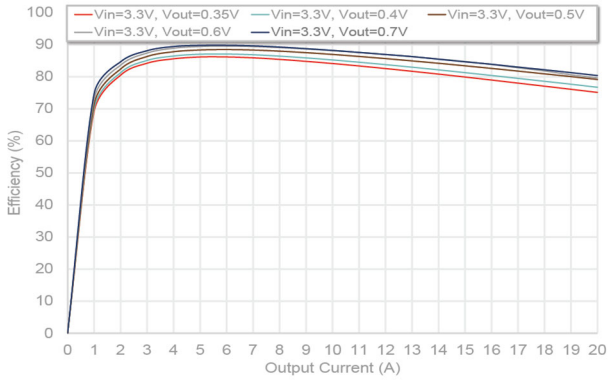

Figure 1. Single Device Efficiency Plot

Simplified Application

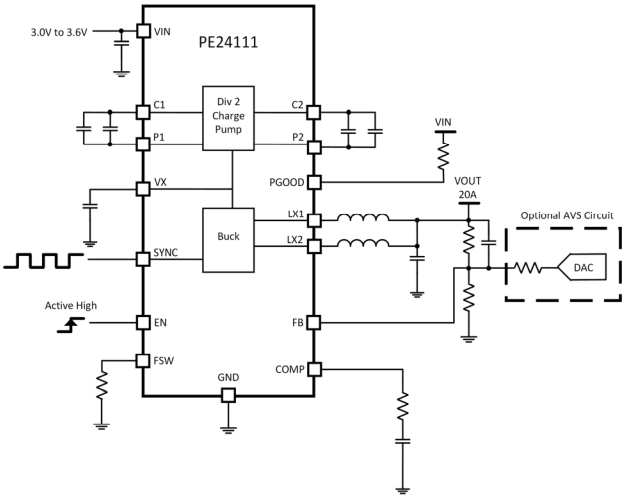

Figure 2. Typical Applications Circuit

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Absolute Maximum Ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the ratings specified in Table 1.

Table 1. PE24111 Absolute Maximum Ratings

Parameter	Min	Max	Unit
VIN to PGND	-0.3	3.8	V
EN, SYNC, FB, and COMP to PGND	-0.3	V_{IN} + 0.3	V
LX1 and LX2	-0.3	2.1	V
C1 and C2	-0.3	3.8	V
P1 and P2	-0.3	2.1	V
PGOOD	-0.3	V_{IN} + 0.3	V
VX	-0.3	2.1	V
Storage temperature (T_{ST})	-65	150	°C
Junction temperature (T_J)	-40	150	°C
Human body model, all pins[1]	–	± 2000	V
Charged device model, all pins[2]	–	± 500	V

Notes:
1. Human Body Model, all pins (Joint JEDEC/ESDA Human Body Model (JS-001-2017))
2. Charged Device Model, all pins (Joint JEDEC/ESDA Charged Device Model (JS-002-2018))

Recommended Operating Conditions

Table 2 lists the PE24111 recommended operating conditions. Do not operate the device outside the operating conditions listed below.

Table 2. PE24111 Recommended Operating Conditions

Parameter	Min	Max	Unit
V_{IN} input voltage range, relative to AGND or PGND	3.0	3.6	V
Junction temperature range, T_J	-40	125	°C

Package Thermal Characteristics

Table 3. Package Thermal Characteristics[1][2]

Parameter	Condition	Min	Max	Unit
Maximum junction temperature	Measured at max ambient temperature (T_A) and max power dissipation.	–	150.0	°C
Junction-to-case top thermal resistance (Θ_{JT})	JEDEC JESD51-12-01 and JESD15-3	17.4	–	°C/W
Junction-to-board thermal resistance (Θ_{JB})	JEDEC JESD51-12-01 and JESD15-3	3.7	–	°C/W
Junction-to-air thermal characterization (Θ_{JA})	JEDEC JESD51-12-01 and JESD15-3	29.4	–	°C/W

Notes:

1. The package thermal characteristics and performance are measured and reported in a manner consistent with the JEDEC standards JESD51-8 and JESD51-12.
2. The junction-to-ambient thermal resistance (Θ_{JA}) is a function not only of the IC but is also extremely sensitive to the environment which includes, but is not limited to, board thickness, planes, copper weight/routes, and air flow. Pay attention to the board layout to realize the expected thermal performance.

Electrical Specifications

V_{IN} = 3.0–3.6V (3.3V typical), V_{OUT} = 0.35–0.7V (0.5V typical), I_{OUT} = 0–20A per part and 10A per phase, V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -40 °C to +125 °C (25 °C typical), L = 10 nH, R_{COMP} = 909Ω, C_{COMP} = 10 nF, flying capacitors C1 and C2 = 2x 22 µF, unless otherwise noted.

Table 4. Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input supply						
Input voltage range	V_{IN}	–	3.0	–	3.6	V
UVLO threshold high	V_{UVLO_H}	V_{IN} rising	–	–	2.9	V
UVLO threshold low	V_{UVLO_L}	V_{IN} falling	2.5	–	–	V
UVLO hysteresis	V_{HYST}	–	–	100	–	mV
Supply currents						
Shutdown supply current	I_{SHDN}	V_{EN} = 0V, T_A = 25 °C	–	–	10	µA
Operating supply current	I_Q	V_{EN} > 1.1V, closed loop switching frequency = 800 kHz, V_{OUT} = 0.5V	–	55	–	mA
Thermal shutdown						
Thermal shutdown threshold	T_{TSD}	Typical temperature rising, minimum temperature falling	125	150	–	°C
Thermal shutdown hysteresis	T_{TSD_HYST}	Device is always guaranteed to operate < 125 °C	–	20	–	°C
Power good (PGOOD) threshold						
Power good under-voltage	–	V_{OUT} falling fault	–	90	–	% of V_{OUT}
Power good over-voltage	–	V_{OUT} rising	–	110	–	% of V_{OUT}
Logic thresholds (EN)						
Logic threshold high	–	Tolerant up to V_{IN} + 0.3V	0.4	–	–	V
Logic threshold low	–	–	–	–	0.3	V
Hysteresis	–	–	–	50	–	mV
Pull-down resistor	–	–	100	500	–	kΩ
Logic thresholds sync						
SYNC threshold high	–	DC coupled	0.7 × V_{IN}	–	–	V
SYNC threshold low	–	DC coupled	–	–	0.3 × V_{IN}	V
Hysteresis	–	–	–	660	–	mV
Logic outputs (PGOOD)						
Logic output low	–	I_L = 1 mA	–	–	0.4	V
Frequency						
Nominal internal clock frequency	F_{SW_NOM}	R_{FSW} = 287 kΩ or 0Ω	–	1600	–	kHz

Electrical Specifications, continued

V_{IN} = 3.0–3.6V (3.3V typical), V_{OUT} = 0.35–0.7V (0.5V typical), I_{OUT} = 0–20A per part and 10A per phase, V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -40 °C to +125 °C (25 °C typical), L = 100 nH, R_{COMP} = 909Ω, C_{COMP} = 10 nF, flying capacitors C1 and C2 = 2x 22 µF, unless otherwise noted.

Table 4. Electrical Specifications, continued

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Frequency, continued						
Internal clock frequency range	f_{SW_MG}	Via the FSW pin	1000	–	3000	kHz
Synchronization range	f_{SW_SYNC}	The external sync frequency must be higher than the internal clock frequency.	1750	–	2600	kHz
Charge pump						
Charge pump switching frequency range per phase	f_{CP_EXT}	External sync	–	0.5 x f_{SW_SYNC}	–	kHz
	f_{CP_SET}	Via the FSW pin (synced to the buck frequency)	500	–	1500	kHz
Buck converter						
Nominal buck switching frequency, per phase	$f_{SW\_BUCK\_NOM}$	R_{FSW} = 287 kΩ or 0Ω	–	800	–	kHz
Buck switching frequency range per phase	f_{SW_BUCK}	External sync	–	0.5 x f_{SW_SYNC}	–	kHz
		Via the FSW pin	500	–	1500	kHz
Buck minimum on time	T_{ON_MIN}	–	–	145	–	ns
Output voltage range	V_{OUT_SET}	–	0.35	–	0.7	V
FB set point	–	–	–	300	–	mV
FB accuracy	–	–	-2	–	+2	%
Output voltage ripple	V_{RIPPLE}	C_{OUT_NOM} = 5x 100 µF, I_{LOAD} = 20A, V_{OUT} = 0.5V, T_A = 25 °C, bandwidth = 20 MHz	–	10	–	mV
Output current	I_{OUT}	10A per phase, two phases per device. For the thermal safe operating region, see Figure 18.	20	–	–	A
Load regulation	–	I_{OUT} = 10–15A, C_{OUT_NOM} = 5x 100 µF T_A = 25 °C	–	0.5	–	mV
Line regulation	–	V_{IN} = 3.0–3.6V, V_{OUT} = 0.5V C_{OUT_NOM} = 5x 100 µF, T_A = 25 °C	–	1.65	–	mV/V
Error amplifier transconductance	–	–	–	6	–	mS
Peak current limit set point	–	Per phase	13	–	–	A
Peak current limit accuracy	–	–	–	±20	–	%

Electrical Specifications, continued

V_{IN} = 3.0–3.6V (3.3V typical), V_{OUT} = 0.35–0.7V (0.5V typical), I_{OUT} = 0–20A per part and 10A per phase, V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -40 °C to +125 °C (25 °C typical), L = 10 nH, R_{COMP} = 909Ω, C_{COMP} = 10 nF, flying capacitors C1 and C2 = 2x 22 µF, unless otherwise noted.

Table 4. Electrical Specifications, continued

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Timing						
EN to PG time	–	C_{OUT_NOM} = 5x 100 µF, I_{LOAD} = 12A	–	1.5	–	ms

Pin Configuration

Figure 3 shows the PE24111 pin configuration for the 5.2 × 4.2 × 0.55 mm QFN package, and Table 5 lists the pin descriptions.

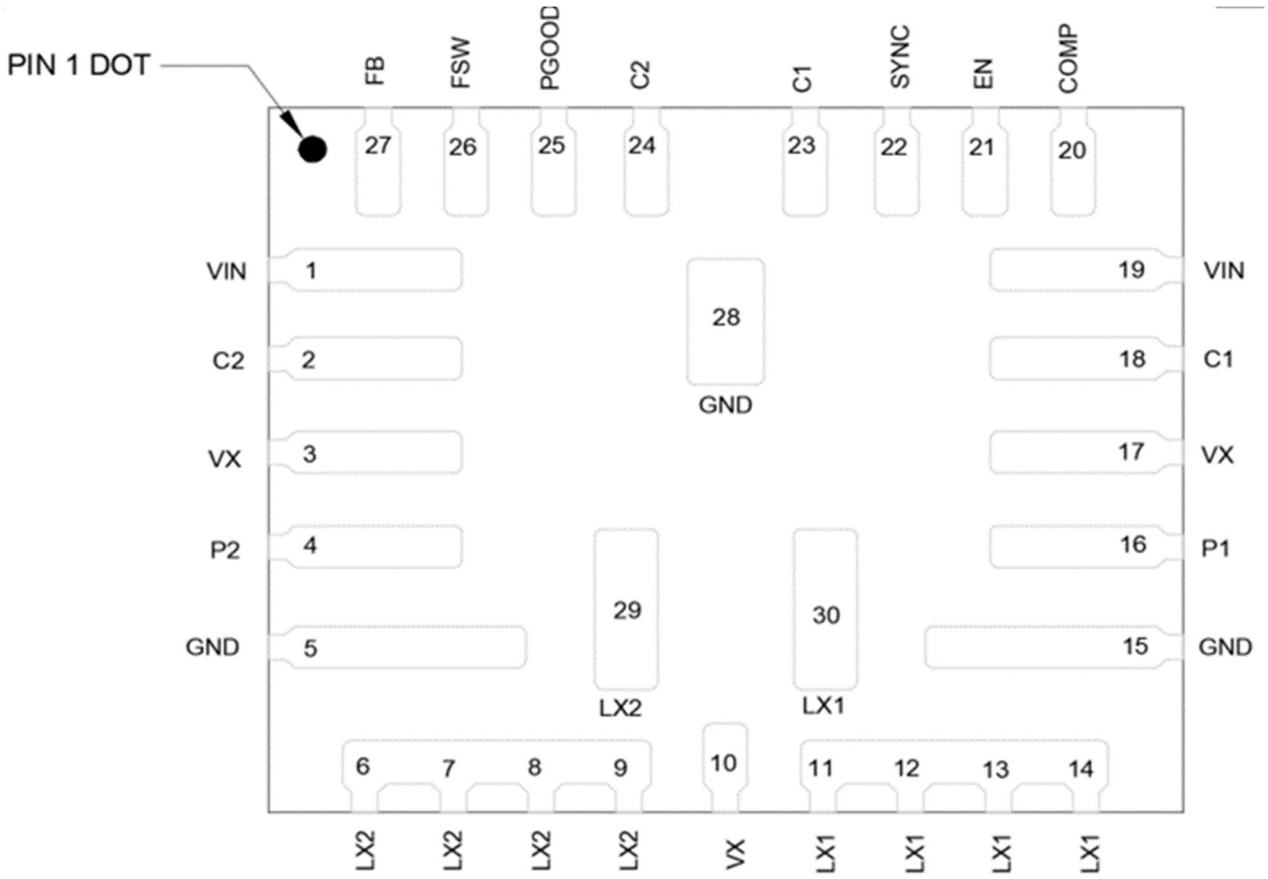


Figure 3. Pin Configuration (Top View)

Pin Descriptions

Table 5. Pin Descriptions

Pin No.	Pin Name	Description
1, 19	VIN	Connect to an input voltage between 3.0–3.6V. Bypass to GND using four 4.7 µF capacitors.
16	P1	Phase 1 flying capacitor. Connect two 22 µF capacitors between P1 and C1.
5, 15	GND	Connect to the power ground.
6, 7, 8, 9, 29	LX2	Connect to a 100 nH external chip inductor.
3, 10, 17	VX	Charge pump output capacitor. Connect a 10 µF capacitor to ground.
11, 12, 13, 14, 30	LX1	Connect to a 100 nH external chip inductor.
4	P2	Phase 2 flying capacitor. Connect two 22 µF capacitors between P2 and C2.
25	PGOOD	The PGOOD pin must be pulled up by an external resistor to a voltage less than 3.6V. In a multiple device configuration, connect all PGOOD pins to a single pull-up resistor. PGOOD is pulled low if the output voltage is below the PGOOD under-voltage or above the PGOOD over-voltage threshold. This signal is only valid after the soft start has completed.
2, 24	C2	Flying capacitor. Connect two 22 µF capacitors between this pin and P2.
27	FB	Feedback pin. To set the output voltage, set the external resistor divider to a 0.3V reference. To reduce the output ripple, add an optional 470 pF feed-forward capacitor in parallel with the top resistor. Connect all FB pins for parallel operation.
20	COMP	Compensation pin. Connect to a 909Ω resistor and a 10 nF capacitor between the COMP pin and ground for operation over the full output voltage range. This compensation can be changed to improve dynamic responses if a narrower output voltage range is used in the application.
21	EN	Enable input. Pull high to VIN or drive with a logic high to enable the converter. Connected to an internal pull down by default. For more information, see Enable (EN) on page 21.
18, 23	C1	Flying capacitor. Connect two 22 µF capacitors between this pin and P1.
22	SYNC	The sync pin is an open collector I/O pin. At startup, the internal oscillator is available on the pin. In parallel operation, connect all the sync pins, and the parts synchronize to the fastest internal oscillator. The sync pin can be overclocked by an external clock after the device initially starts. To synchronize the device, the external clock must be faster than the internal 1600 kHz clock. Both the charge pump and buck are synchronized to harmonics of this clock. For more information, see Synchronization on page 21.
26	FSW	The FSW pin sets the oscillator frequency with an external resistor to AGND. For more information, see Switching Frequency Setting on page 24.
28	GND	Analog ground pin

Functional Block Diagram

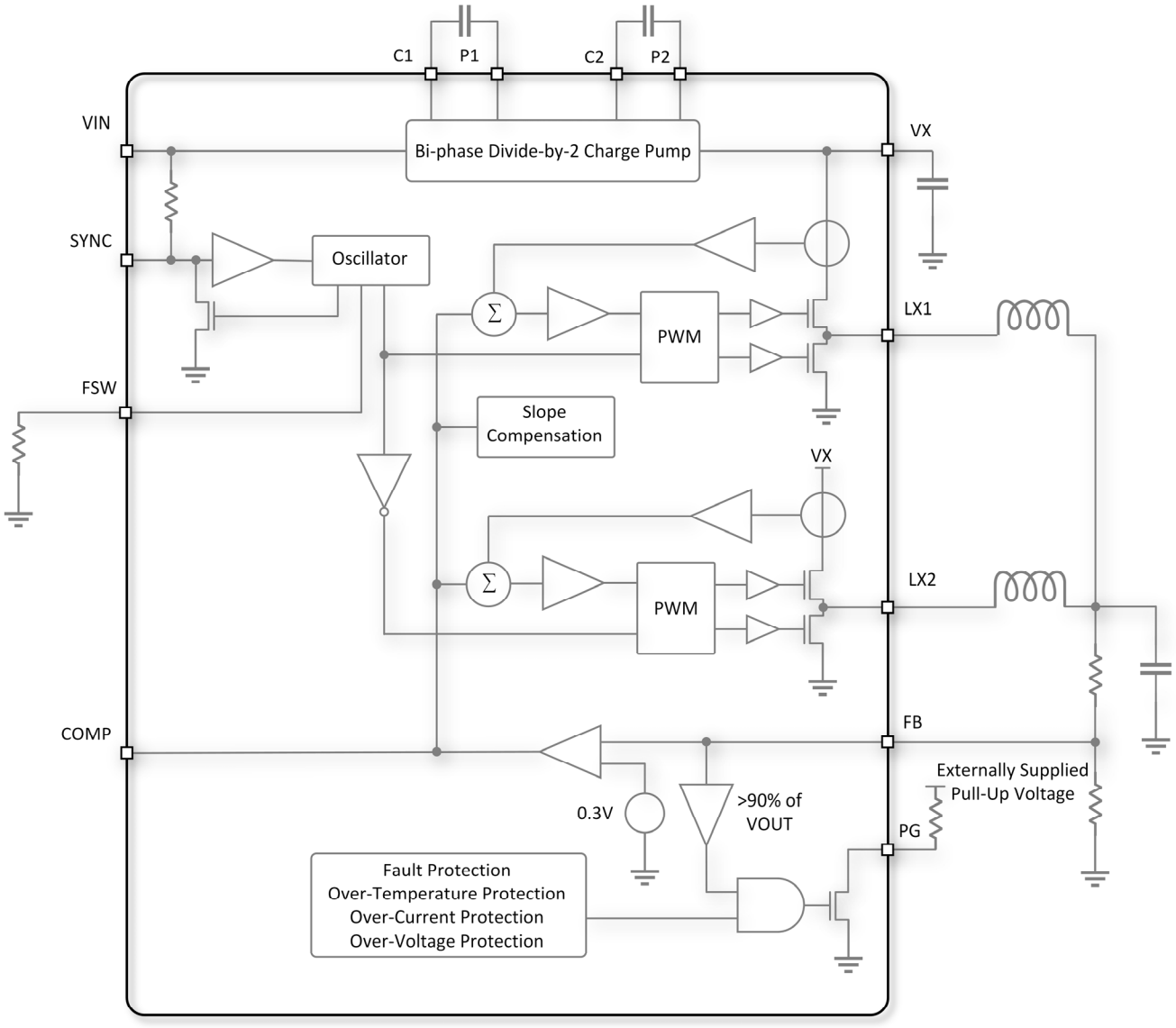


Figure 4. PE24111 Functional Block Diagram

Typical Performance Characteristics

Figure 5 through Figure 18 show the PE24111 typical operating performance data.

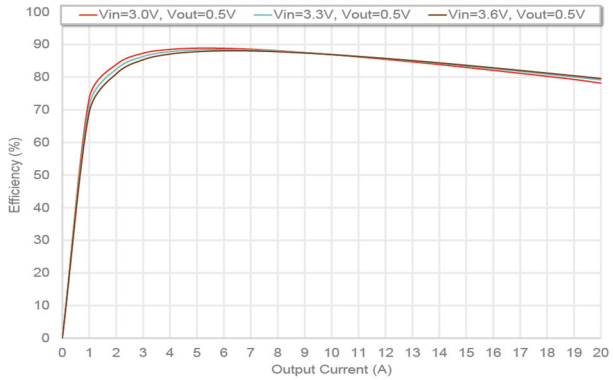


Figure 5. Efficiency vs. Load Current: V_{IN} = 3.0V, 3.3V, or 3.6V, V_{OUT} = 0.5V, Single Device, and f_{SW} = 800 kHz

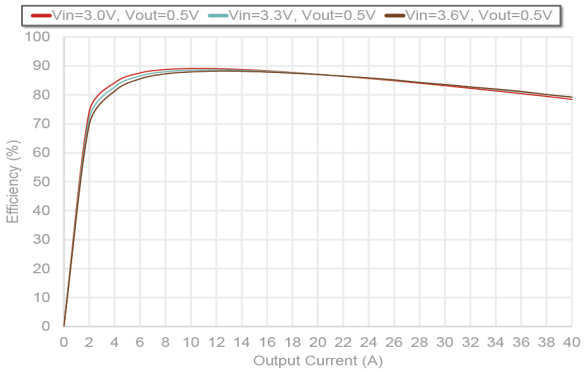


Figure 6. Efficiency vs. Load Current: V_{IN} = 3.0V, 3.3V, or 3.6V, V_{OUT} = 0.5V, Two Devices in Parallel, and f_{SW} = 800 kHz

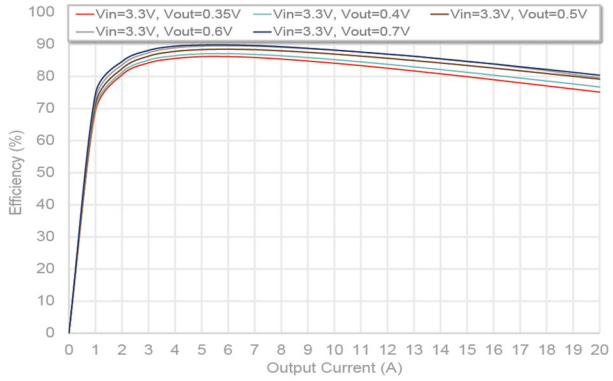


Figure 7. Efficiency vs. Load Current: V_{IN} = 3.3V, V_{OUT} = 0.35V, 0.5V, 0.6V, or 0.7V, Single Device, and f_{SW} = 800 kHz

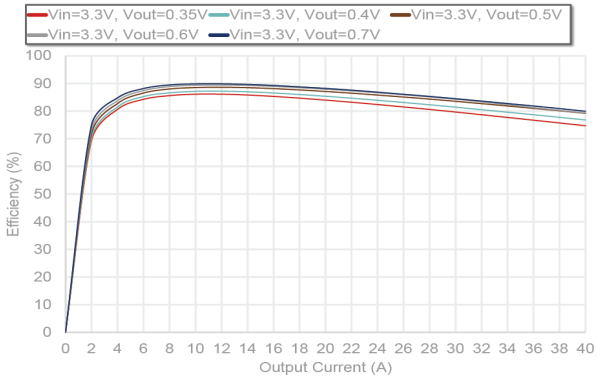


Figure 8. Efficiency vs. Load Current: V_{IN} = 3.3V, V_{OUT} = 0.35V, 0.5V, 0.6V, or 0.7V, Two Devices in Parallel, and f_{SW} = 800 kHz

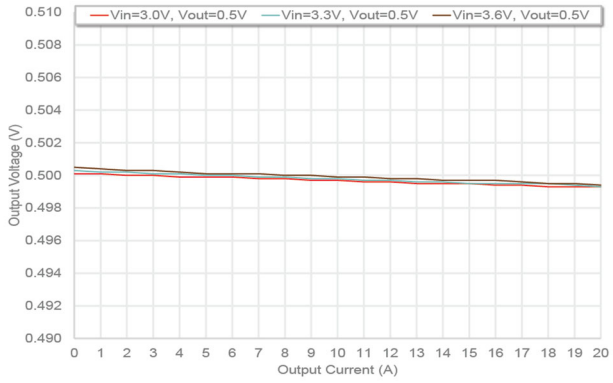


Figure 9. Output Voltage vs. Output Current: Single Device and V_{OUT} = 0.5V

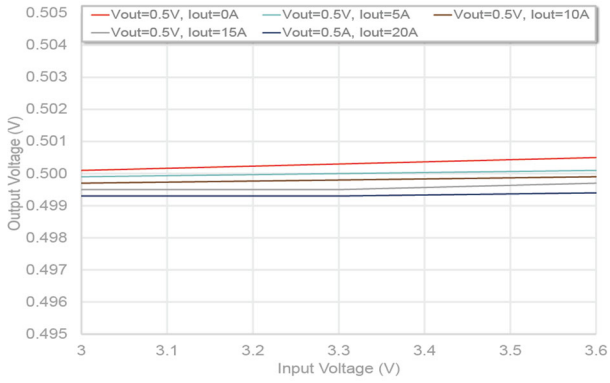


Figure 10. Line Step Output Voltage vs. Input Voltage: Single Device and V_{OUT} = 0.5V (line regulation, mV/V)

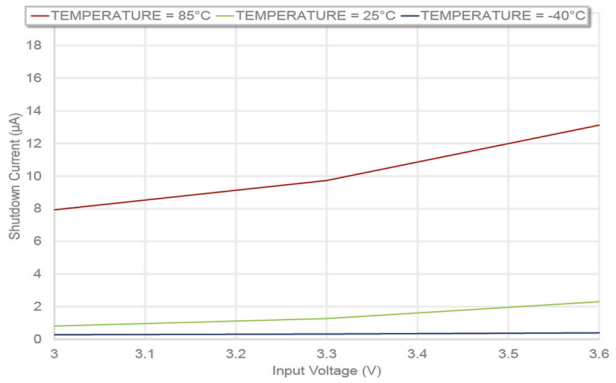


Figure 11. Shutdown Current vs. Temperature

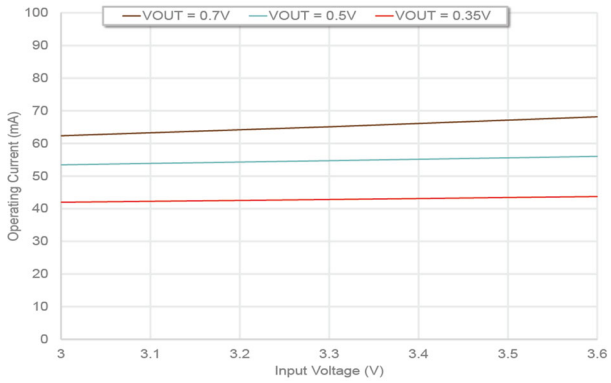


Figure 12. Supply Current vs. Input Voltage

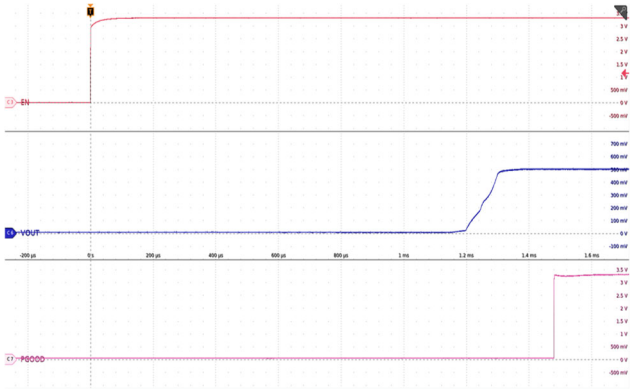


Figure 13. Startup Waveform: V_{IN} = 3.3V, V_{OUT} = 0.5V, and I_{OUT} = 0A

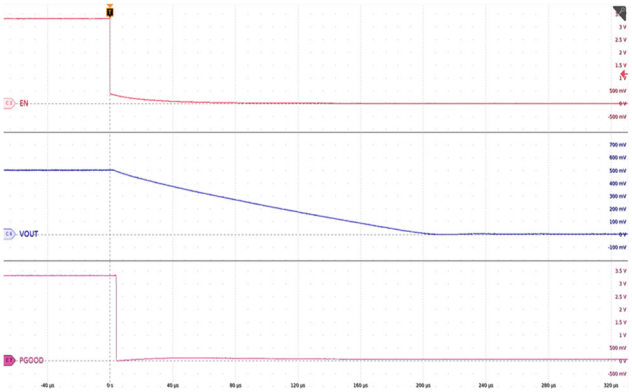


Figure 14. Shutdown Waveform: V_{IN} = 3.3V, V_{OUT} = 0.5V, and I_{OUT} = 1A

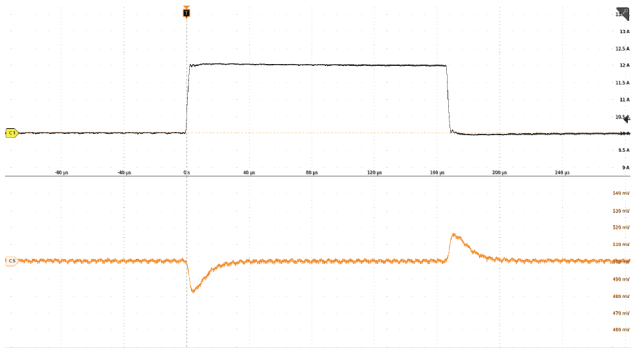


Figure 15. Load Transient: 10A to 12A, 1A/µs, V_{IN} = 3.3V, and V_{OUT} = 0.5V

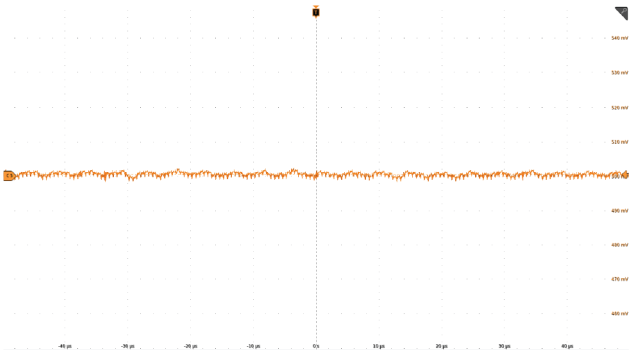


Figure 16. Output Ripple: V_{IN} = 3.3V, V_{OUT} = 0.5V, and I = 10A

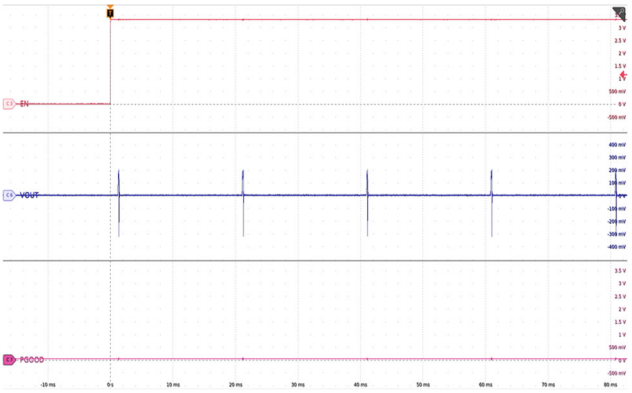


Figure 17. Startup into Short Circuit

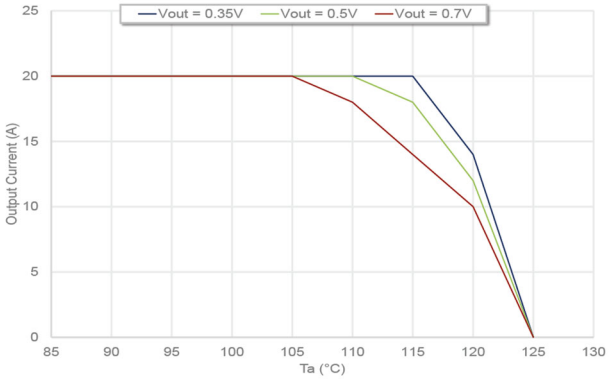


Figure 18. Thermal Safe Operating Region

Theory of Operation

The PE24111 is a two-stage, DC-DC POL regulator that can be used in parallel operation to allow higher current outputs.

Charge Pump

Most of the power conversion is done by a divide-by-two charge pump. This charge pump works like an open-loop DC transformer in which the output voltage tracks the input voltage and presents the downstream buck regulator with an unregulated input voltage much lower than a traditional single-stage buck.

The charge pump is based on pSemi's patented, proprietary architecture that employs soft start, soft switching, and close synchronization with the buck stage to ensure that no current flows during transitions within the charge pump. This eliminates issues such as the in-rush current and large transition losses seen in more traditional charge pumps.

The charge pump also demonstrates extremely high conversion efficiency with much lower EMI than traditional single-stage buck architectures. The phase-interleaved design uses two individual charge pumps operating in parallel along with a 50% charge-pump duty cycle. This design minimizes pulsed currents at the input and exhibits very low input ripple, regardless of the output voltage of the downstream buck stage.

The charge pump relies on well-balanced capacitance values and the overall operating conditions, so pay close attention to the physical sizing of the capacitors and the effects of DC bias on capacitance.

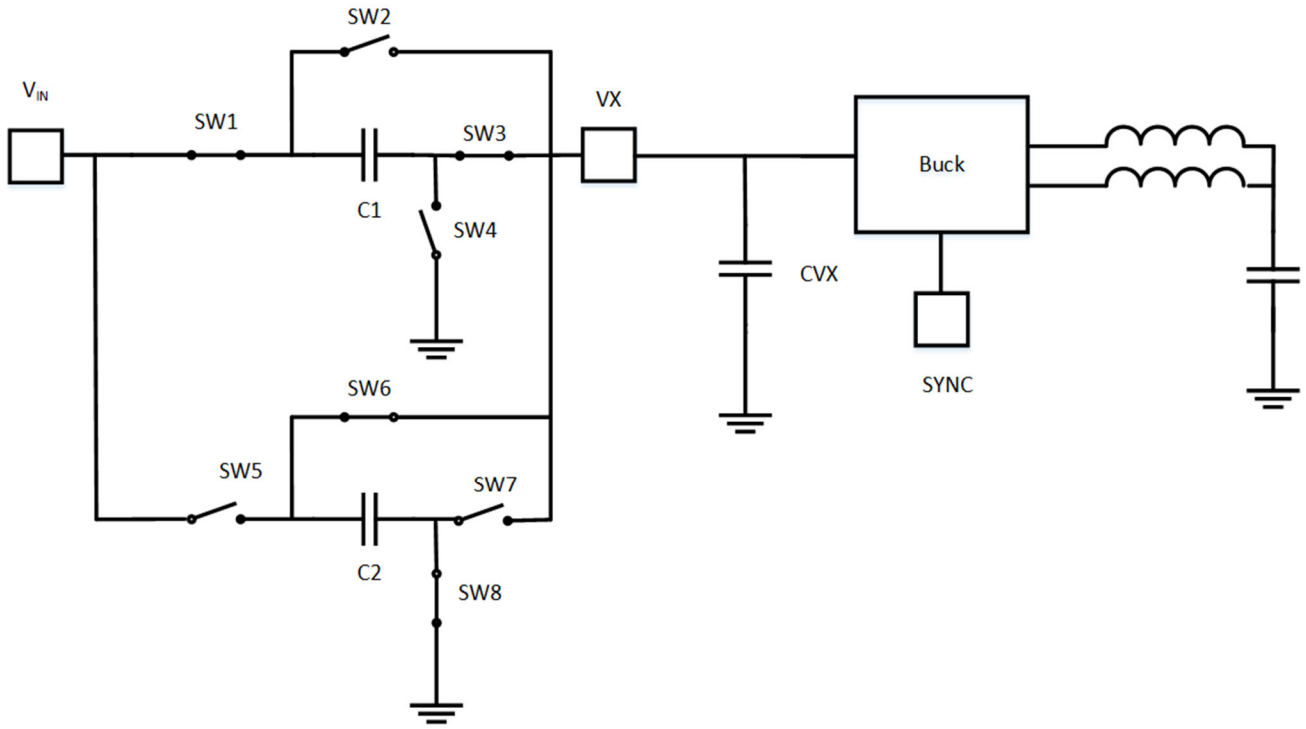


Figure 19. Phase 1 Charge Pump Operation

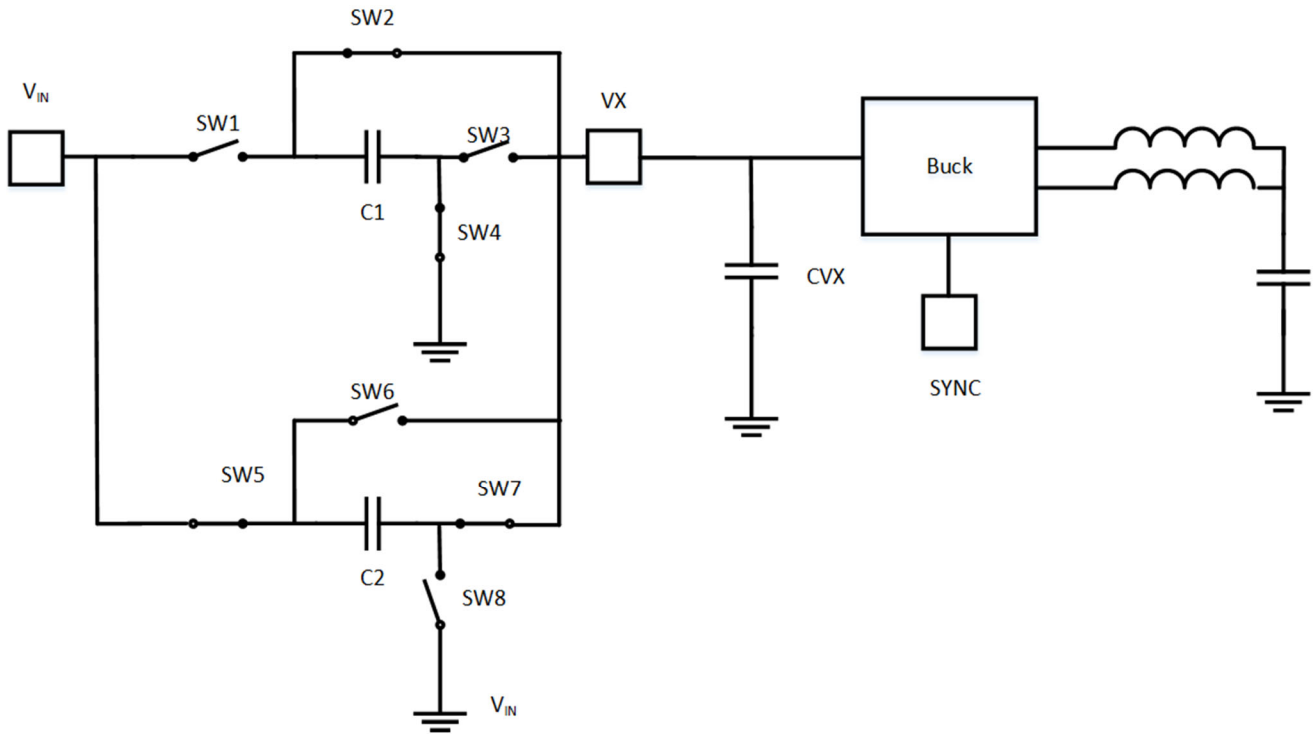


Figure 20. Phase 2 Charge Pump Operation

Between the two phases, a constant flow of energy is drawn from the input and supplied to the downstream buck converter. This further minimizes conducted EMI at the input of the converter and ensures a very low intermediate noise for the buck converter.

Buck Converter

The buck converter uses fixed-frequency peak current mode pulse-width modulation (PWM) control to regulate the output voltage. It has two PWM phases interleaved with a fixed-phase difference of 180 degrees.

The buck converter switching frequency can be overdriven by using the SYNC pin to further control system EMI. For more information, see Synchronization on page 21.

Buck Regulator Compensation

The buck regulator is a two-phase, fixed-frequency peak current mode regulator with phases staggered 180º apart.

Both regulators connect to a single-slope compensation pin (COMP). In normal operation, pSemi recommends connecting the COMP pin to a 909 Ω resistor and 10 nF capacitor to ground as shown in Figure 21.

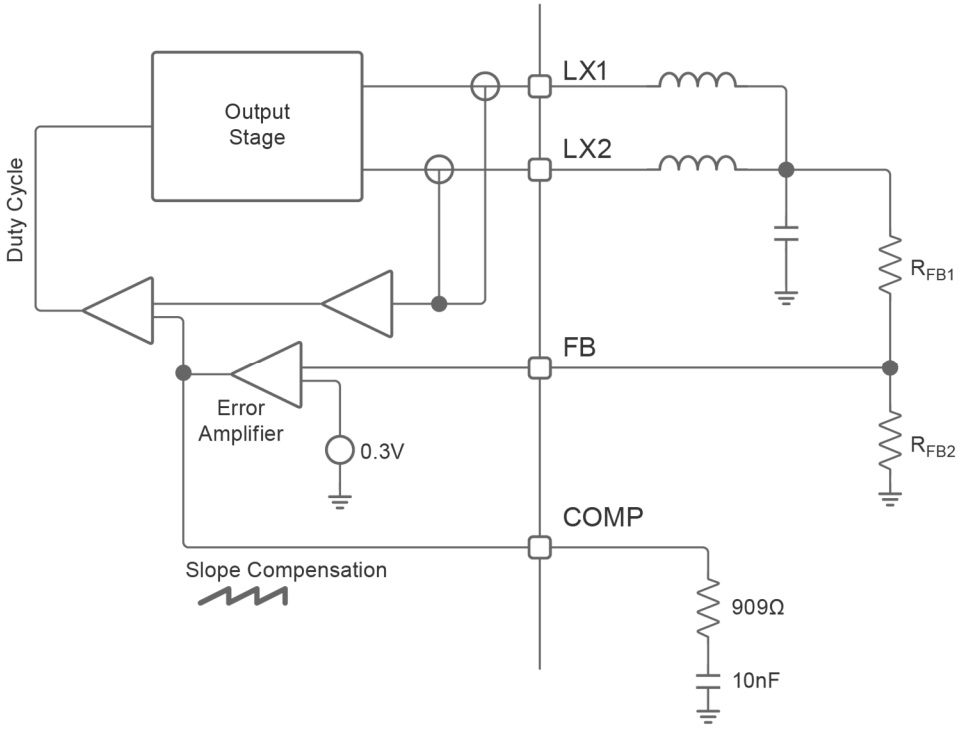


Figure 21. Compensation Circuit

Detailed Description

Setting the Output Voltage

The output voltage is set by the external feedback resistors connected between VOUT and ground, which are compared to an internal 300 mV reference. To prevent noise-coupling onto the FB pin, the divider resistor values must not be too high. For parallel operation, connect the FB pins.

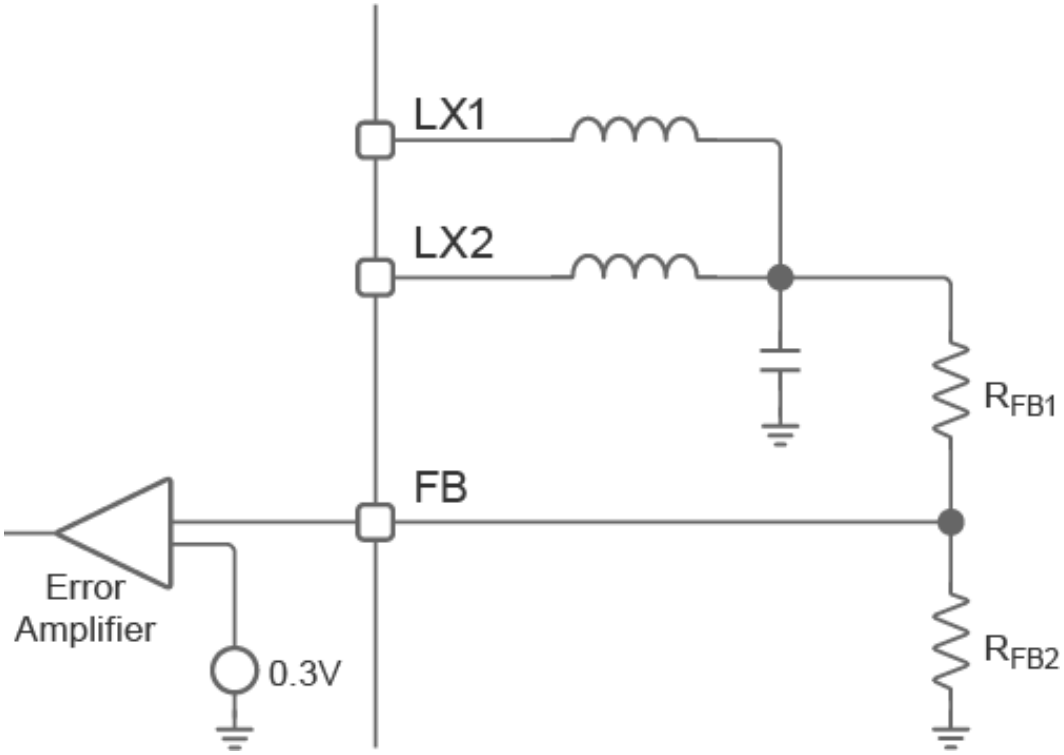


Figure 22. Set the Output Voltage with External Feedback Resistors

To set the output voltage, first select an R_{FB2} value of < 10 kΩ.

To calculate the R_{FB1} value, use the following formula, in which V_{FB} = 0.3V.

$$R_{FB1} = R_{FB2}.\frac{VOUT - V_{FB}}{V_{FB}}$$

When picking the top resistor value first, calculate the bottom resistor R_{FB2} as follows:

$$R_{FB2} = \frac{R_{FB1}.V_{FB}}{V_{OUT} - V_{FB}}$$

To maintain the initial accuracy specifications of the device, pSemi recommends using 0.1% resistors. For higher accuracy, close the loop with an external DAC.

Power-up Sequence

The PE24111 wakes up when V_{IN} exceeds the input under-voltage (UVLO) threshold of 2.9V and the EN pin is pulled above the threshold voltage.

Initially, the device powers up its internal logic and then, if no fault is present, it proceeds to balance the charge pump.

After this, the charge pump operates in soft start control. This process continues until the charge pump is charged to within 10% of V_{IN}/2.

When this happens, the charge pump enters normal switching and can supply the full load current.

Next, the buck regulator soft starts until the output voltage is reached.

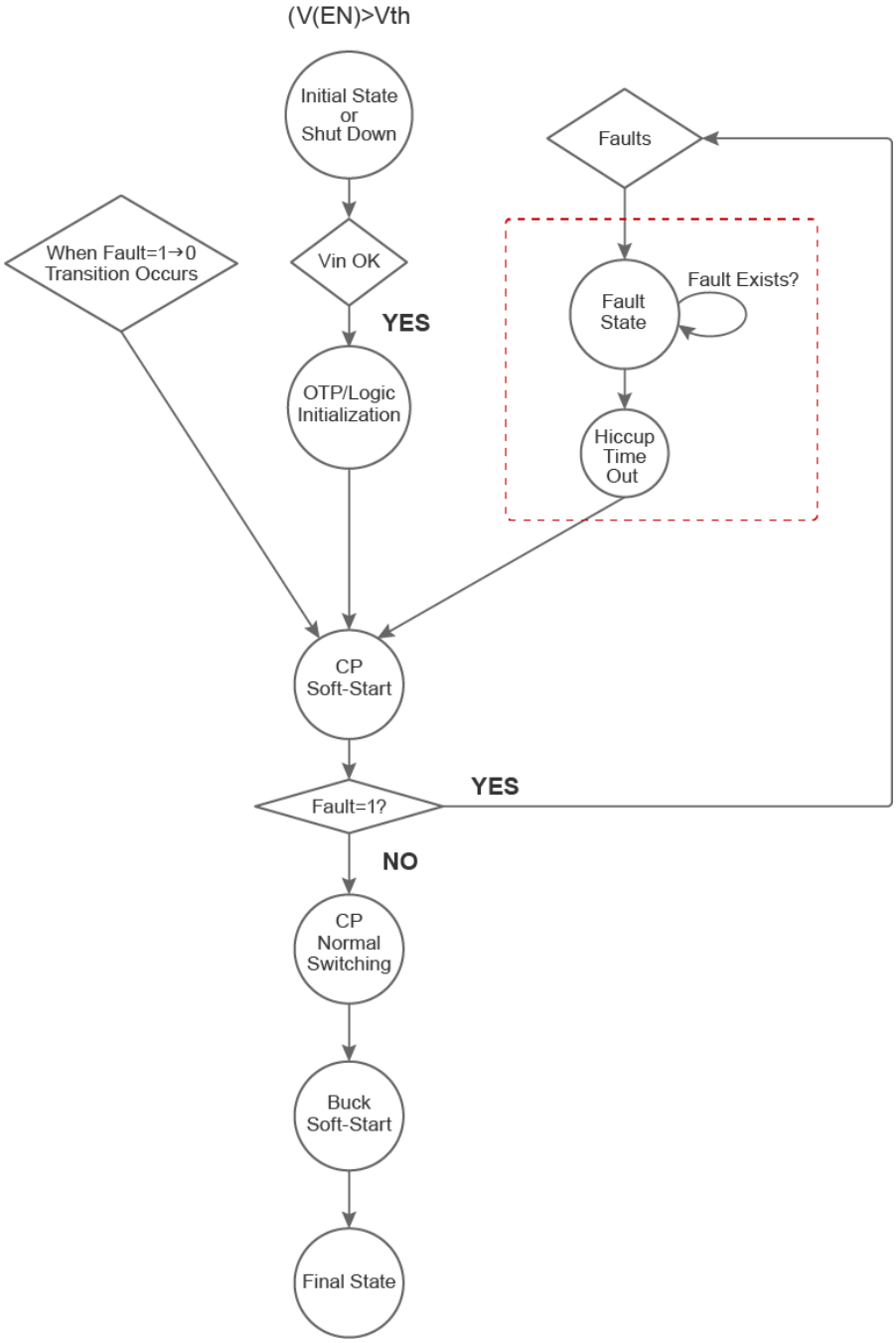


Figure 23. Power-up Sequence

During the initial power-up sequence and until PGOOD goes high, the PE24111 always uses its own internal oscillator. After PGOOD is established, you can synchronize the PE24111 to an external clock on the SYNC pin. The time from the PE24111 being enabled to PGOOD going high is 1.5 ms.

Enable (EN)

pSemi designed the enable (EN) pin to be compatible with low-voltage logic signals from DSP controllers and ASICs and has a threshold high of 0.4V. A voltage on the EN pin above 0.4V enables the PE24111. The EN pin is tolerant of voltages up to VIN + 0.3V and can be tied directly to the input supply to enable the device upon power-up.

If a voltage of less than 0.2V is present on the EN pin, the PE24111 enters shutdown.

Input Under-voltage Lockout (UVLO)

The PE24111 is intended to work from a 3.3V input supply and begins operating above its UVLO rising threshold (V_{UVLO_H}) of 2.9V. The UVLO threshold has a typical hysteresis of 200 mV.

Synchronization

The PE24111 contains an internal oscillator that initially switches at the frequency set by the FSW pin, which is double the switching frequency of the charge pump and buck converter. If the application uses the internal oscillator, leave the SYNC pin unconnected.

To synchronize a device to an external clock—or to place multiple devices in parallel—connect an external clock to the SYNC pin. The internal oscillator then synchronizes to the clock edges of the fastest clock on the SYNC pin. The frequency applied to the SYNC pin must be greater than the default clock frequency set by the FSW pin. For more information on the internal clock settings, see Switching Frequency Setting on page 24.

From a DC perspective, the SYNC pin has thresholds set at 70% and 30% of V_{DD}. The input sync waveform must exceed these thresholds for the SYNC signal to be recognized.

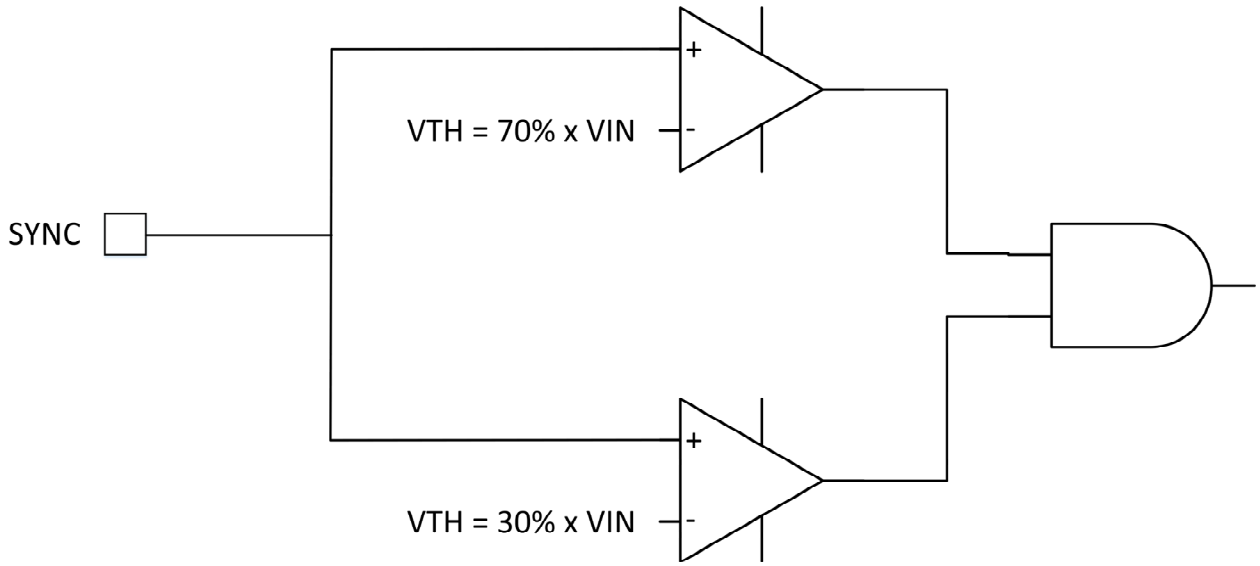


Figure 24. SYNC Pin Thresholds

To synchronize with an external clock, the SYNC pin can be overdriven by connecting directly to an external clock, as shown in Figure 25.

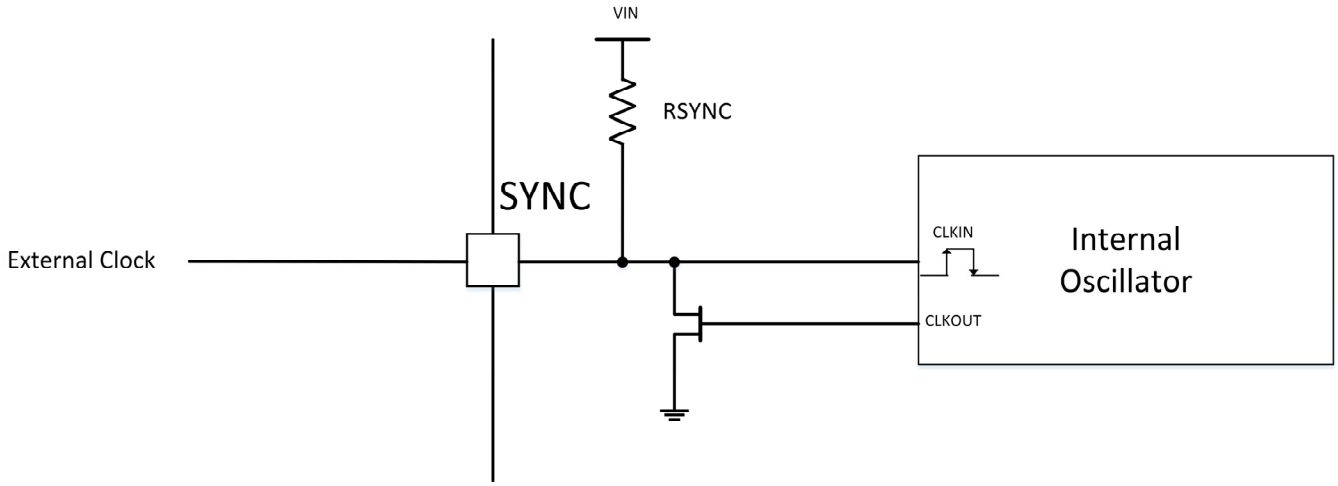


Figure 25. Synchronization Circuit

If the voltage level is less than these levels, the device does not synchronize. The scope plots in Figure 26 and Figure 27 show the device with SYNC waveforms below and above the threshold, respectively.

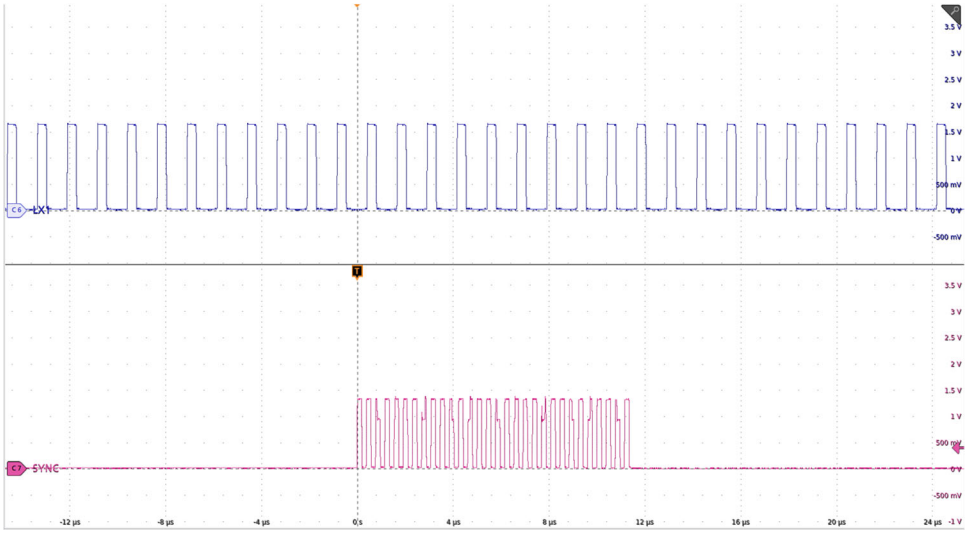


Figure 26. Scope Plot Showing Device Not Synchronizing with SYNC = 1.4V DC Coupled

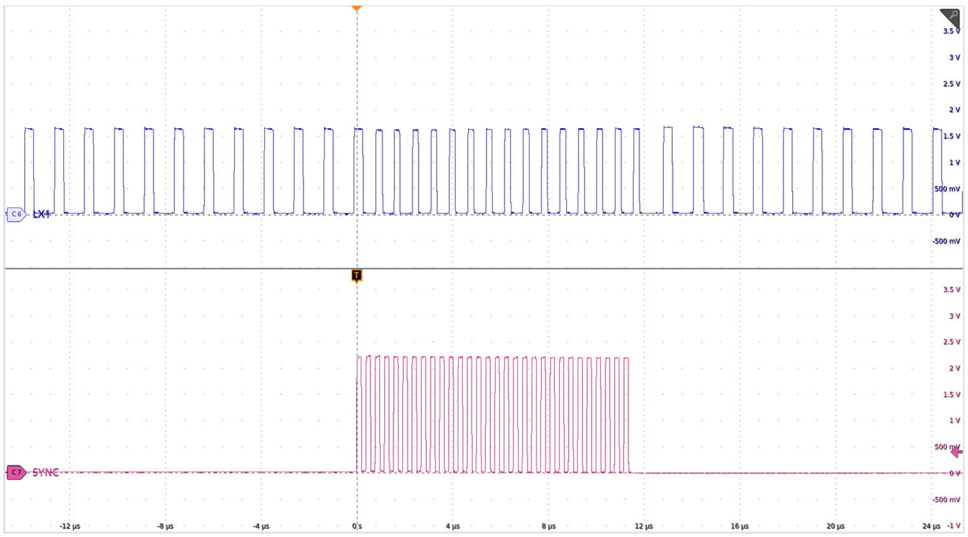


Figure 27. Scope Plot Showing Device Synchronization with SYNC = 2.1V DC Coupled

Power Good (PGOOD)

The PGOOD pin is an open drain pin. The PGOOD pin must be pulled up externally to a power supply of less than 3.6V.

During startup, the PGOOD pin is pulled low until 180 µs (typical) after the output voltage reaches within 10% of the value—such as > 90% of VOUT—programed by the feedback resistors. Above this, the PGOOD pulldown FET is high impedance, and the PGOOD pin is pulled up by the external resistor.

If the output voltage goes above the PGOOD over-voltage level, the PGOOD pin is pulled low.

When operating multiple devices in parallel, connect the PGOOD pins together to a single pull-up resistor.

Temperature Detection

The PE24111 includes an integrated temperature sensor that protects the device in the event of overheating. If the PE24111 enters thermal shutdown, its outputs are turned off to reduce power dissipation inside the device. When the temperature drops below the hysteresis limit, the output turns on again. If the underlying cause of the over-temperature fault is not cleared, the system enters a *hiccup* mode of operation until the fault condition is removed.

Switching Frequency Setting

The PE24111 supports user-selectable default switching frequency options for the charge pump and down-stream buck converter. The switching frequency is selected by tying a 1% tolerance resistor between the FSW pin and AGND. The device reads the resistance upon VIN being applied and EN being pulled high. The decoded value is then latched until the next time the power is cycled or the EN pin is pulled low. To identify what resistance to tie between FSW and AGND for your preferred switching frequency setting, see Table 6. The internal clock frequency setting will be twice the frequency of the charge pump and buck switching frequency.

Table 6. Switching Frequency Setting vs. Resistance between FSW Pin and AGND

R_{FSW} (Ω)	Charge Pump and Buck Switching Frequency (kHz)	Internal Clock Frequency Setting (kHz)
0	800	1600
22.1k	1500	3000
40.2k	1200	2400
84.5k	1000	2000
287k	800	1600
1M	500	1000
Open	800	1600

Verify that the calculated on time is above the minimum on time (typically 145 ns). pSemi recommends some margin between the calculated on time and the minimum on time to account for transient behavior. Limit the switching frequency to 1.2 MHz for VOUT below 0.5V. Calculate the on time using the following equation:

$$TON = \frac{VOUT}{\left(\frac{VIN\_MAX}{2}\right) * FSW}$$

Fault Protection

The PE24111 provides extensive protection against input and output faults, output overload, and over-temperature, as listed in Table 7.

Table 7. Fault protection

Fault	Fault Response	Fault Detection Time[1]	Threshold
VIN under-voltage	Power on reset	Immediate (VIN falling)	< 2.5V
VOUT over-voltage	PGOOD pulled low	Immediate	> 110% of target VOUT
VOUT under-voltage	PGOOD pulled low	Immediate	< 90% of target VOUT
VOUT short circuit	PGOOD pulled low; hiccup mode[2]	Immediate	
Peak current limit	PGOOD pulled low; hiccup mode[2]	Immediate	> 20A
Over temperature[3]	PGOOD pulled low; hiccup mode[4]	Immediate	> 150 °C

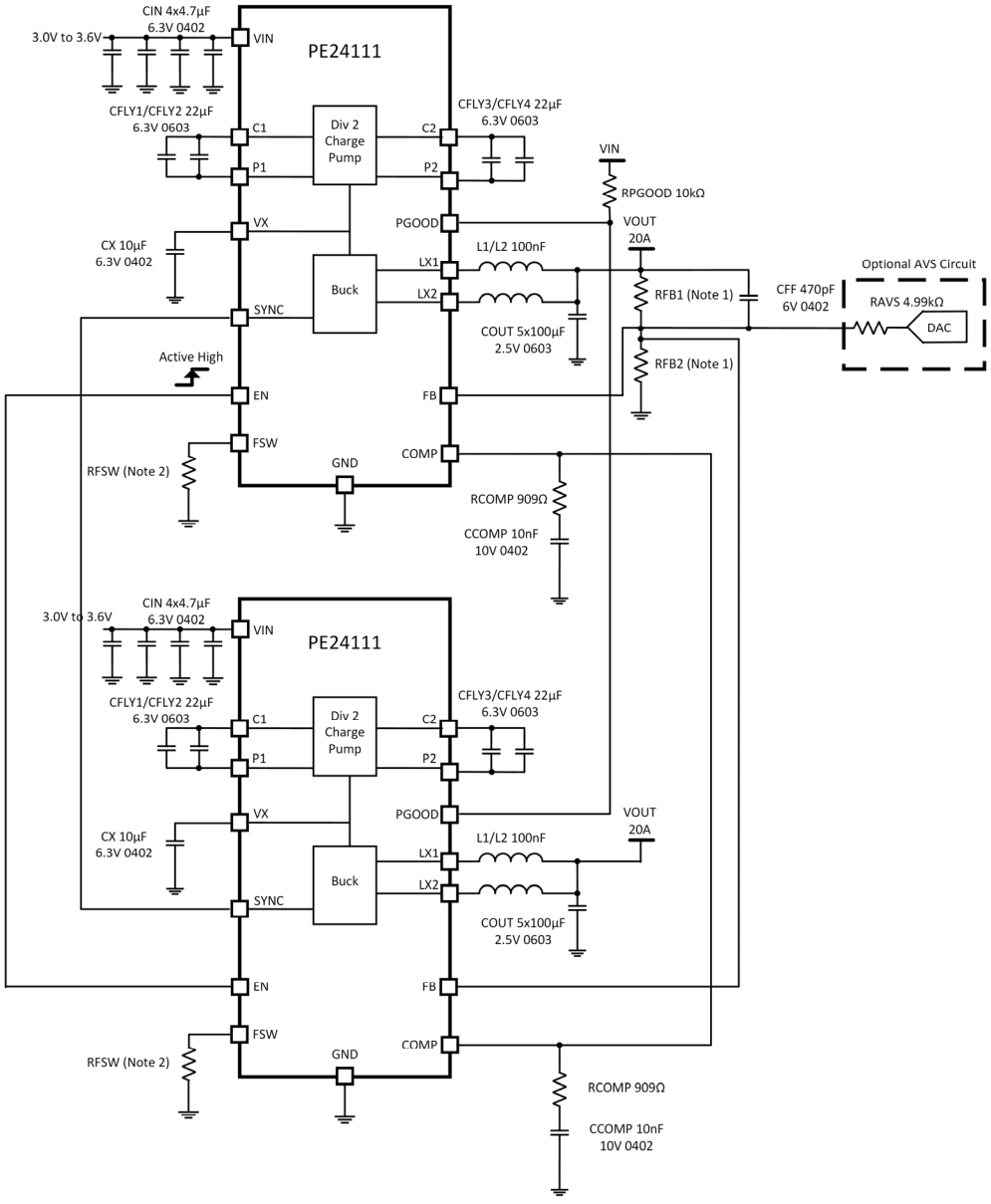
Notes:

1. Typical detection time. For the minimum and maximum specifications, see the Electrical Specifications in Table 4.
2. In hiccup mode, switching is disabled, the output is tri-stated, and a 20 ms wait timer is started. When the wait timer expires, the system attempts to restart the charge-pump stage but hiccups until the fault condition is cleared. During this state, PGOOD is set to 0 until the fault is removed.
3. The PE24111 junction temperature is used for the over-temperature detection.
4. The system does not attempt to restart until a wait timer has expired and the PE24111 junction temperature has dropped below the over-temperature hysteresis threshold.

Applications Information

Parallel Operation

You can connect a maximum of four PE24111 devices in parallel as power stages allowing output currents of 20A, 40A, or 60A. In parallel operation, connect the FB, SYNC, COMP, PGOOD, and EN pins of both devices. To adjust the output voltage, use a single DAC externally feeding a current through a resistor into the feedback network, as shown in Figure 28.



Note 1: See the "Setting the Output Voltage" section for information regarding selecting values for RFB1 and RFB2.
Note 2: See the "Switching Frequency Setting" section for information regarding selecting a value for RFSW to set the switching frequency for the part.

Figure 28. Two PE24111 Devices Operating in Parallel

Example Layout of Two Devices in Parallel

Figure 29 shows an example of two parts in parallel providing 40A supply at V_{OUT} = 0.35V to 0.7V. This layout can fit in a very small form factor, because the dual-stage architecture is extremely thin at 1.2 mm.

To ensure proper current sharing between the devices, keep the output impedance between the devices and the load as equal as possible.

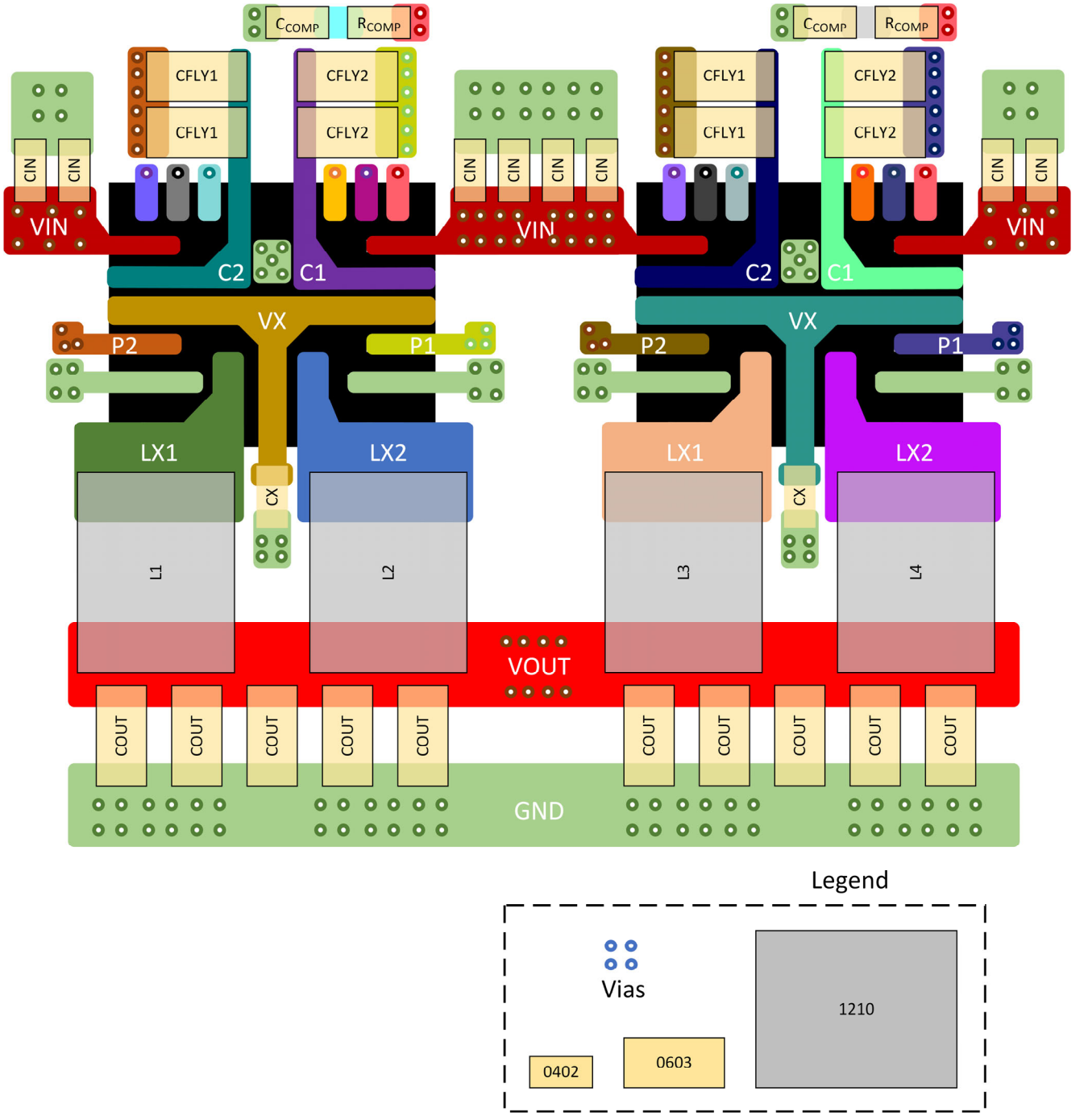


Figure 29. Example Layout of Two Parallel Devices

Oscillator Synchronization in Parallel Operation

The PE24111 has a SYNC pin that can be used for three separate operation modes:

- Basic standalone operation
- Parallel operation without an external clock
- Parallel operation with a common external clock

Basic Standalone Operation

In basic operation mode for a standalone PE24111 configured for a 20A supply, nothing needs to be connected to the SYNC pin. The SYNC pin oscillates at its own internal oscillator frequency.

Parallel Operation Without an External Clock

In parallel operation of multiple PE24111s without an external clock, connect the SYNC pins. In this mode, the devices synchronize to the fastest clock of the devices in parallel.

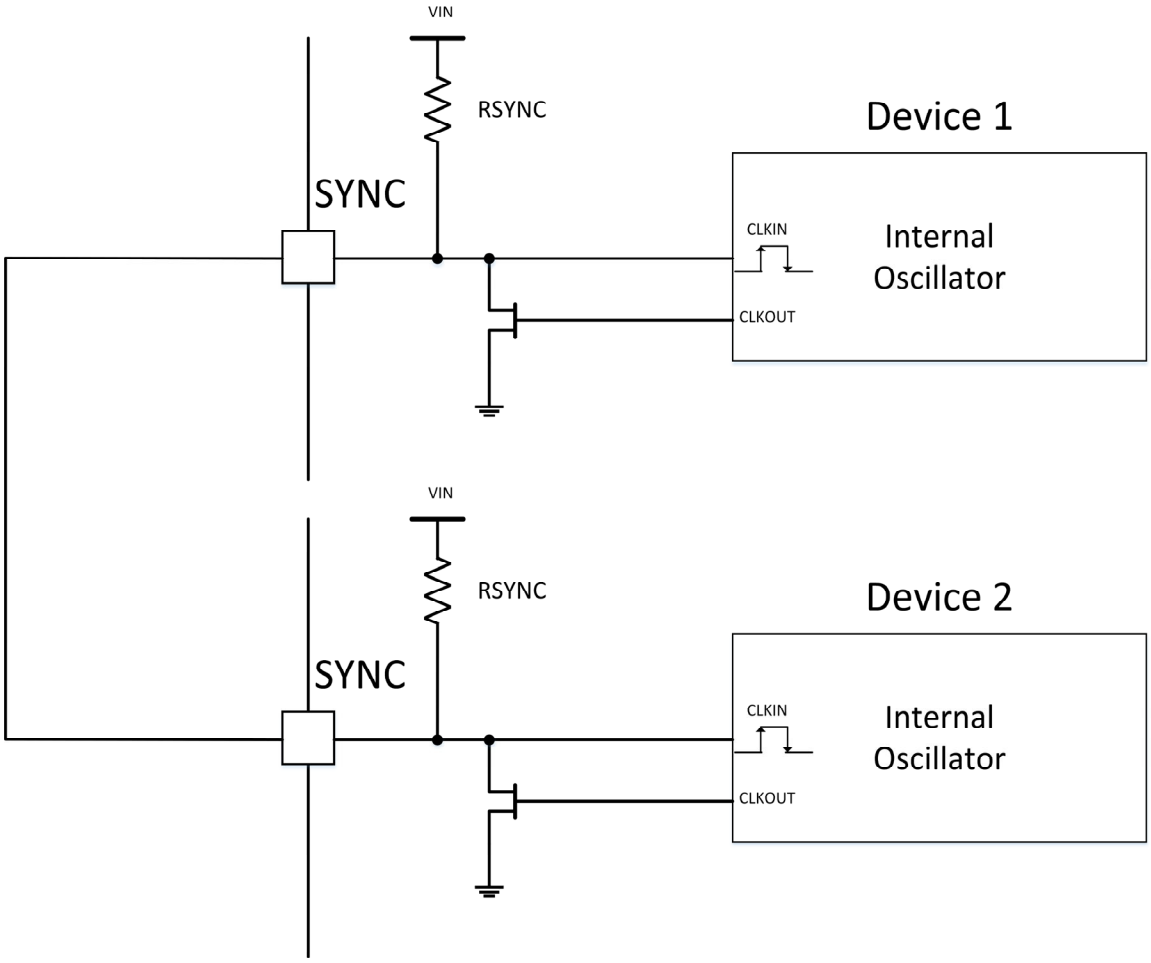


Figure 30. Sync Pin Connections for Parallel Operation without an External Clock

Parallel Operation with a Common External Clock

In parallel operation of multiple PE24111s with a common external clock, connect the SYNC pins. Initially on power-up, the devices synchronize to the fastest internal clock. When the external clock is applied after the initial power-up, it must clock the SYNC pin between 1750 kHz and 2600 kHz and to a frequency faster than the internal oscillator frequency set by the FSW pin. For more information, see Switching Frequency Setting on page 24.

After this, all the parts synchronize their internal oscillators to this frequency.

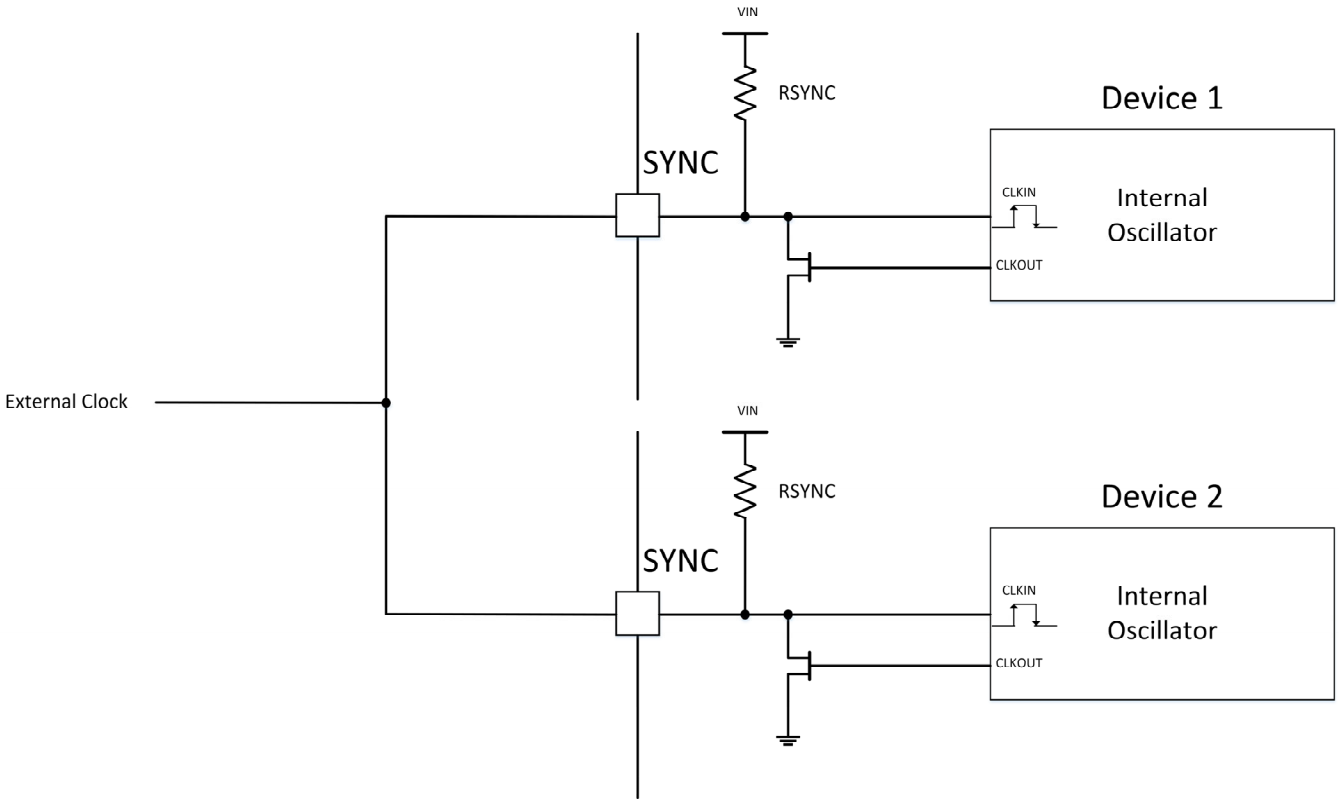


Figure 31. SYNC pin Connections for Parallel Operation with a Common External Clock

Adjusting the Output Voltage AVS

The output voltage of the PE24111 is set externally by the resistor network into the feedback pin. This voltage can be adjusted externally by using a DAC and feeding the adjustment into the feedback node to scale the output voltage to optimize performance for low-voltage core supplies. In parallel operation, only one DAC is required to adjust the feedback node. Tie all other FB pins together.

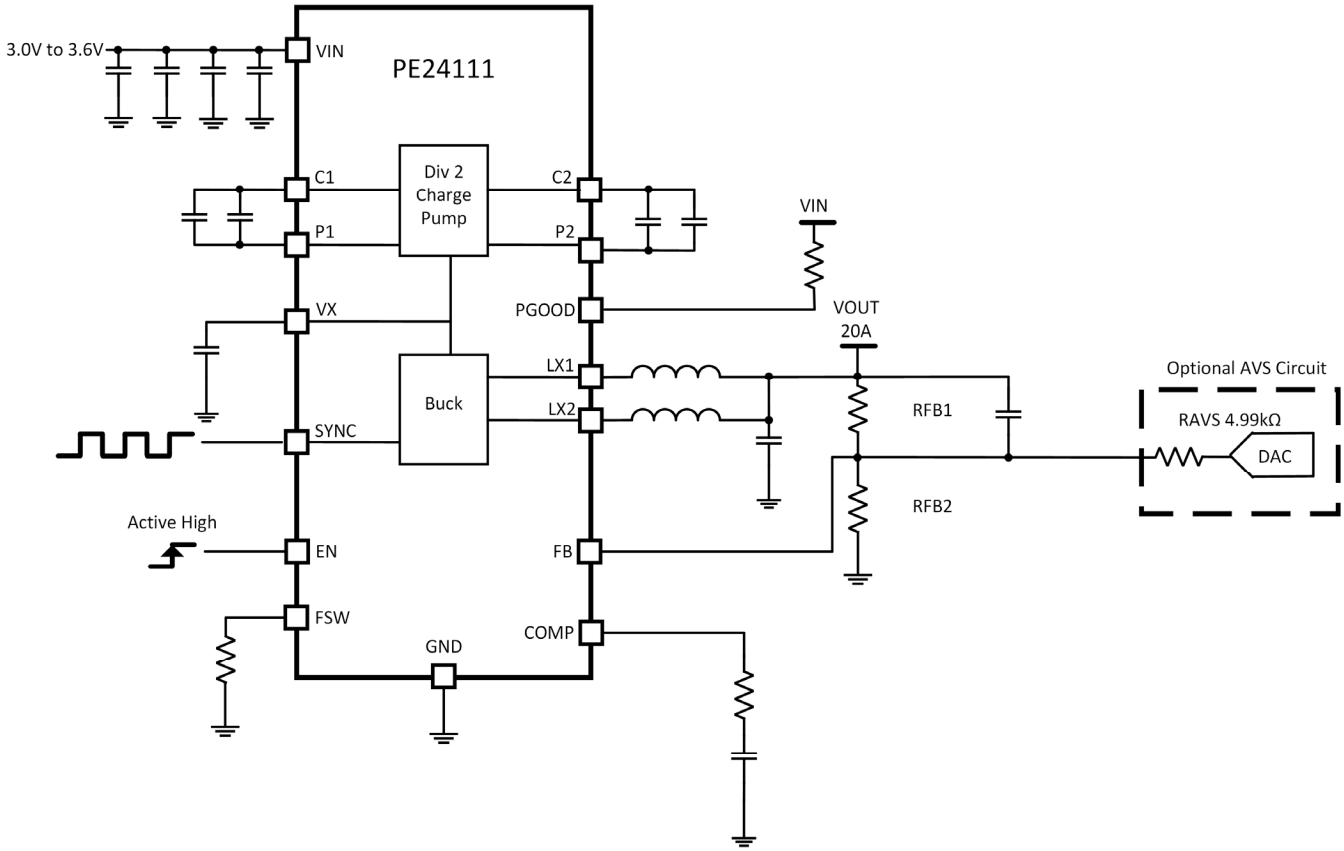
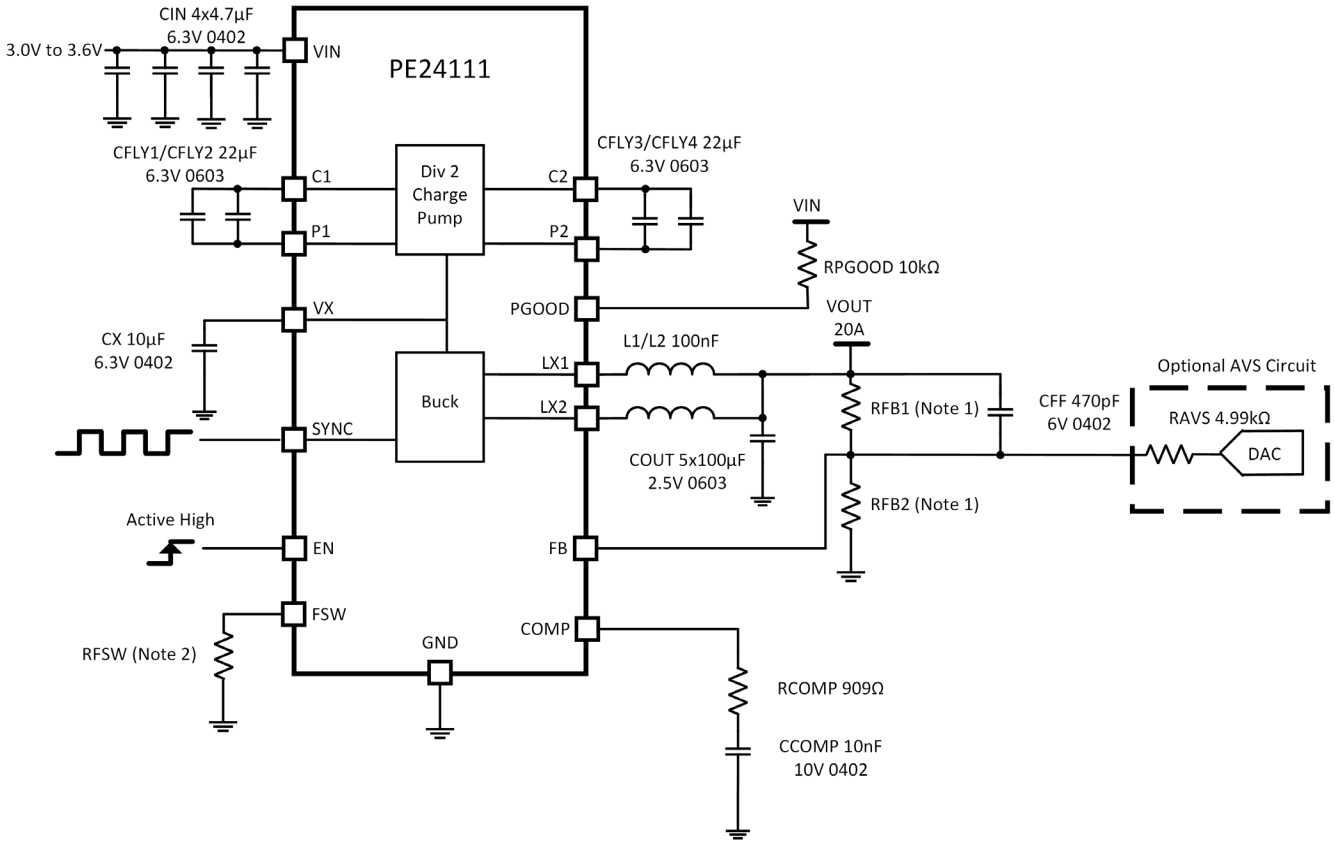


Figure 32. Adjusting the Output Voltage with an External DAC

Typical Applications Circuit



Note 1: See the "Setting the Output Voltage" section for information regarding selecting values for RFB1 and RFB2.
Note 2: See the "Switching Frequency Setting" section for information regarding selecting a value for RFSW to set the switching frequency for the part.

Figure 33. Typical Applications Circuit

Packaging Information

This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the 5.2 × 4.2 × 0.55 mm QFN package is MSL1.

Package Drawing

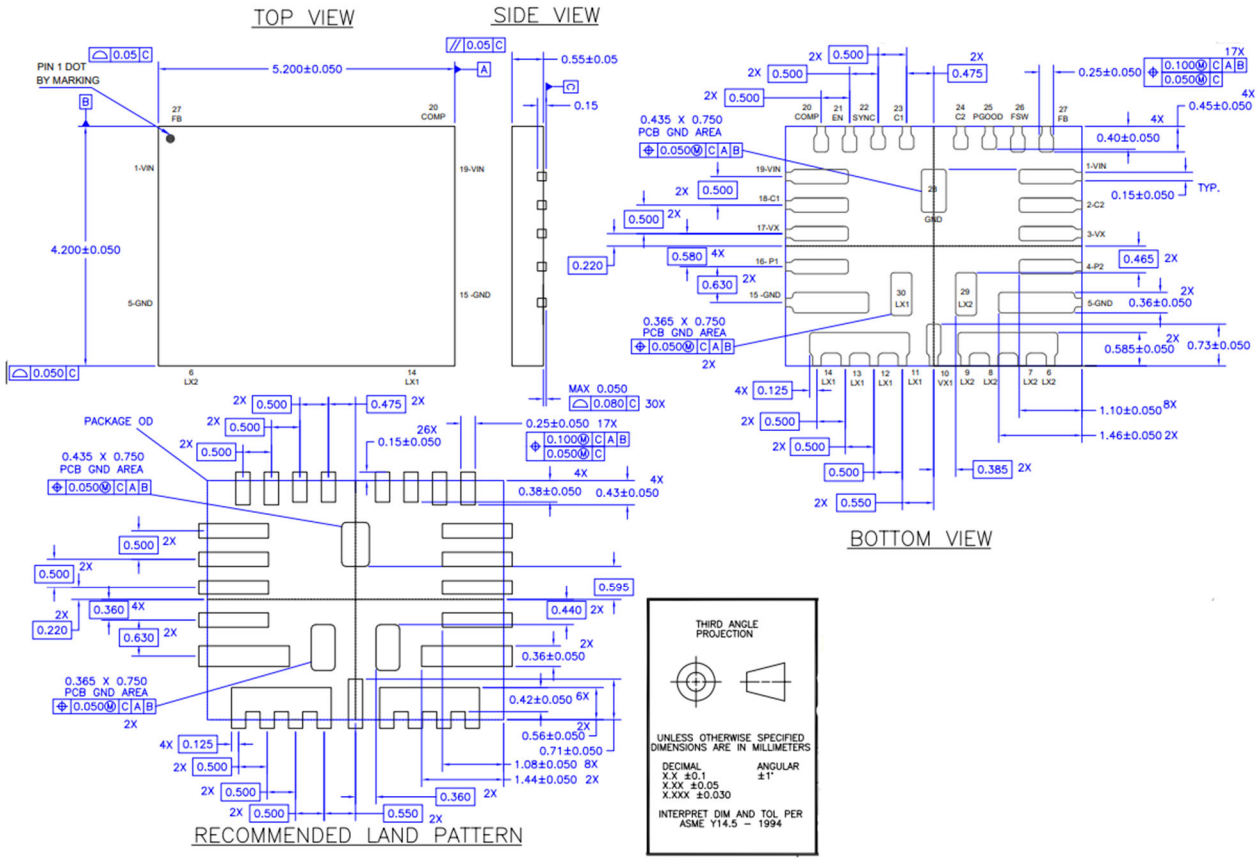


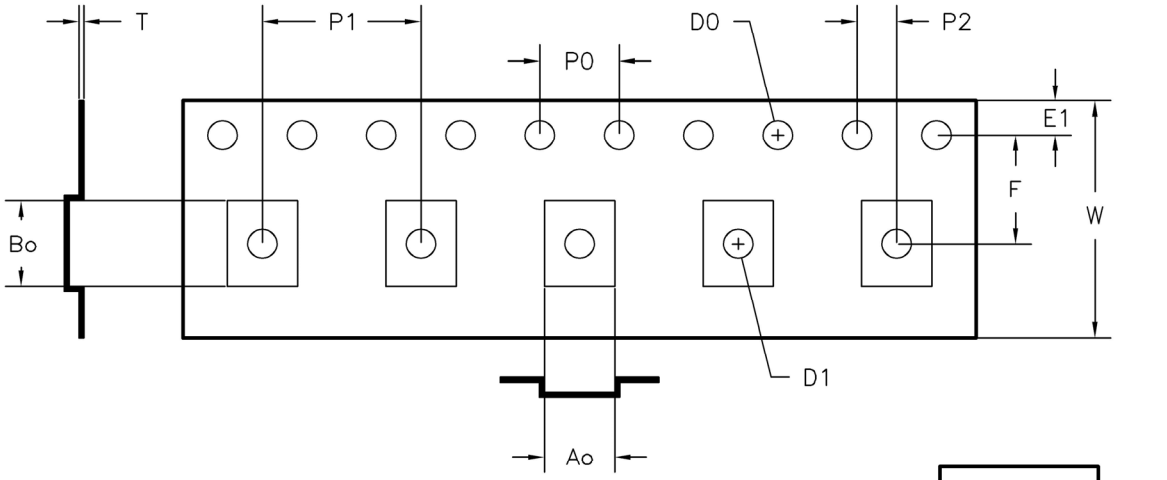
Figure 34. Package Drawing for the 5.2 × 4.2 × 0.55 mm QFN

Top-marking Specification

● = Pin 1 indicator
PPPPP = Product part number
YY = Last two digits of assembly year (2022 = 22)
WW = Assembly Work Week (01,02,03,...,52)
ZZZZZZ = Assembly lot code (maximum six characters)

Figure 35. Package Marking Specification

Tape and Reel Specification



Notes:

Not drawn to scale.
Dimensions are in Millimeters
Maximum cavity angle 5 degrees.
Bumped die are oriented active side down.

Carrier Tape Dimension Table

Pocket	Nominal	Tolerance	Pocket	Nominal	Tolerance
Ao	3.55	+/- 0.10	D1	1.50	+ 0.2 / - 0
Bo	4.30	+/- 0.10	D0	1.50	+ 0.1 / - 0
Ko	0.75	+/- 0.10	E1	1.75	+/- 0.1
P1	8.00	+/- 0.1	P0	4.00	+/- 0.1
W	12.00	+ 0.3 / - 0.1	P2	2.00	+/- 0.05
F	5.50	+/- 0.05	T	0.25	+/- 0.03

Figure 36. Tape and Reel Specification

Ordering Information

Table 8. Order Codes and Shipping Methods

Order Codes	Description	Packaging	Shipping Method
PE24111A-X	20A buck regulator	QFN on tape and reel	500 units/T&R
PE24111A-Z	20A buck regulator	QFN on tape and reel	3000 units/T&R

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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