

PDTA115T series

PNP resistor-equipped transistors; R1 = 100 k Ω , R2 = open

Rev. 05 — 2 September 2009

Product data sheet

1. Product profile

1.1 General description

PNP resistor-equipped transistors.

Table 1. Product overview

Type number	Package		NPN complement
	NXP	JEITA	
PDTA115TE	SOT416	SC-75	PDTC115TE
PDTA115TK	SOT346	SC-59	PDTC115TK
PDTA115TM	SOT883	SC-101	PDTC115TM
PDTA115TS ^[1]	SOT54 (TO-92)	SC-43A	PDTC115TS
PDTA115TT	SOT23	-	PDTC115TT
PDTA115TU	SOT323	SC-70	PDTC115TU

[1] Also available in SOT54A and SOT54 variant packages (see [Section 2](#))

1.2 Features

- Built-in bias resistors
- Reduces component count
- Simplifies circuit design
- Reduces pick and place costs

1.3 Applications

- General purpose switching and amplification
- Circuit drivers
- Inverter and interface circuits

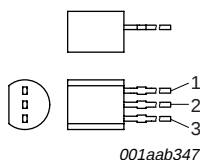
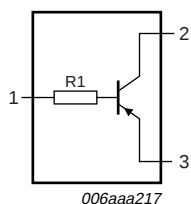
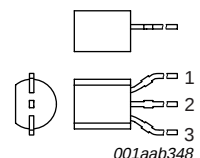
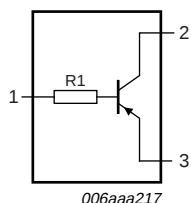
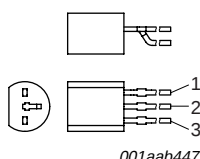
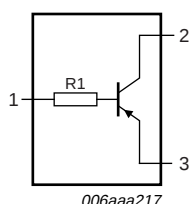
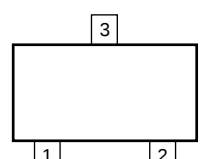
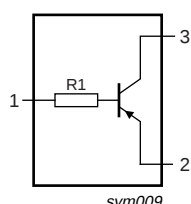
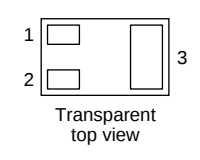
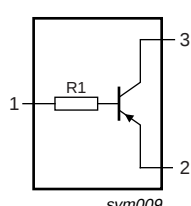
1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	-50	V
I_O	output current (DC)		-	-	-100	mA
R1	bias resistor 1 (input)		70	100	130	k Ω

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Symbol
SOT54			
1	input (base)		
2	output (collector)		
3	GND (emitter)		
SOT54A			
1	input (base)		
2	output (collector)		
3	GND (emitter)		
SOT54 variant			
1	input (base)		
2	output (collector)		
3	GND (emitter)		
SOT23, SOT323, SOT346, SOT416			
1	input (base)		
2	GND (emitter)		
3	output (collector)		
SOT883			
1	input (base)		
2	GND (emitter)		
3	output (collector)		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PDTA115TE	SC-75	plastic surface mounted package; 3 leads	SOT416
PDTA115TK	SC-59	plastic surface mounted package; 3 leads	SOT346
PDTA115TM	SC-101	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTA115TS ^[1]	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTA115TT	-	plastic surface mounted package; 3 leads	SOT23
PDTA115TU	SC-70	plastic surface mounted package; 3 leads	SOT323

[1] Also available in SOT54A and SOT54 variant packages (see [Section 2](#) and [Section 9](#)).

4. Marking

Table 5. Marking codes

Type number	Marking code ^[1]
PDTA115TE	12
PDTA115TK	11
PDTA115TM	E8
PDTA115TS	TA115T
PDTA115TT	*AC
PDTA115TU	*11

[1] * = -: made in Hong Kong
 * = p: made in Hong Kong
 * = t: made in Malaysia
 * = W: made in China

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter	-	-50	V
V _{CEO}	collector-emitter voltage	open base	-	-50	V
V _{EBO}	emitter-base voltage	open collector	-	-5	V
I _O	output current (DC)		-	-100	mA
I _{CM}	peak collector current		-	-100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT416		[1] -	150	mW
	SOT346		[1] -	250	mW
	SOT883		[2][3] -	250	mW
	SOT54		[1] -	500	mW
	SOT23		[1] -	250	mW
	SOT323		[1] -	200	mW
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	+150	°C

[1] Refer to standard mounting conditions.

[2] Reflow soldering is the only recommended soldering method.

[3] Refer to SOT883 standard mounting conditions; FR4 printed-circuit board with 60 μm copper strip line.

6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air				
	SOT416		[1] -	-	833	K/W
	SOT346		[1] -	-	500	K/W
	SOT883		[2][3] -	-	500	K/W
	SOT54		[1] -	-	250	K/W
	SOT23		[1] -	-	500	K/W
	SOT323		[1] -	-	625	K/W

[1] Refer to standard mounting conditions.

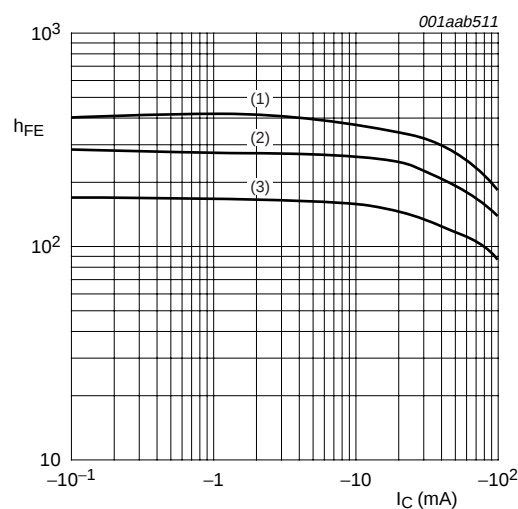
[2] Reflow soldering is the only recommended soldering method.

[3] Refer to SOT883 standard mounting conditions; FR4 printed-circuit board with 60 μm copper strip line.

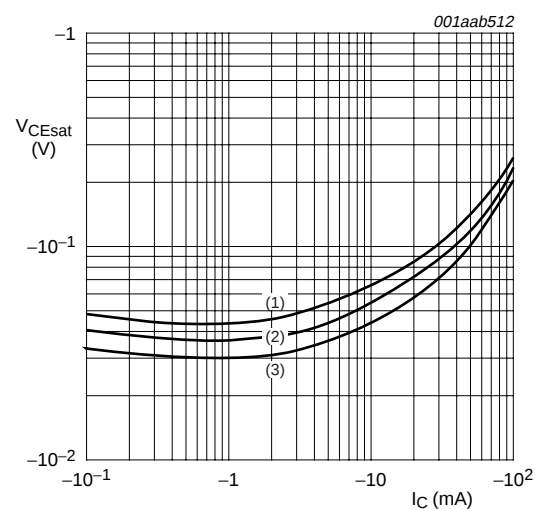
7. Characteristics

Table 8. Characteristics
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CBO}	collector-base cut-off current	$V_{CB} = -50\text{ V}$; $I_E = 0\text{ A}$	-	-	-100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = -30\text{ V}$; $I_B = 0\text{ A}$	-	-	-1	μA
		$V_{CE} = -30\text{ V}$; $I_B = 0\text{ A}$; $T_j = 150\text{ }^{\circ}\text{C}$	-	-	-50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}$; $I_C = 0\text{ A}$	-	-	-100	nA
h_{FE}	DC current gain	$V_{CE} = -5\text{ V}$; $I_C = -1\text{ mA}$	100	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -5\text{ mA}$; $I_B = -0.25\text{ mA}$	-	-	-150	mV
R1	bias resistor 1 (input)		70	100	130	k Ω
C_c	collector capacitance	$V_{CB} = -10\text{ V}$; $I_E = i_e = 0\text{ A}$; $f = 1\text{ MHz}$	-	-	3	pF


 $V_{CE} = -5\text{ V}$.

- (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$.
- (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$.
- (3) $T_{amb} = -40\text{ }^{\circ}\text{C}$.

Fig 1. DC current gain as a function of collector current; typical values

 $I_C/I_B = 20$.

- (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$.
- (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$.
- (3) $T_{amb} = -40\text{ }^{\circ}\text{C}$.

Fig 2. Collector-emitter saturation voltage as a function of collector current; typical values

8. Package outline

Plastic surface-mounted package; 3 leads

SOT416

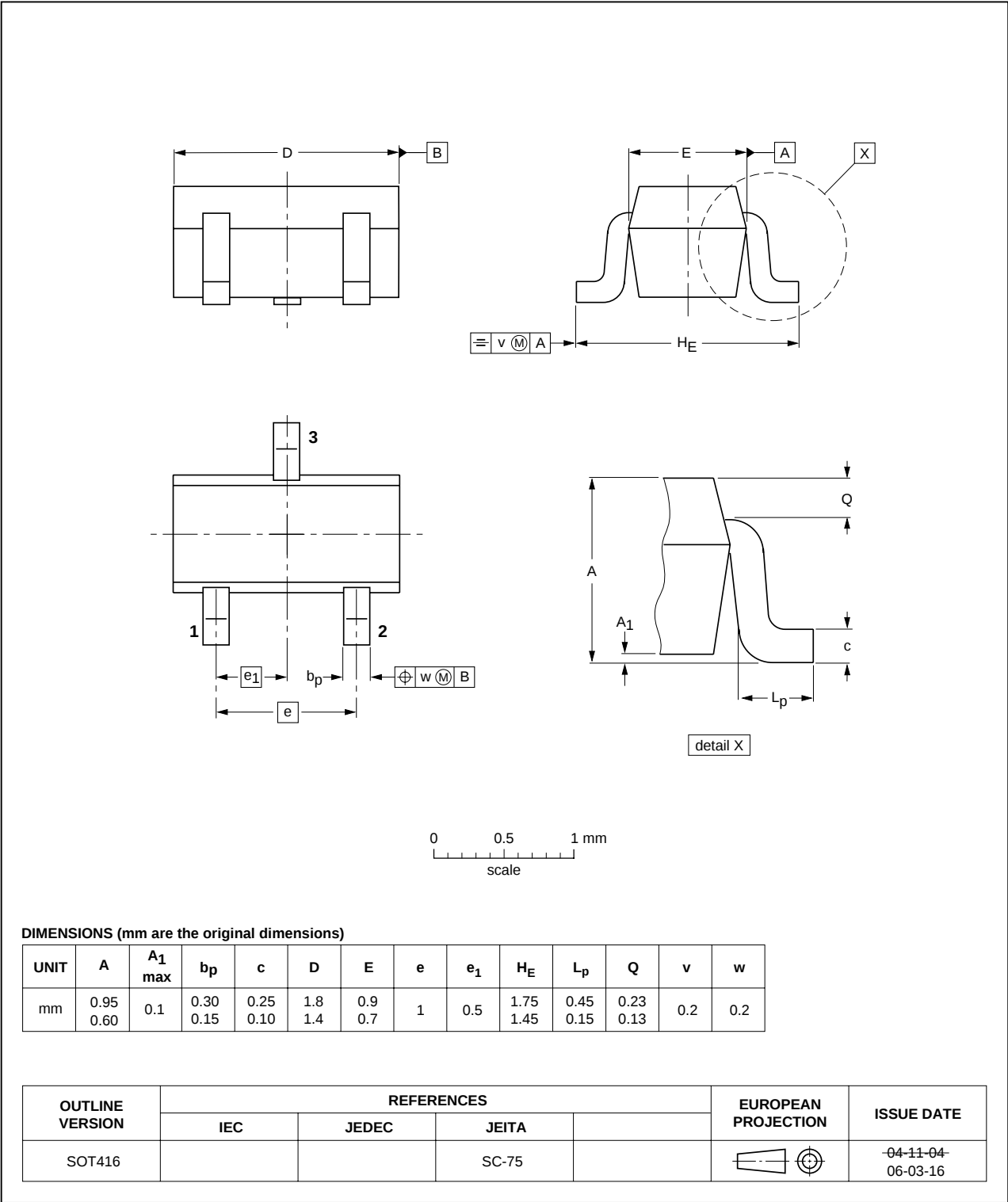


Fig 3. Package outline SOT416 (SC-75)

PDTA115T series

PNP resistor-equipped transistors; R1 = 100 kΩ, R2 = open

Plastic surface-mounted package; 3 leads

SOT346

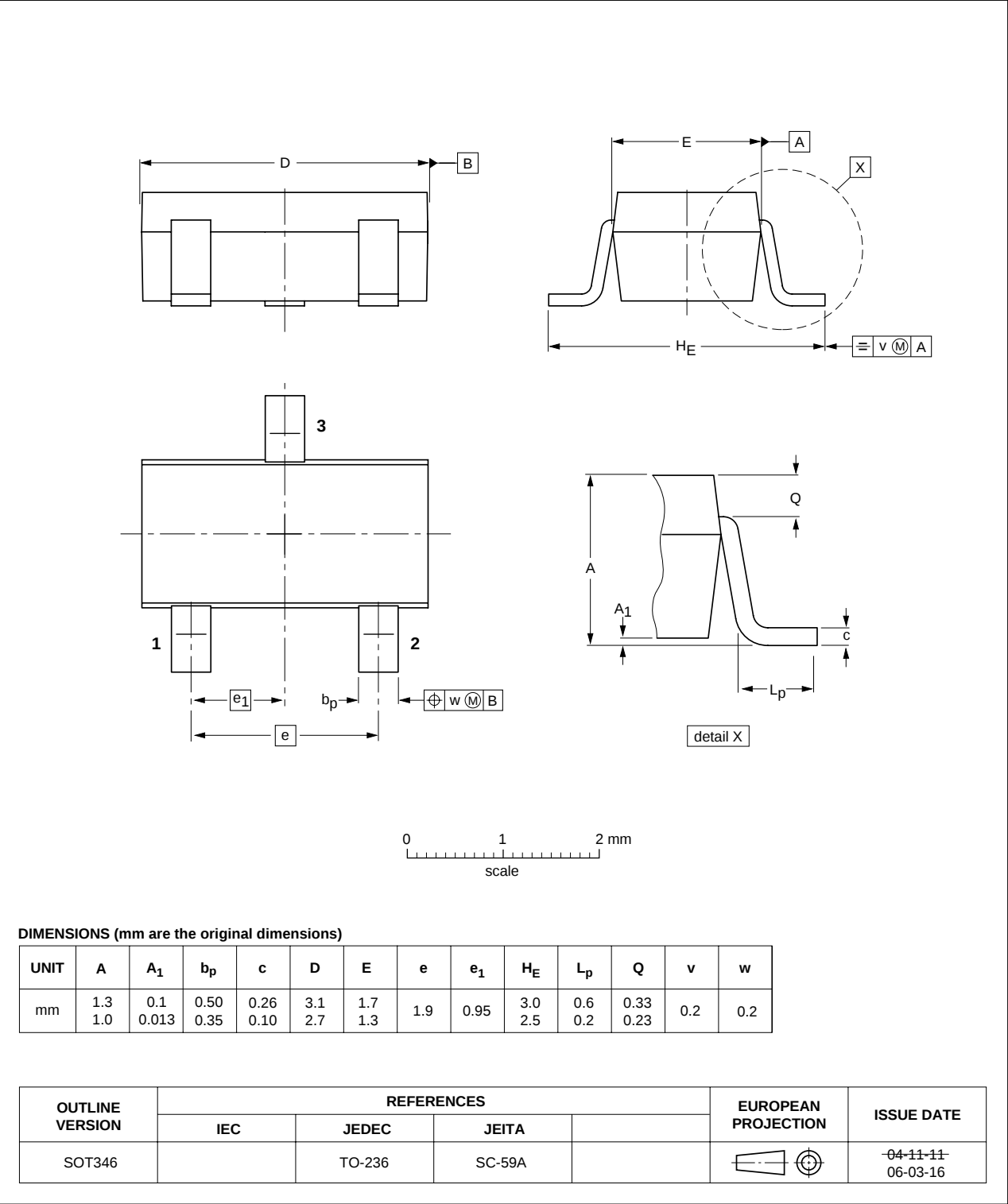


Fig 4. Package outline SOT346 (SC-59/TO-236)

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883

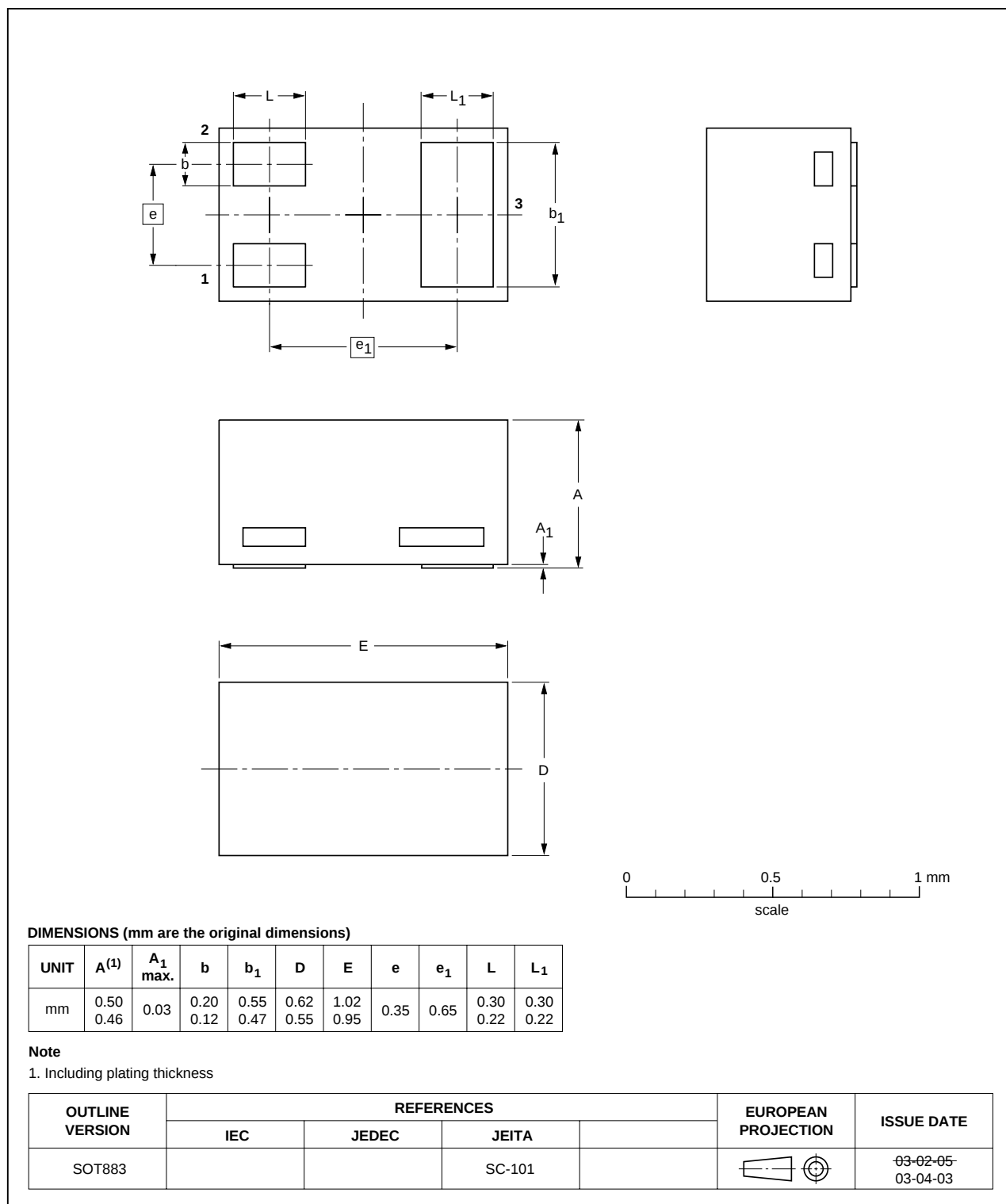


Fig 5. Package outline SOT883 (SC-101)

PDTA115T series

PNP resistor-equipped transistors; R1 = 100 kΩ, R2 = open

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

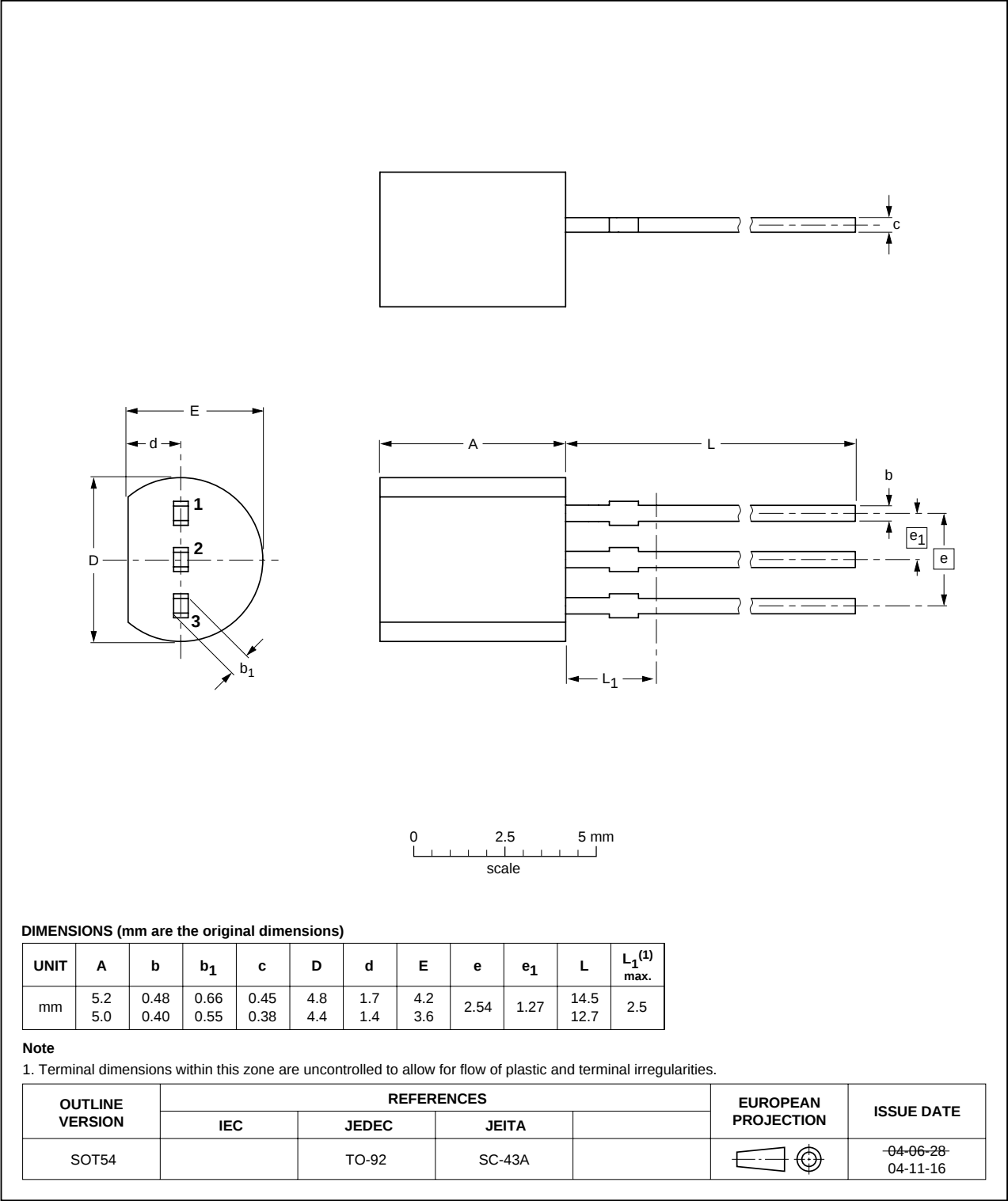
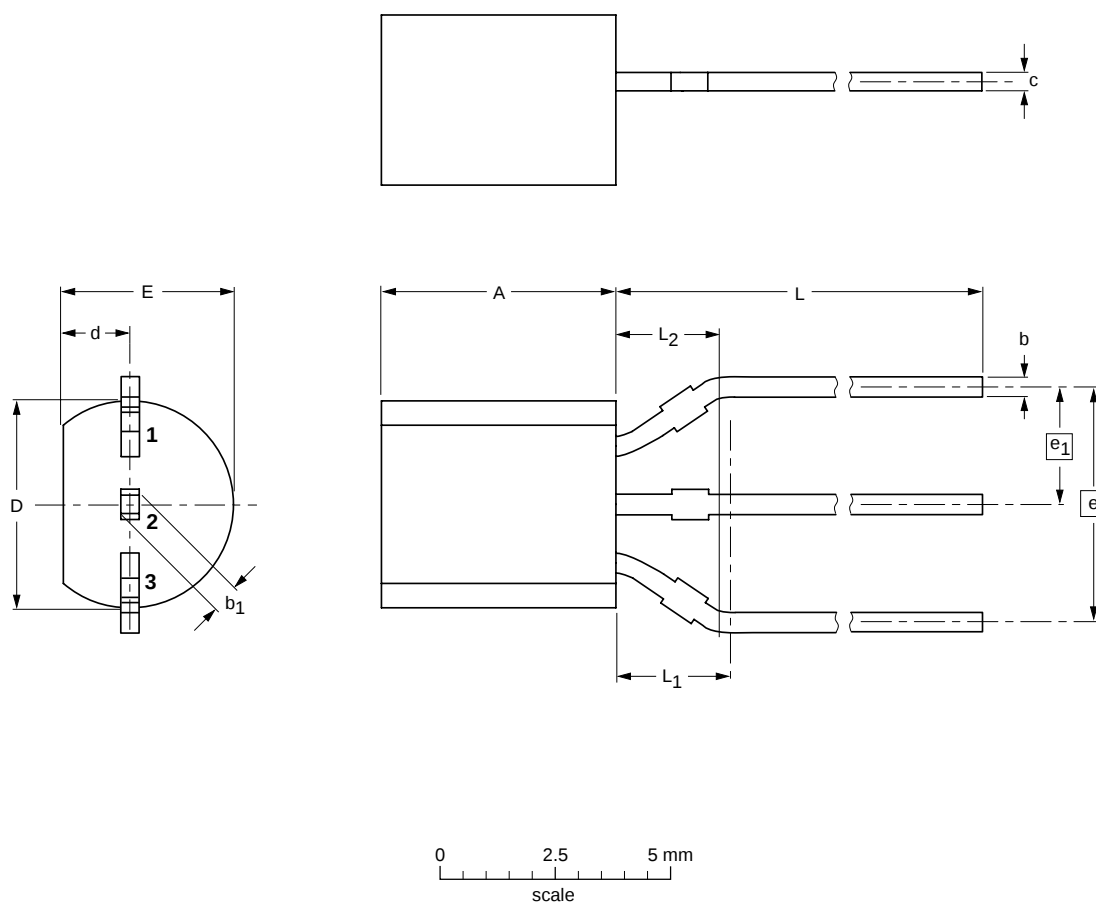


Fig. 6. Package outline SOT54 (SC-43A/TO-92)

Plastic single-ended leaded (through hole) package; 3 leads (wide pitch)

SOT54A



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.	L ₂
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	5.08	2.54	14.5 12.7	3	3 2

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54A						97-05-13 04-06-28

Fig 7. Package outline SOT54A

PDTA115T series

PNP resistor-equipped transistors; R1 = 100 kΩ, R2 = open

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant

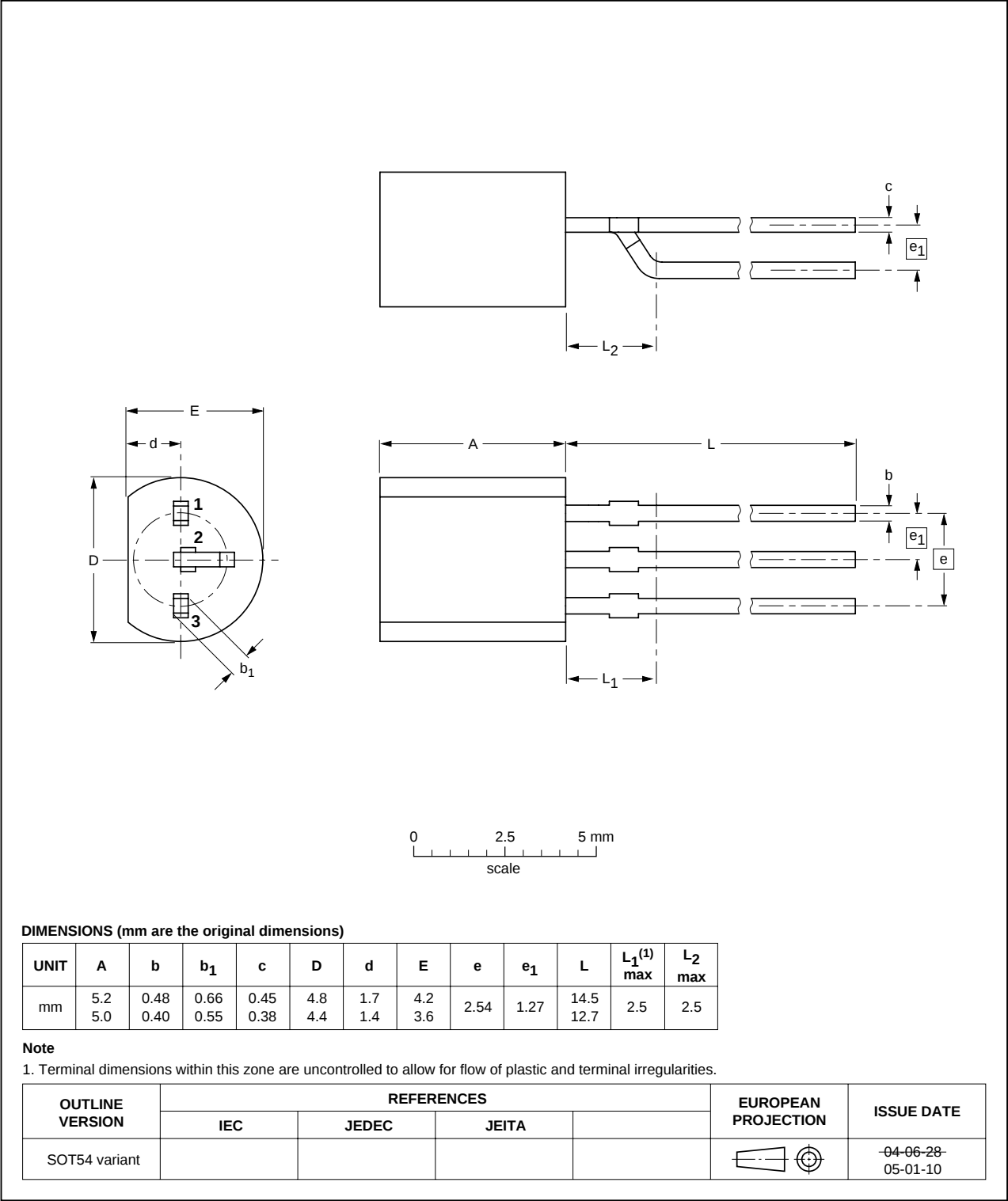
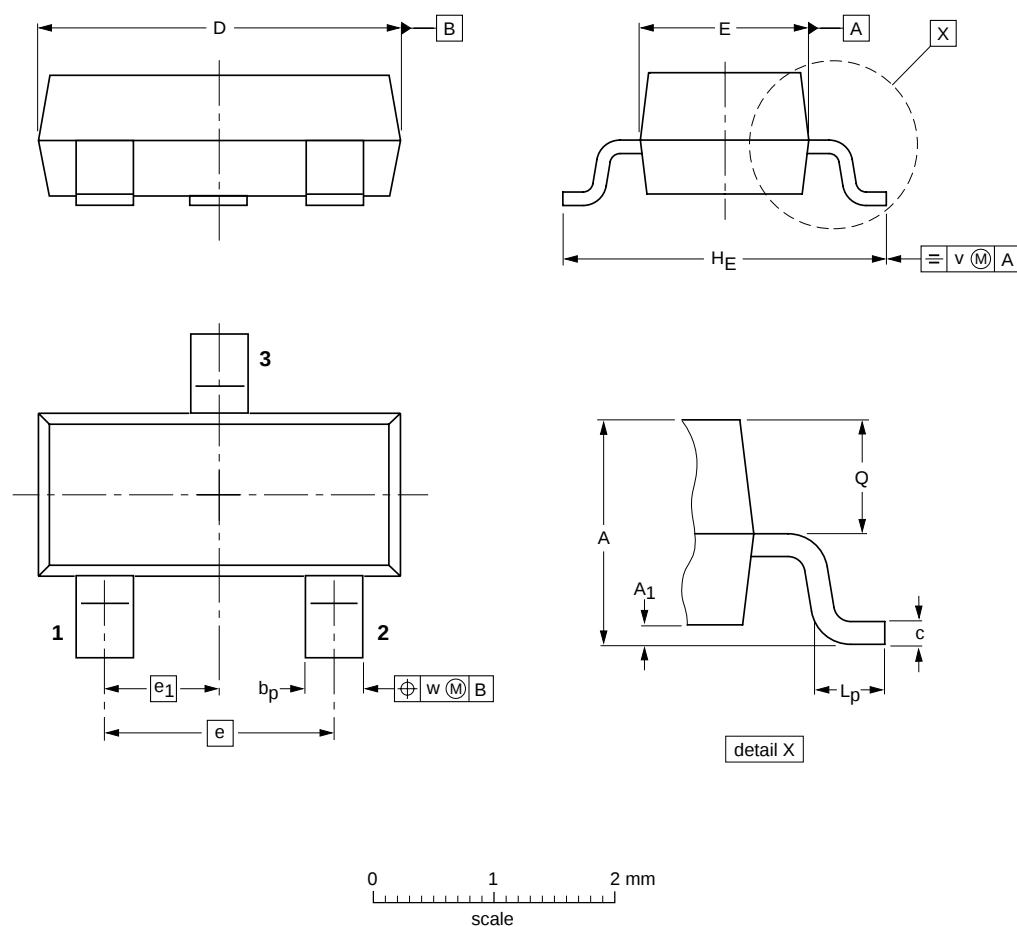


Fig 8. Package outline SOT54 variant

Plastic surface-mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max.	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

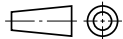
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				04-11-04 06-03-16

Fig 9. Package outline SOT23 (TO-236AB)

PDTA115T series

PNP resistor-equipped transistors; R1 = 100 kΩ, R2 = open

Plastic surface-mounted package; 3 leads

SOT323

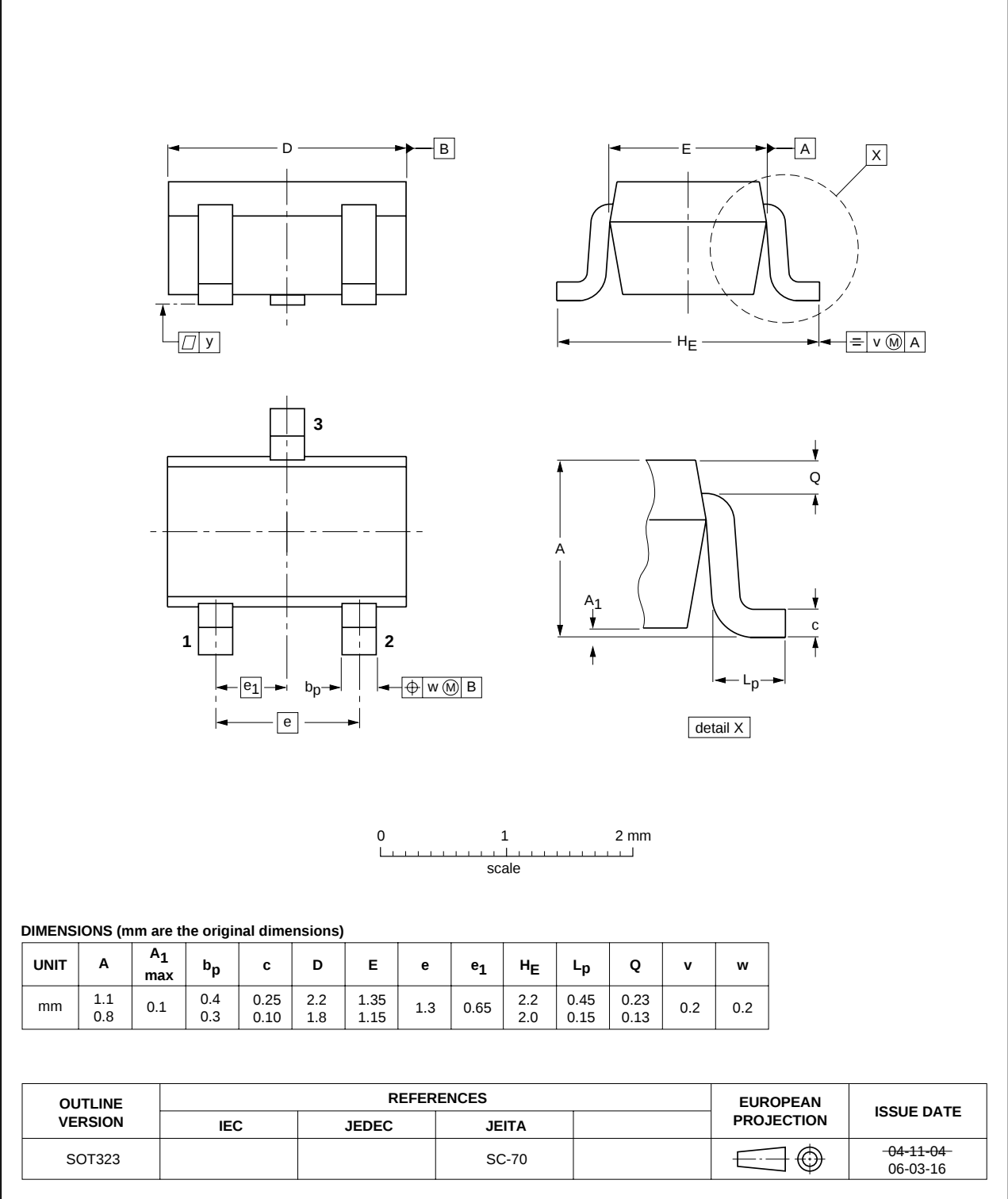


Fig 10. Package outline SOT323 (SC-70)

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code. [\[1\]](#)

Type number	Package	Description	Packing quantity		
			3000	5000	10000
PDTA115TE	SOT416	4 mm pitch, 8 mm tape and reel	-115	-	-135
PDTA115TK	SOT346	4 mm pitch, 8 mm tape and reel	-115	-	-135
PDTA115TM	SOT883	2 mm pitch, 8 mm tape and reel	-	-	-315
PDTA115TS	SOT54	bulk, straight leads	-	-412	-
	SOT54A	tape and reel, wide pitch	-	-	-116
	SOT54A	tape ammopack, wide patch	-	-	-126
	SOT54 variant	bulk, delta pinning	-	-112	-
PDTA115TT	SOT23	4 mm pitch, 8 mm tape and reel	-215	-	-235
PDTA115TU	SOT323	4 mm pitch, 8 mm tape and reel	-115	-	-135

[1] For further information and the availability of packing methods, see [Section 12](#).

10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTA115T_SER_5	20090902	Product data sheet	-	PDTA115T_SER_4
Modifications: • This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content. • Figure 3 "Package outline SOT416 (SC-75)": updated • Figure 4 "Package outline SOT346 (SC-59/TO-236)": updated • Figure 9 "Package outline SOT23 (TO-236AB)": updated • Figure 10 "Package outline SOT323 (SC-70)": updated				
PDTA115T_SER_4	20050405	Product data sheet	-	PDTA115TT_3
PDTA115TT_3	20040907	Objective data sheet	-	PDTA115TT_2
PDTA115TT_2	20040518	Objective data sheet	-	PDTA115TT_1
PDTA115TT_1	20040323	Objective data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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13. Contents

1	Product profile	1
1.1	General description.	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data.	1
2	Pinning information	2
3	Ordering information	3
4	Marking	3
5	Limiting values	4
6	Thermal characteristics	4
7	Characteristics	5
8	Package outline	6
9	Packing information	14
10	Revision history	15
11	Legal information	16
11.1	Data sheet status	16
11.2	Definitions	16
11.3	Disclaimers	16
11.4	Trademarks	16
12	Contact information	16
13	Contents	17

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