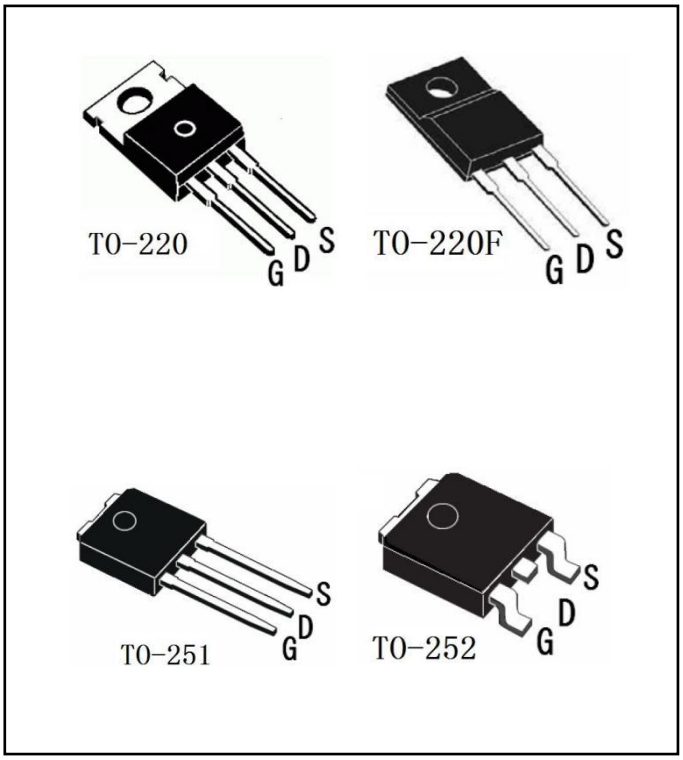
PDMP007N065

7A ,650V N-CHANNEL

POWER MOSFET



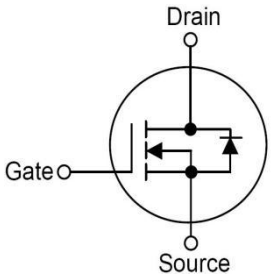
Description:

The PDP 7N65 is an N-channel enhancement mode MOSFET, The self-aligned process and improved terminal technology reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for higher efficiency and system miniaturization.

Feature:

- RDS_{ON} < 1.4Ω@V_{GS}=10V
- Low Gate Charge (typ 23nC)
- Fast Switching
- Improved ESD Capability
- Improved dv/dt Capability
- 100% Avalanche Energy Test

■ Symbol



■ Ordering Information

P/N	PACKAGE	PACKING CODE	UNIT WEIGHT(g)	MINIIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
PDMP007N065F	TO-220F	F	Approximate 1.7	50	1000	5000	TUBE
PDMP007N065A	TO-220	A	Approximate 2.0	50	1000	5000	TUBE
PDMP007N065C	TO-251	C	Approximate 0.4	75	4500	22500	TUBE
PDMP007N065D	TO-252	D	Approximate 0.4	2500	5000	25000	TAPE

■ Maximum Ratings (T_a=25℃ Unless otherwise specified)

Parameter	Symbol		Value	Unit
Drain-Source Voltage	V_{DSS}		650	V
Continues Drain Current	I_D	Tc=25℃	7*	A
		Tc=100℃	4*	
Plused Drain Current (note 1)	I_{DM}		25	A
Gate-to-Source Voltage	V_{GS}		±30	V
Single Pulsed Avalanche Energy (note 2)	E_{AS}		612	mJ
Avalanche Current (note 1)	I_{AR}		7.0	A
Repetitive Avalanche Energy (note 1)	E_{AR}		14.5	mJ
Peak Diode Recovery (note 3)	dv/dt		4.5	V/ns
Power Dissipation	P_D Tc=25℃	TO-220	147	W
		TO-220F	48	
		TO-251/TO-252	51	
Power Dissipation Derating Factor	$P_{D(DF)}$ Above 25℃	TO-220	1.18	W/℃
		TO-220F	0.26	
		TO-251/TO-252	0.39	
Operating and Storage Temperature Range	T_J, T_{STG}		150, -55 ~ +150	℃
Maximum Temperature for Soldering	T_L		300	℃

■Electrical Characteristics (Ta=25℃ Unless otherwise specified)

Off-Characteristics

Parameter	Symbol	Tests Conditions	Min	Type	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	650	-	-	V
Breakdown Voltage Temperature Coefficient	$\triangle BV_{DSS}/\triangle T_J$	I_D=250μA, referenced to 25℃	-	0.7	-	V/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V,V_{GS}=0V, T_C=25℃	-	-	1	μA
		V_{DS}=520V, T_C=125℃	-	-	10	
Gate-body leakage current, forward	I_{GSSF}	V_{DS}=0V, V_{GS} =30V	-	-	100	nA
Gate-body leakage current, reverse	I_{GSSR}	V_{DS}=0V, V_{GS} = -30V	-	-	-100	nA

On-Characteristics

Parameter	Symbol	Tests Conditions	Min	Type	Max	Unit
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D=250μA	2.0	-	4.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V , I_D=3.5A	-	1.1	1.4	Ω
Forward Transconductance	g_{fs}	V_{DS} = 40V, I_D=3.5A (note4)	-	4.0	-	S

Dynamic Characteristics

Parameter	Symbol	Tests Conditions	Min	Type	Max	Unit
Input capacitance	C_{iss}	V_{DS}=25V, V_{GS} =0V, f=1.0MHZ	-	1150	-	pF
Output capacitance	C_{oss}		-	92	-	pF
Reverse transfer capacitance	C_{rss}		-	2	-	pF

Switching Characteristics						
Parameter	**Symbol**	**Tests Conditions**	**Min**	**Type**	**Max**	**Unit**
Turn-On delay time	$t_{d(on)}$	V_{DD}=325V, I_D=7A, R_G=25Ω (note 4, 5)	-	42	-	ns
Turn-On rise time	t_r		-	19	-	ns
Turn-Off delay time	$t_{d(off)}$		-	97	-	ns
Turn-Off Fall time	t_f		-	30	-	ns
Total Gate Charge	Qg	V_{DS} =520V , I_D=7A, V_{GS} =10V (note 4, 5)	-	23	-	nC
Gate-Source charge	Qgs		-	6.5	-	nC
Gate-Drain charge	Qgd		-	10	-	nC

Drain-Source Diode Characteristics and Maximum Ratings						
Parameter	**Symbol**	**Tests Conditions**	**Min**	**Type**	**Max**	**Unit**
Maximum Continuous Drain-Source Diode Forward Current	I_S		-	-	7	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}		-	-	25	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=7A	-	-	1.4	V
Reverse recovery time	t_{rr}	V_{GS}=0V, I_S=7A dI_F/dt=100A/μs (note 4)	-	415	-	ns
Reverse recovery charge	Q_{rr}		-	4.3	-	μC

■ Thermal Characteristics （T_a=25℃ Unless otherwise specified）

Parameter	**Symbol**		**Max**	**Unit**
Thermal Resistance, Junction to Case	Rth(j-c)	TO-220	1.25	℃/W
		TO-220F	3.79	
		TO-251/TO-252	2.5	
Thermal Resistance, Junction to Ambient	Rth(j-A)	TO-220	62.5	℃/W
		TO-220F	62.5	
		TO-251/TO-252	83	

* Drain current limited by maximum junction temperature

Notes:

1: Pulse width limited by maximum junction temperature

2: L=25mH, I_{AS}=7A, V_{DD}=50V, R_G=25Ω, Starting T_J=25℃

3: I_{SD} ≤7A, di/dt ≤300A/μs, V_{DD}≤BV_{DSS}, Starting T_J=25℃

4: Pulse Test: Pulse Width ≤300μs, Duty Cycle≤2%

5: Essentially independent of operating temperature

■ Test Circuits And Waveforms

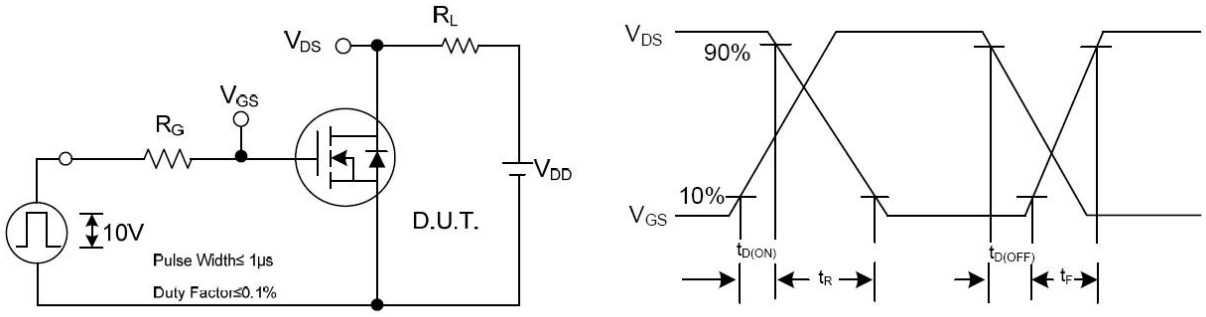


Fig.1 Resistive Switching Test Circuit & Waveforms

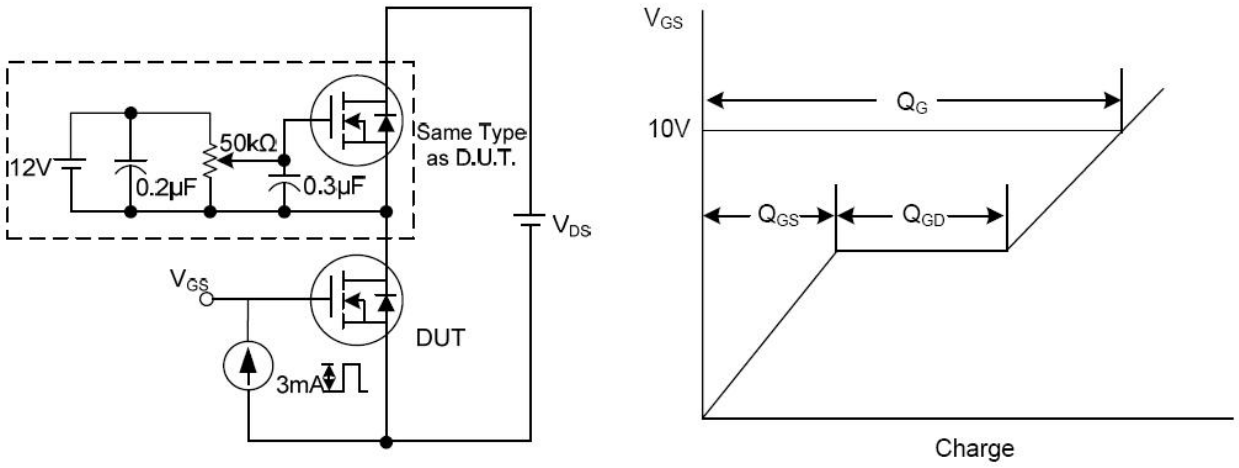


Fig.2 Gate Charge Test Circuit & Waveform

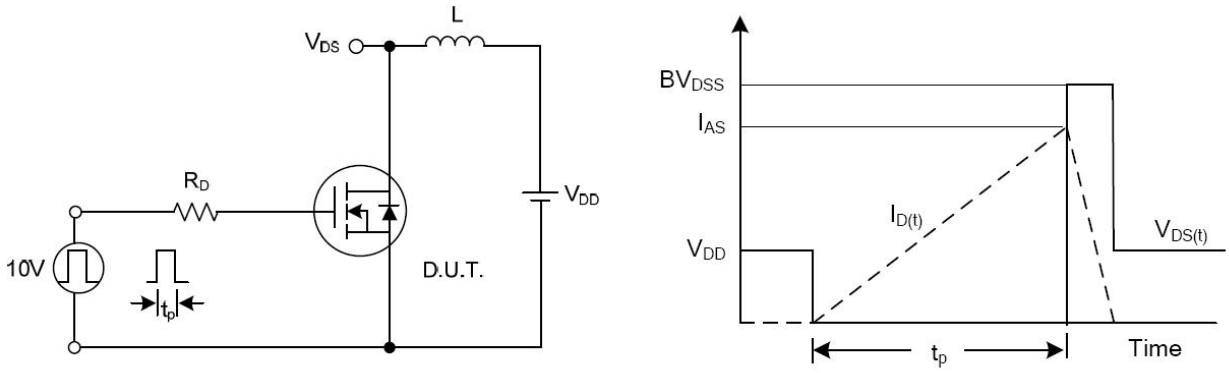


Fig.3 Unclamped Inductive Switching Test Circuit & Waveforms

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