32K x 9 Bit Fast CMOS Synchronous Static RAM with Burst Counter

Features

- ☐ Interfaces directly with the i486™, Pentium™ processors (66.6, 60, 50, 40 and 33.3 MHz)
- ☐ High speed access and cycle times
  - Clock to data valid times: 9,10,12,14 and 19 ns
  - Cycle times: 15, 16.6, 20, 25, and 30 ns
- ☐ High density 32K x 9 architecture
- ☐ Choice of 5V or 3.3V±10% output Vcc for output level compatibility
- ☐ Self-timed write cycle
- ☐ Internal burst read/write address counter
- ☐ Internal write registers (address, data, and control)
- ☐ Packages: 44 pin PLCC

Description

The PDM44259 is a high performance synchronous CMOS static RAM organized as 32,768 x 9 bits. This product which is produced in Paradigm's proprietary CMOS technology integrates a high-speed SRAM array, input registers (address, data, and control), and a clock input to achieve synchronous read and write access. The PDM44259 was designed with specific control inputs and features to support high-performance secondary cache designs for the i486 and Pentium™ architectures.

The PDM44259 internal self-timed write logic and input data and address registers eliminate the need for external write pulse generation and permit simplified self-timed write cycles triggered by the rising edge of the clock.

The internal burst address counter accepts the first cycle address from the processor, then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock.

The PDM44259 is available in a 44 pin plastic leaded chip carrier (PLCC). Multiple power and ground pins minimize effects induced by output noise. Separate power pins are provided for DQ0-DQ8 to allow user-controlled output levels of 5 volts or 3.3 volts.

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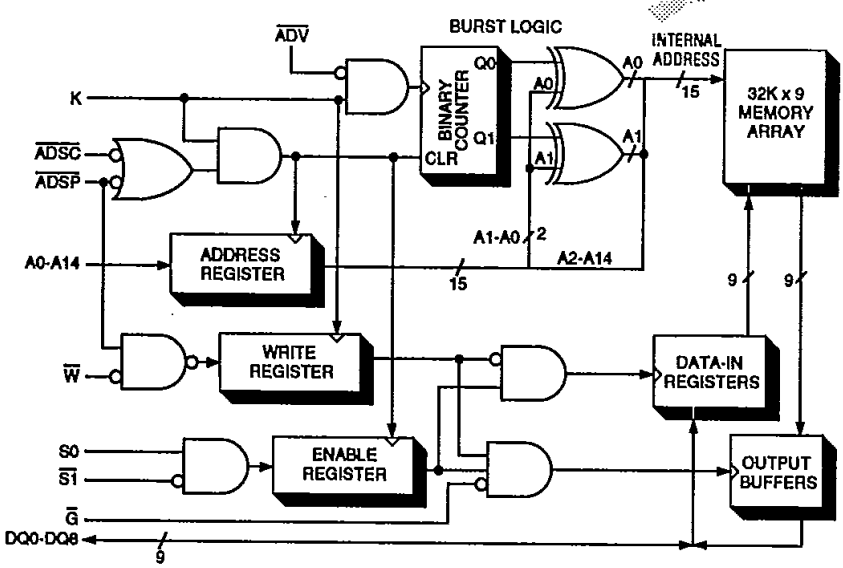
Functional Block Diagram



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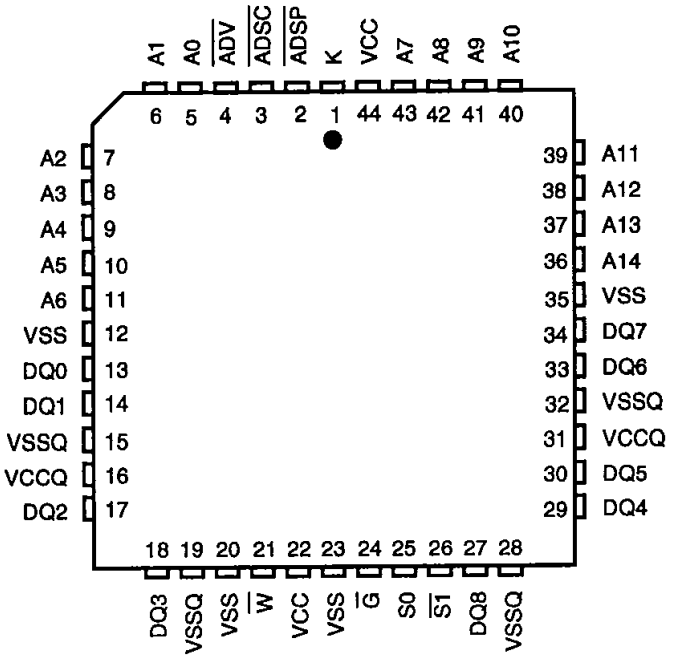
Pin Assignment



Pin Descriptions

Pin	In/Out	Description	Pin	In/Out	Description
A0-A14	I	Address	$\overline{ADV}$	I	Burst Address Advance
K	I	Clock	DQ0-DQ8	I/O	Data Input/Output
$\overline{W}$	I	Write Enable	VCC		+5 Power Suypply
$\overline{G}$	I	Output Enable	VCCQ		Output Buffer Power Supply
S0, $\overline{S1}$	I	Chip Selects	VSS		Ground
$\overline{ADSP}$	I	Address Status Processor	VSSQ		Output Buffer Ground
$\overline{ADSP}$	I	Address Status Controller			

All registers are positive-edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. chip selects (S0, $\overline{S1}$) are sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{W}$ determines whether the next cycle is a read or write cycle, and $\overline{ADV}$ controls the advance of the address counter. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**.

Synchronous Truth Table (See Notes 1, 2, 3, and 4)

S0	$\overline{ST}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	W	K	Address Used	Operation
L	X	L	X	X	X	L-H	N/A	Deselected
X	H	X	L	X	X	L-H	N/A	Deselected
H	L	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
H	L	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
H	L	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTE: 1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. S represents S0 and $\overline{ST}$. T implies $\overline{ST}$ = L and S0 = H; F implies $\overline{ST}$ = H or S0 = L.
4. Wait states are inserted by suspending burst.

Asynchronous Truth Table (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0-DQ8)
Read	H	High-Z
Write	X	High-Z -- Data In (DQ0-DQ8)
Deselected	X	High-Z

NOTE: 1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

Burst Sequence Table

External Address	A1	A0
1st Burst Address	A1	$\overline{A0}$
2nd Burst Address	$\overline{A1}$	A0
3rd Burst Address	$\overline{A1}$	$\overline{A0}$

NOTE: Upon completion, the burst wraps around to its initial state.

Absolute Maximum Ratings (1)

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage	-0.5 to +7.0	V
V_{CCQ}	Output Power Supply Voltage	-0.5 to V_{CC}	V
V_{IN}, V_{OUT}	Voltage Relative to V_{SS}	-0.5 to V_{CC} +0.5	V
I_{OUT}	Output Current (per I/O)	±20	mA
P_D	Power Dissipation (T_A = 70°C, V_{CC} = 5V, t_{KHKH} = 20 ns	1.2	W
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_A	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	-55 to +125	°C

NOTE:1.Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
V_{CCQ}	Output Supply Voltage	5V	4.5	5.0	5.5	V
		3.3V	3.0	3.3	3.6	V
V_{SS}	Reference Voltage		0	0	0	V
Commercial	Ambient Temperature Range		0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V±5%)

Symbol	Parameter	Test Conditions	PDM44259S		PDM44259L		Unit
			Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage Current	V_{CC} = MAX., V_{IN} = GND to V_{CC}	-5	5	-2	2	µA
I_{LO}	Output Leakage Current	V_{CC}= MAX., V_{OUT} = GND to V_{CC} $\overline{ST}$ = V_{IH} or S0 = V_{IL}	-5	5	-2	2	µA
V_{OL}	Output Low Voltage	I_{OL}=8mA, V_{CC} = Min. I_{OL} = 10mA, V_{CC} = Min.	-- --	0.4 0.5	-- --	0.4 0.5	V V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	--	2.4	--	V
V_{IH}	Input High Voltage		2.2	6	2.2	6	V
V_{IL}	Input Low Voltage		-0.5(1)	0.8	-0.5(1)	0.8	V

NOTE: 1. V_{IL}(min) = -3.0V for pulse width less than 20ns.

Power Supply Characteristics

Symbol	Parameter	Power	9	10	12	14	19 ns	Unit
I_{CC}	Dynamic Operating Current $\overline{ST} = V_{IL}$, $S0 = V_{IH}$ Vcc = Max., Outputs Open $f = f_{MAX} = 1/t_{RC}$	S	240	220	200	180	180	mA
		L	230	210	190	170	170	mA
I_{SB}	Standby Current (TTL Level) $\overline{ST} \geq V_{IH}$ or $S0 \leq V_{IL}$ Vcc = Max., Outputs Open $f = f_{MAX} = 1/t_{RC}$	S	90	80	70	60	60	mA
		L	80	70	60	50	50	mA

NOTES: 1. All Values are maximum guaranteed values. $V_{LC} \leq 0.2V$, $V_{HC} \geq V_{CC} - 0.2V$

Capacitance(1) (T_A = +25°C, f=1.0 Mhz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pf
C_{OUT}	Output Leakage Current	V_{OUT} = 0V	8	pf

NOTE:1. This parameter is determined by device characterization but is not production tested.

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AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

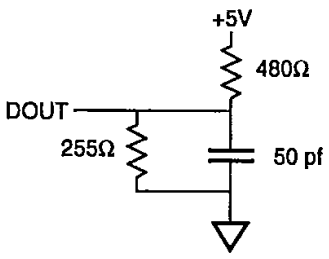


Figure 1. Output Load Equivalent

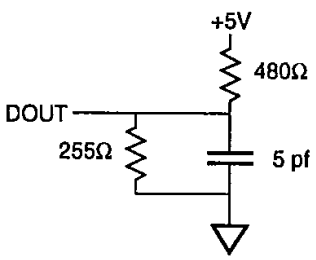


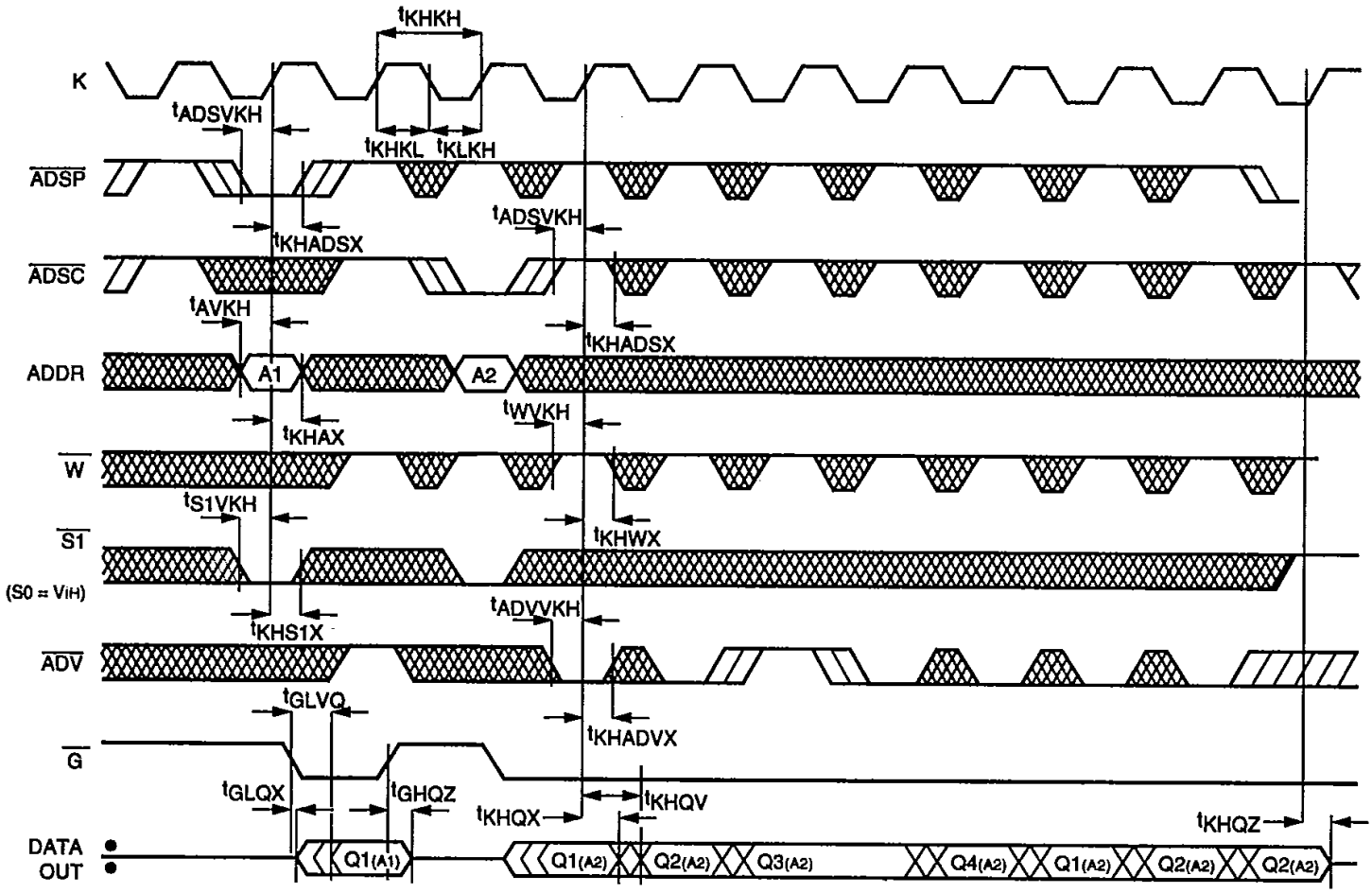
Figure 2. Output Load Equivalent
(for t_{LZ}, t_{CZ}, t_{OHZ}, t_{OLZ})
*including scope and test jig capacitor

Read/Write Cycle Timing (See Notes 1, 2, 3)

Parameter	Symbol	Alternate Symbol	-09 Min.	-09 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-14 Min.	-14 Max.	-19 Min.	-19 Max.	Units
Cycle time	t_{KHKH}	t_{CYC}	15		16.6		20		25		30		ns
Clock access time, 50 pF Load	t_{KHQV}	t_{CD}		9		10		12		14		19	ns
Clock access time, 0 pF Load	t_{KHQVO}	t_{CDO}		7.5		8.5		10		12		16	ns
Output enable to output valid	t_{GLQV}	t_{OE}		5		5		6		7		8	ns
Clock high to output active	t_{KHQX}	t_{DC}	3		3		3		3		3		ns
Output enable to output active[4]	t_{GLQX}	t_{OLZ}	0		0		0		0		0		ns
Output disable to Q high Z[4]	t_{GHQZ}	t_{OHZ}	2	5	2	5	2	6	2	7	2	8	ns
Clock High to Q high Z[4]	t_{KHQZ}	t_{CZ}		6		6		7		8		9	ns
Clock High to Q Low Z[4]	t_{KHLZ}	t_{LZ}	3		3		3		3		3		ns
Clock high pulse width	t_{KHKL}	t_{CH}	4		5		6		7		8		ns
Clock low pulse width	t_{KLKH}	t_{CL}	4		5		6		7		8		ns
Setup times for:[5] Address	t_{AVKH}	t_{AS}	2.5		2.5		3		3		3		ns
Address Status	t_{ADSVKH}	t_{SS}											
Data in	t_{DVKH}	t_{DS}											
Write	t_{WVKH}	t_{WS}											
Address Advance	t_{ADVVKH}												
Chip Select	t_{S0VKH}												
	t_{S1VKH}												
Hold times for: [5] Address	t_{KHAX}	t_{AH}	0.5		0.5		0.5		0.5		0.5		ns
Address Status	t_{KHADSX}	t_{SH}											
Data in	t_{KHDX}	t_{DH}											
Write	t_{KHWX}	t_{WH}											
Address Advance	t_{KHADVX}												
Chip Select	t_{KHS0X}												
	t_{KHS1X}												

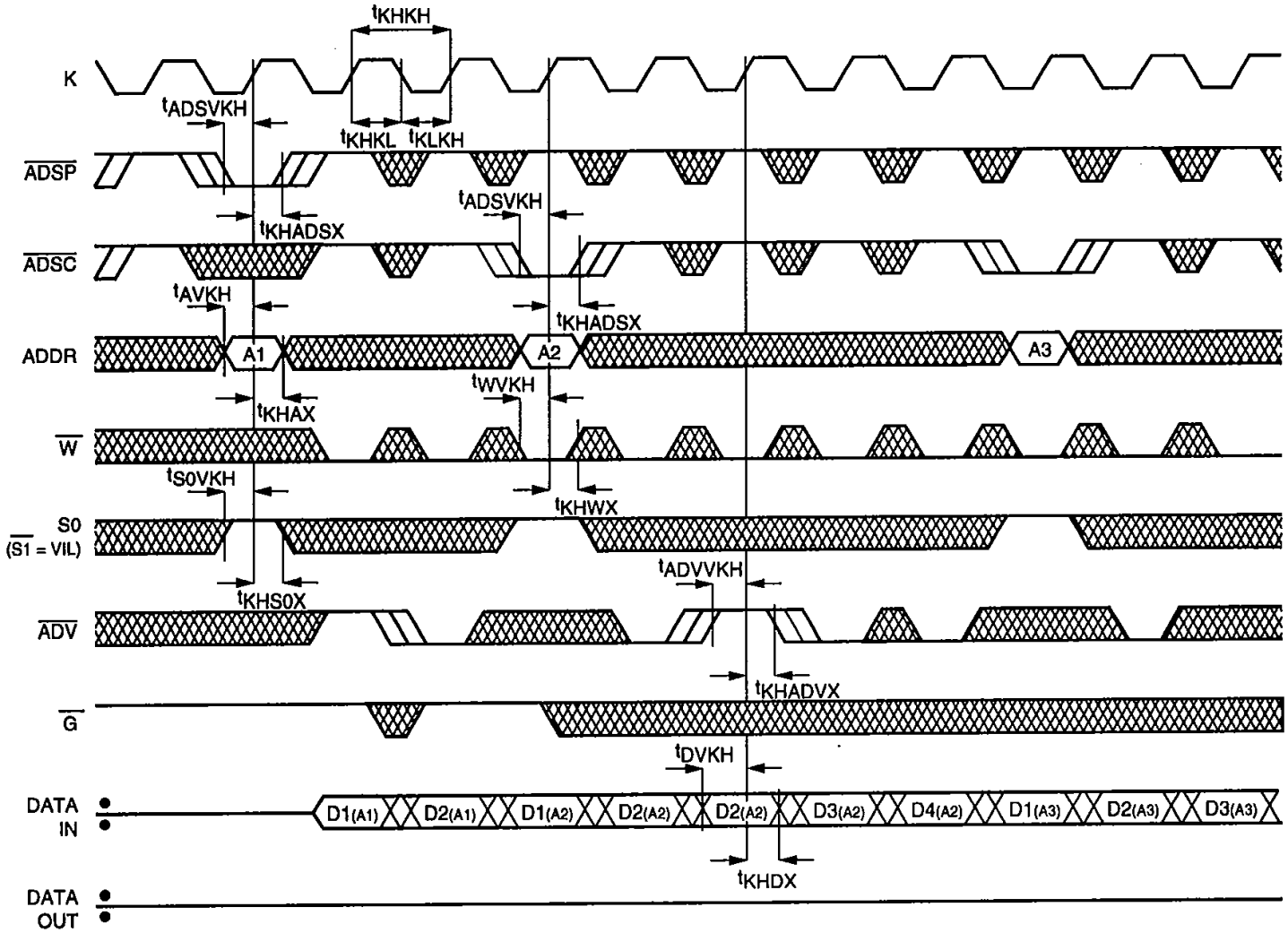
Notes:
1. A read cycle is defined by $\overline{W}$ high or $\overline{ADSP}$ low for the set-up and hold times. A write cycle is defined by $\overline{W}$ low for the set-up and hold times.
2. All read and write cycle timings are referenced from (K).
3. $\overline{G}$ is a don't care when $\overline{W}$ is sampled low.
4. Transition is measured ±200mV from steady-state voltage with load of Figure 2. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for *ALL* rising edges of clock (K). Chip Select must be true ($\overline{S1}$ low and S0 high) at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled. Timings for $\overline{S1}$ and S0 are similar.

Read Cycle



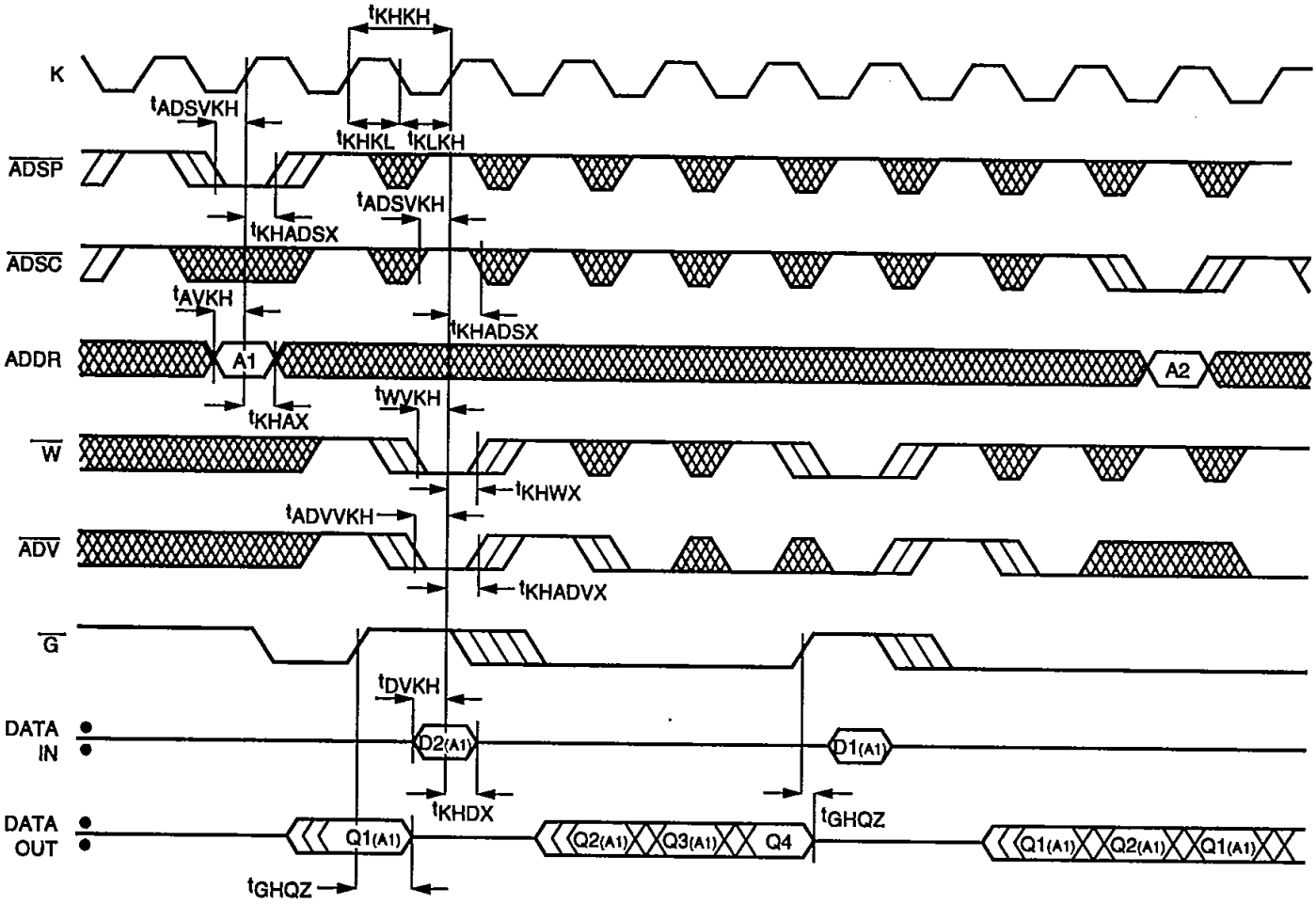
NOTE:
Q1(A2) represents the first output data from the base address A2;
Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

Write Cycle



Note: $\overline{W}$ is ignored for the first cycle when $\overline{ADSP}$ initiates the burst. $\overline{ADSP}$ active loads a new base address and forces the first cycle to be a read cycle.

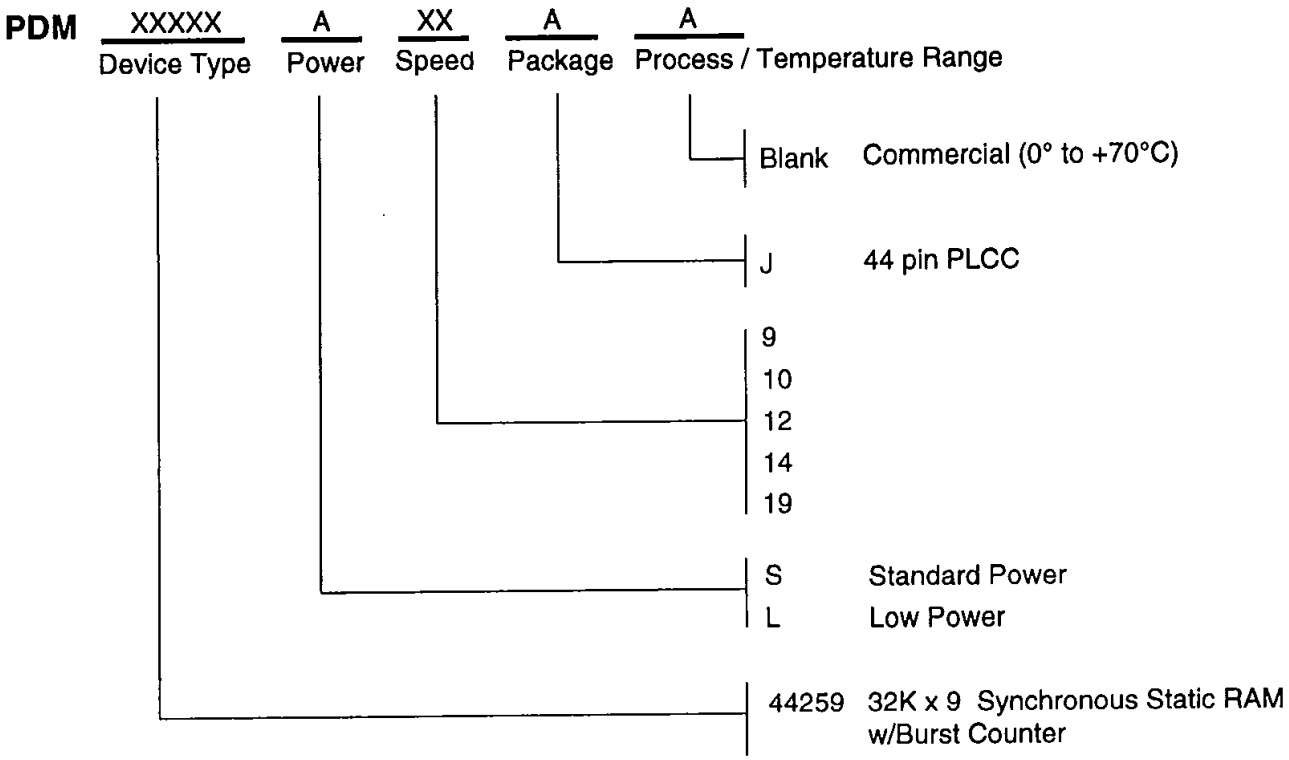
Combined Read/Write Cycle



($\overline{S1}$ = V_{IL}; S0 = V_{IH})

Note: $\overline{W}$ is ignored for the first cycle when $\overline{ADSP}$ initiates the burst. $\overline{ADSP}$ active loads a new base address and forces the first cycle to be a read cycle.

Ordering Information



Chip	Package Type
PDM44259	44 pin Plastic LCC