32K x 36 Fast CMOS Synchronous Static SRAM with Interleaved Burst Counter

Features

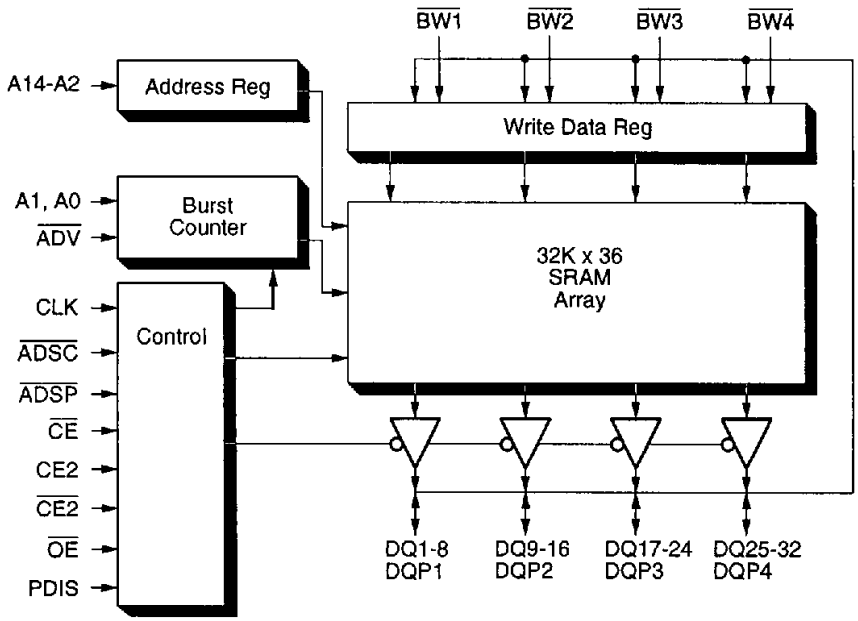
- Interfaces directly with the i486™ , Pentium™ processors (80, 66, 60, 50, 40 MHz)
- High Speed Access Times
  - Clock to data valid times: 8, 9, 10, 12, 14 ns
  - Cycle Times: 12.5, 15, 20, 25 ns
- High Density 32K x 36 Architecture
- Choice of 5V or 3V ±10% Output Vcc for output level compatability
- High Output Drive: 30 pF at Rated Taa
- Asynchronous Output Enable
- Self Timed Write Cycle
- Byte Writeable via Dual Write Strobes
- Internal interleaved burst read/write address counter
- Internal registers for Address, Data, Controls
- Packages: 100-pin TQFP

Description

The PDM44026 is a 1,179,648 bit synchronous random access memory organized as 32,768 words by 36 bits. It has burst mode capability and interface controls designed to provide high performance in secondary cache designs for i486 and Pentium™ microprocessors. Addresses, write data and all control signals except output enable are controlled through positive edge triggered registers. Write cycles are self timed and are also initiated by the rising edge of the clock. Controls are provided to allow burst reads and writes of up to four words in length. A two-bit burst address counter controls the two least significant bits of the address during burst reads and writes. The burst address counter uses the 2-bit counting scheme required by the i486 and Pentium™ microprocessors. Individual write strobes provide byte write for the four 9-bit bytes of data. An asynchronous output enable simplifies interface to high speed buses. Separate output Vcc pins provide user controlled output levels of 5V or 3.3V, for 3.3V TTL compatibility.

6

Functional Block Diagram



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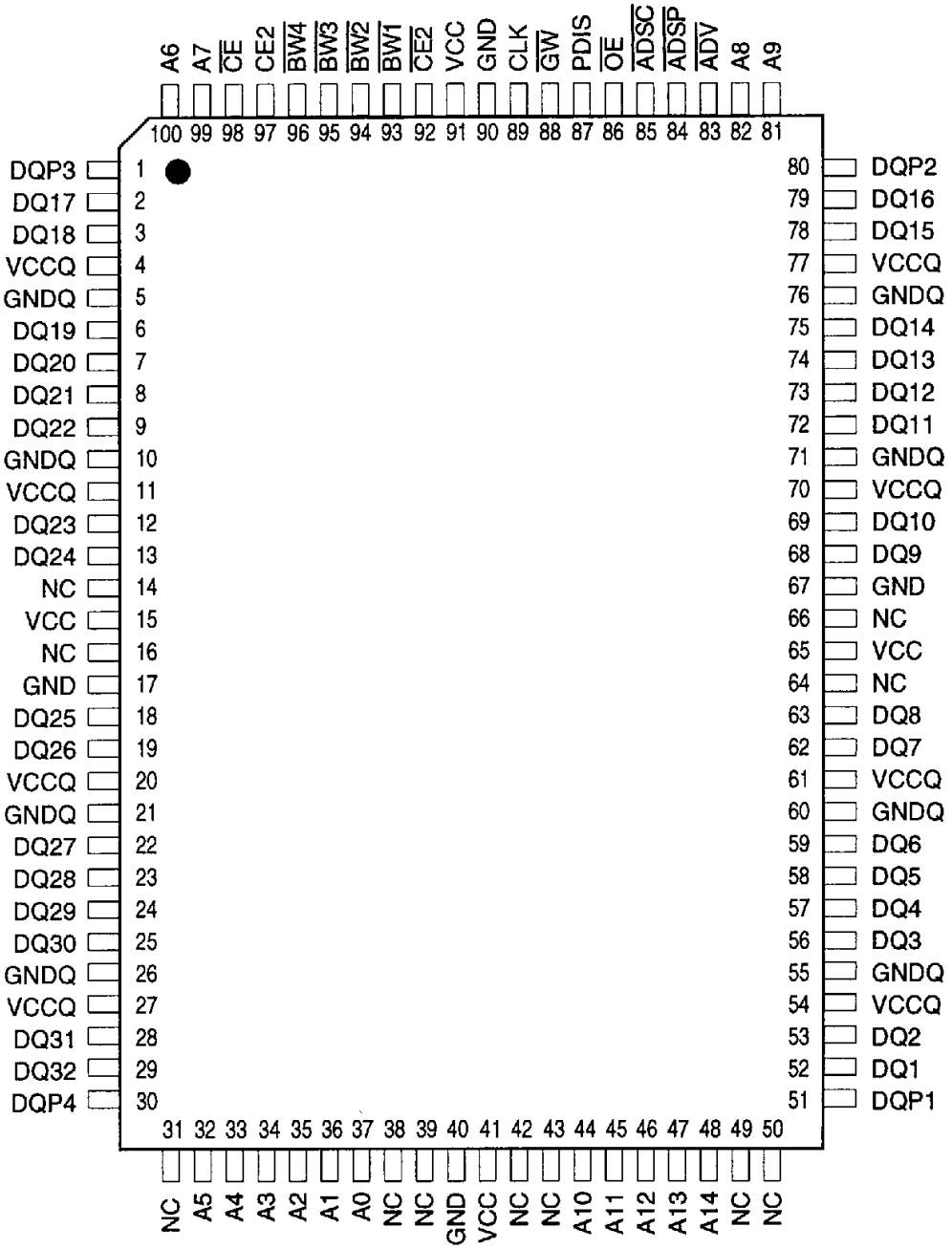
Pin Assignment



Pinout

Name	I/O	Description	Name	I/O	Description
A14-A2	I	Address Inputs A14-A2	$\overline{CE}$, CE2, $\overline{CE2}$	I	Chip EnableS
A1, A0	I	Address Inputs A1 & A0	$\overline{BW1}$-$\overline{BW4}$	I	Byte Write Enables
DQ1-DQ32	I/O	Read/Write Data	$\overline{OE}$	I	Output Enable
DQP1-DQP4	I/O	Read/Write Data	CLK	I	Clock
PDIS	I	Parity Disable (disables DQP1-4)	VCC	—	Array Power (+5V)
$\overline{ADV}$	I	Burst Counter Advance	VCCQ	—	Output Power for DQ's (+3.3V or +5V)
$\overline{ADSC}$	I	Controller Address Status	GND	—	Array Ground
$\overline{ADSP}$	I	Processor Address Status	GNDQ	—	Output Ground for DQ's

Asynchronous Truth Table

Operation	$\overline{OE}$	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z: Write Data In
Deselected	X	High-Z

NOTE: 1. X means Don't Care.
2. For a write operation following a read operation, $\overline{OE}$ must be high before the input data required setup time and held high through the input data hold time.

Burst Sequence Table

Sequence	A14-A2	A1	A0
Start Address	XXXX	A1	A0
1st Burst Address	XXXX	A1	$\overline{A0}$
2nd Burst Address	XXXX	$\overline{A1}$	A0
3rd Burst Address	XXXX	$\overline{A1}$	$\overline{A0}$

6

Synchronous Truth Table (See Notes 1 through 4)

$\overline{CE}$, CE2, $\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{BW1}$-$\overline{BW4}$	CLK	Address	Operation
HXX, XLX or XXH	X	L	X	X	↑	N/A	Deselected
LHL	L	X	X	X	↑	External	Read Cycle, Begin Burst
LHL	H	L	X	L	↑	External	Write Cycle, Begin Burst
LHL	H	L	X	H	↑	External	Read Cycle, Begin Burst
X	H	H	L	L	↑	Next	Write Cycle, Continue Burst
X	H	H	L	H	↑	Next	Read Cycle, Continue Burst
X	H	H	H	L	↑	Current	Write Cycle, Suspend Burst
X	H	H	H	H	↑	Current	Read Cycle, Suspend Burst
HXX	X	H	L	L	↑	Next	Write Cycle, Continue Burst
HXX	X	H	L	H	↑	Next	Read Cycle, Continue Burst
HXX	X	H	H	L	↑	Current	Write Cycle, Suspend Burst
HXX	X	H	H	H	↑	Current	Read Cycle, Suspend Burst

NOTE: 1. X means Don't Care.
2. All inputs except $\overline{OE}$ must meet setup and hold times relative low-to-high transition of clock, CLK .
3. Wait states are inserted by suspending burst.
4. $\overline{ADSP}$ is gated by $\overline{CE}$. Both $\overline{ADSP}$ and $\overline{CE}$ must be valid for $\overline{ADSP}$ to load the address register and force a read.

Burst Mode Operation

This is a synchronous part. All activities are initiated by the positive, low-to-high edge of the clock (CLK). This part can perform burst reads and writes with burst lengths of up to 4 words. The 4 word burst is created by using a burst counter to drive the two least significant bits of the internal RAM address. The burst counter is loaded at the start of the burst and is incremented for each word of the burst. The burst counter uses a modified binary sequence compatible with the cache line burst reload sequence of i486 microprocessors. This sequence is given in the Burst Sequence Table.

Burst transfers are initiated by the $\overline{ADSC}$ or $\overline{ADSP}$ signals. When the $\overline{ADSP}$ and $\overline{CE}$ signals are sampled low, a read cycle is started (independent of $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$ and $\overline{ADSC}$), and prior burst activity is terminated. $\overline{ADSP}$ is gated by $\overline{CE}$, so both must be active for $\overline{ADSP}$ to load the address register and to initiate a read cycle. The address and the chip enable input ($\overline{CE}$) are sampled by the same edge that samples $\overline{ADSP}$. Read data is valid at the output after the specified delay from the clock edge.

When $\overline{ADSC}$ is sampled low and $\overline{ADSP}$ is sampled high, a read or write cycle is started depending on the state of $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$. If $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ and $\overline{BW4}$ are all sampled high, a read cycle is started, as described above. If $\overline{BW1}$, $\overline{BW2}$, $\overline{BW}$, or $\overline{BW4}$ is sampled low, a write cycle is begun. The address, write data, and the chip enable inputs ($\overline{CE}$, CE2 and $\overline{CE2}$) are sampled by the same edge that samples $\overline{ADSC}$ and $\overline{BW1}$ - $\overline{BW4}$. The $\overline{ADV}$ line is held high for this clock edge to maintain the correct address for the internal write operation which will follow this second clock edge.

After the first cycle of the write burst, The state of $\overline{BW1}$ - $\overline{BW4}$ determines whether the next cycle is a read or write cycle, and $\overline{ADV}$ controls the advance of the address counter. The $\overline{ADV}$ signal advances the address counter. This increments the address to the next available RAM address. You write the next word in the burst by taking $\overline{ADV}$ low and presenting the write data at the positive edge of the clock. If $\overline{ADV}$ is sampled low, the burst counter advances and the write data (which is sampled by the same clock) is written into the internal RAM during the time following the clock edge.

Absolute Maximum Ratings

Symbol	Rating	Com'l.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Description		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
V_{CCQ}		5V	4.5	5.0	5.5	V
		3.3V	3.0	3.3	3.6	V
GND	Supply Voltage		0	0	0	V
Industrial	Ambient Temperature		–40	25	85	°C
Commercial	Ambient Temperature		0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V±5%, All Temperature Ranges)

Symbol	Description	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = MAX., V_{IN} = GND to V_{CC}	—	1	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = MAX., V_{OUT} = GND to V_{CC}	—	1	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8 mA	0	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4 mA	2.4	V_{CCQ}	V
V_{IH}	Input HIGH Voltage		2.2	6	V
V_{IL}	Input LOW Voltage (1)		–0.5	0.8	V

NOTE: 1. Undershoots to –1.5 for 10 ns are allowed once per cycle.

Power Supply Characteristics

Symbol	Description	Test Conditions		-8 ns	-9 ns	-10 ns	-12 ns	-14 ns	Unit
I_{CC1}	Active Supply Current: Outputs Open	V_{CC} = Max., Inputs @ 0.0V or 3.0V F = $1/T_{CYC}$ on Rclk & Wclk	Com'l.	460	440	420	400	380	mA
I_{SB}	Standby Current: Outputs Open	V_{CC} = Max., Inputs @ 0.0V or 3.0V F = $1/T_{CYC}$, CE = V_{IH}	Com'l.	110	100	90	80	70	mA

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Leakage Current	V_{OUT} = 0V	8	pF

NOTES: 1. Characterized values, not currently tested.
2. With output deselected.

6

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input rise and fall times	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output Load	See Figures 1 and 2

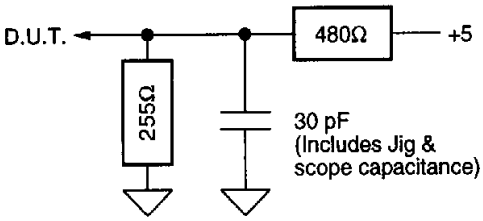


Figure 1a. Output Load

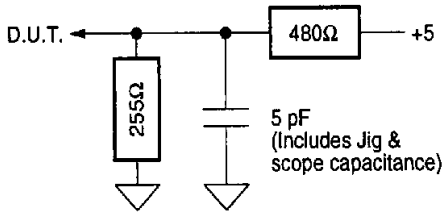


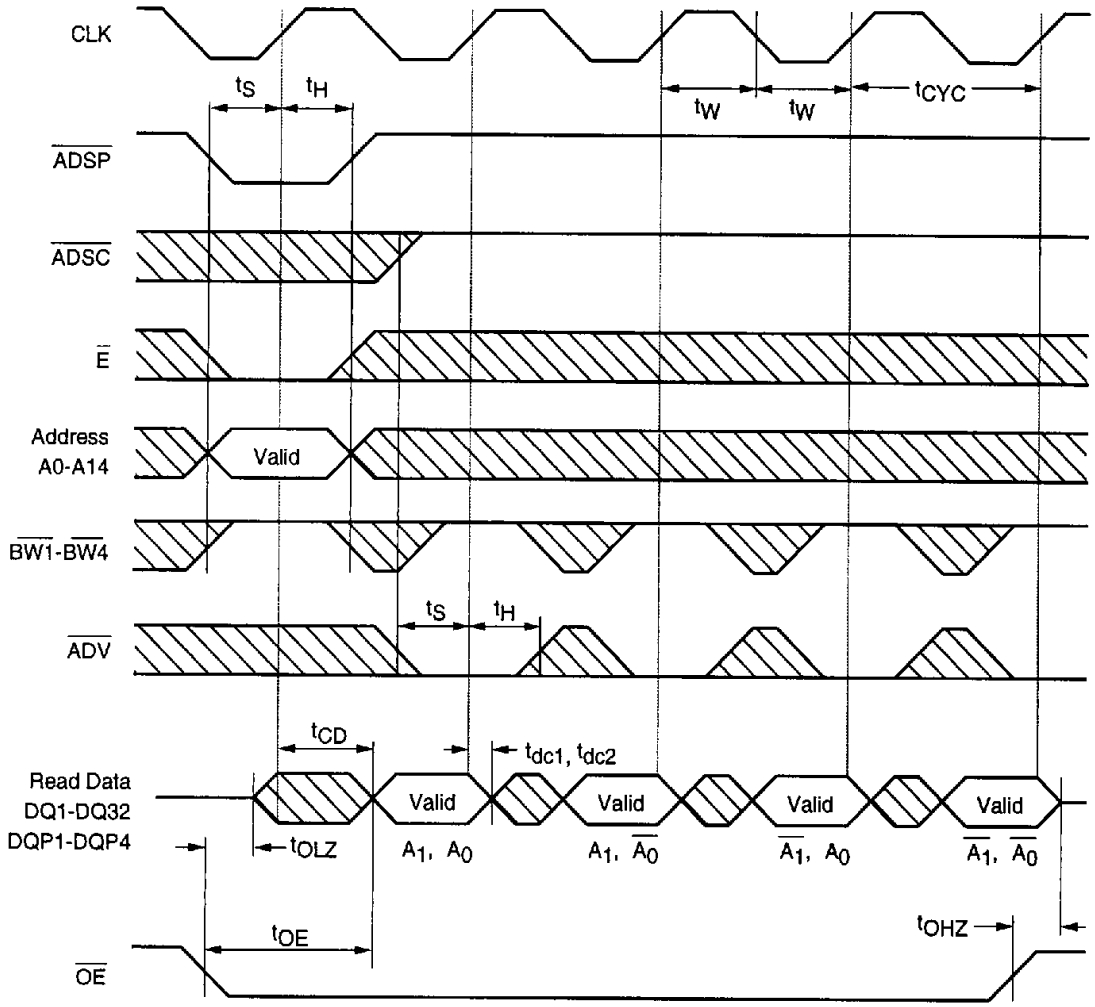
Figure 1b. Output Disable Timing Load

AC Electrical Characteristics (V_{CC} = 5V ± 5%, All Temperature Ranges)

Parameter	Symbol	-8	-9	-10	-12	-14	Type	Units	Notes
Clock Cycle time	t_{CYC}	13	15	15	20	25	Min.	ns	
Clock to Data Valid (Std Load)	t_{CD}	8	9	10	12	14	Max.	ns	5
Clock to Data Valid (0 pF Load)	t_{CD0}	7	8	9	11	13	Min.	ns	
Output Enable	t_{OE}	5	5	5	6	7	Max.	ns	
Clock to Data Low-Z	t_{dc1}	3	3	3	3	3	Min.	ns	
Clock to Data Hold Time	t_{dc2}	3	3	3	3	3	Min.	ns	
OE to Output Low-Z(1)	t_{OLZ}	0	0	0	0	0	Min.	ns	1
OE to Output High-Z(1)	t_{OHZ}	2	2	2	2	2	Min.	ns	1, 6
		5	5	5	6	7	Max.	ns	1, 6
Clock to Data High-Z	t_{CZ}	6	6	6	7	8	Max.	ns	1, 6
Clock High/Low	t_W	4	4	5	6	7	Min.	ns	
Setup Time	t_S	2.5	2.5	2.5	3	3	Min.	ns	7
Hold Time	t_H	0.5	0.5	0.5	0.5	0.5	Min.	ns	7

NOTES: 1. Values characterized and guaranteed by design, not currently tested.
2. A read cycle is defined by $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ and $\overline{BW4}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{BW1}$, $\overline{BW2}$,$\overline{BW3}$ or $\overline{BW4}$ low and $\overline{ADSP}$ high for the set up and hold times.
3. All read and write cycle timings are referenced from CLK or $\overline{OE}$.
4. $\overline{OE}$ is a "don't care" when $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 external bus cycles.
6. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{CHZ} max is less than t_{CLZ} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ALL rising edges of CLK whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

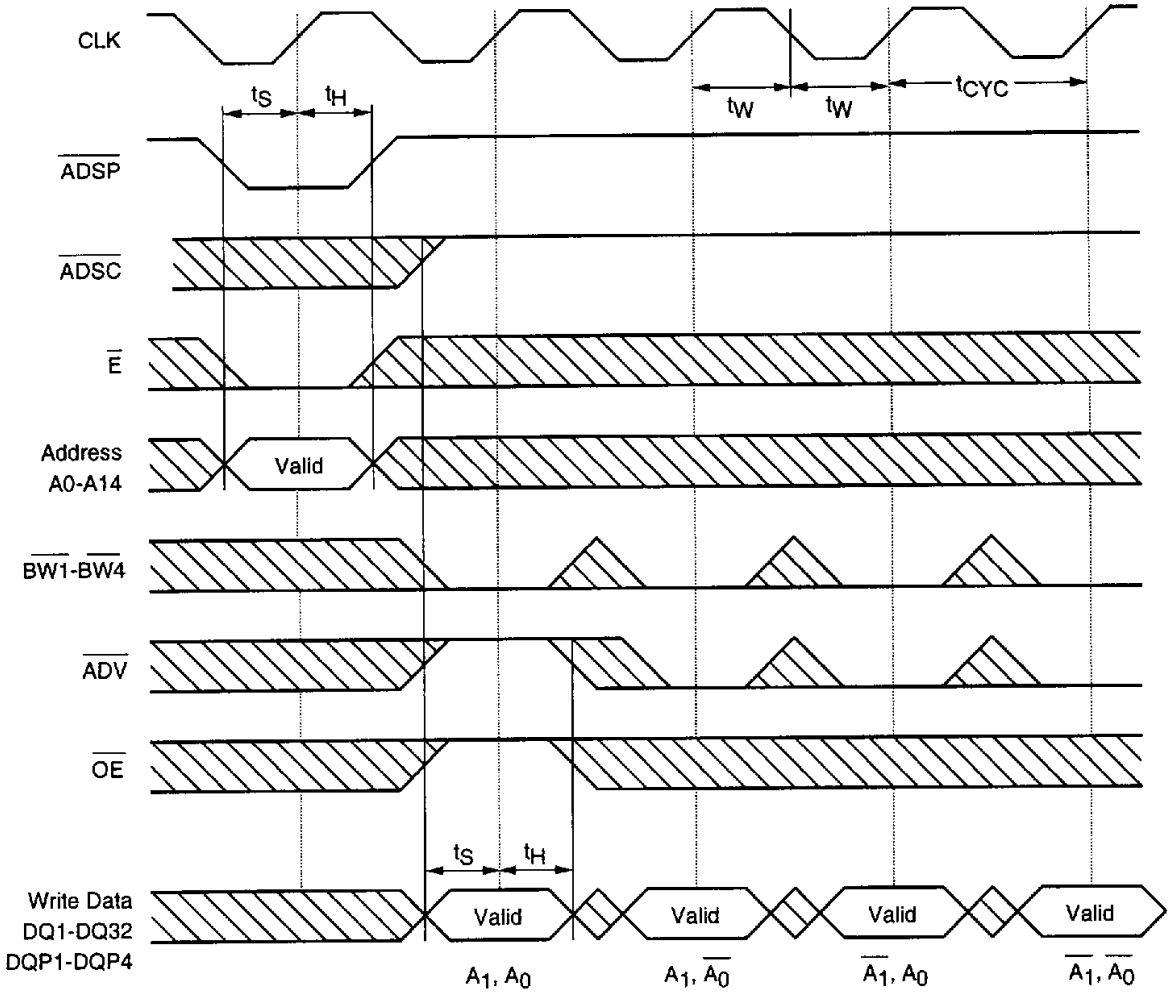
ADSP Read Timing Diagram



NOTES:

1. $\overline{E}$ is the AND of $\overline{CE}$, CE2 and $\overline{CE2}$ valid.

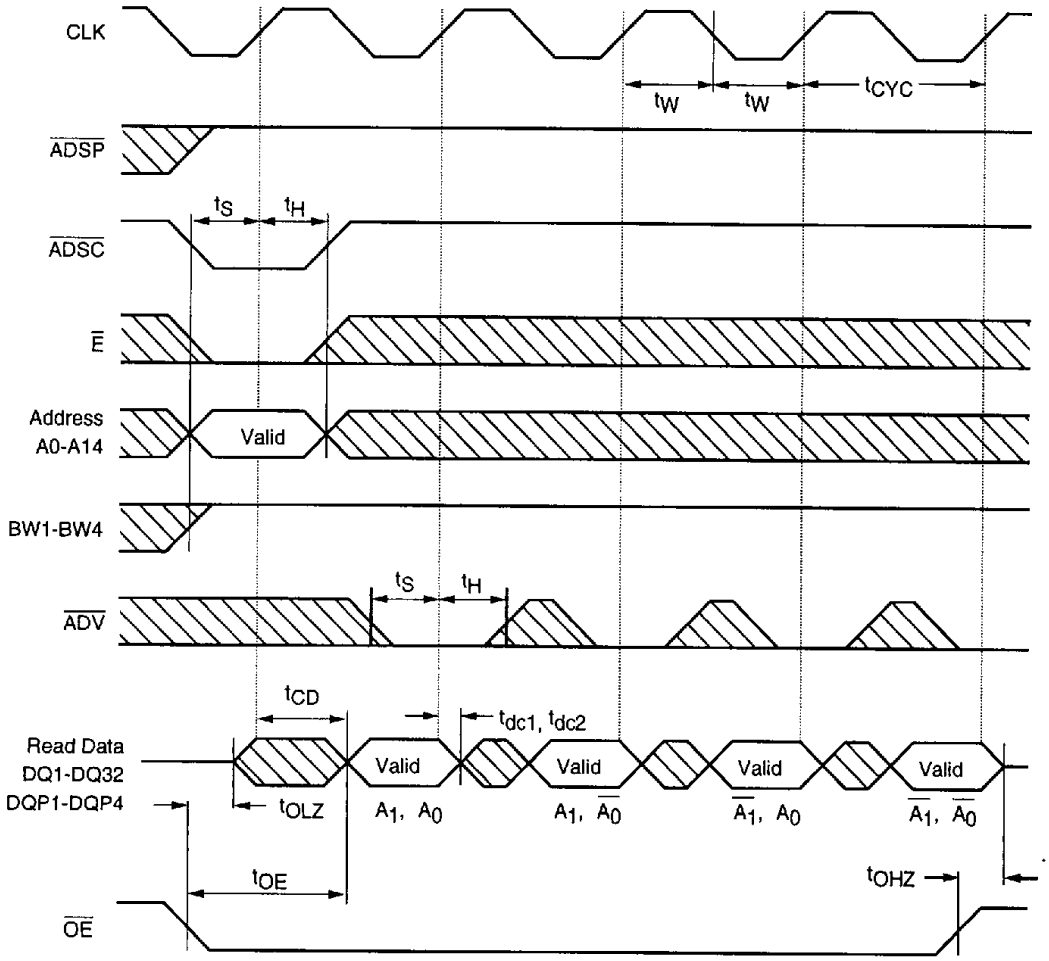
ADSP Write Timing Diagram



NOTES:

1. $\overline{E}$ is the AND of $\overline{CE}$, CE2 and $\overline{CE2}$ valid.
2. $\overline{UW}$ and $\overline{LW}$ are ignored for the first cycle when $\overline{ADSP}$ initiates the burst. $\overline{ADSP}$ active loads a new address into the address counter and forces the first cycle to be a read cycle.

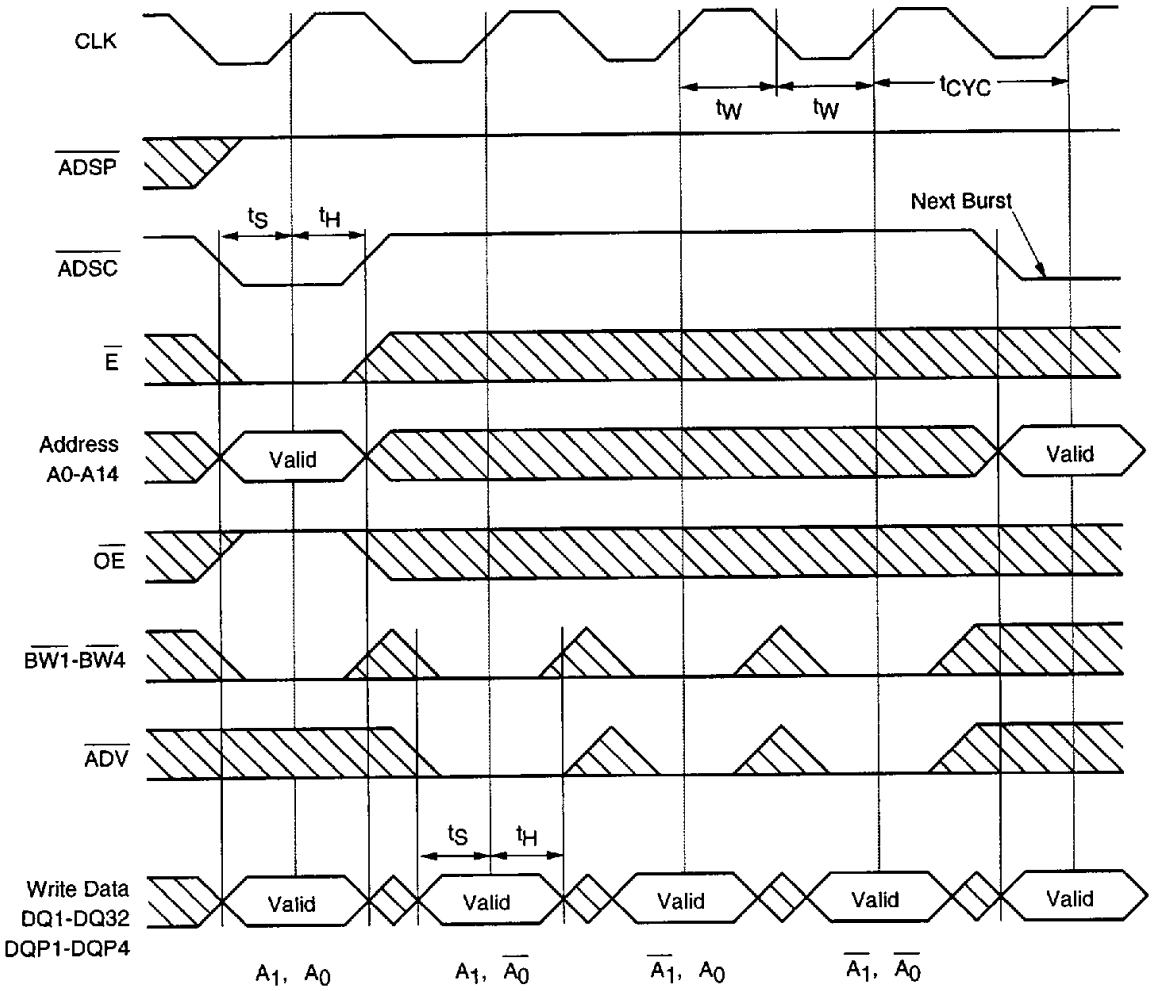
ADSC Read Timing Diagrams



NOTES:

1. $\overline{E}$ is the AND of $\overline{CE}$, CE2 and $\overline{CE2}$ valid.

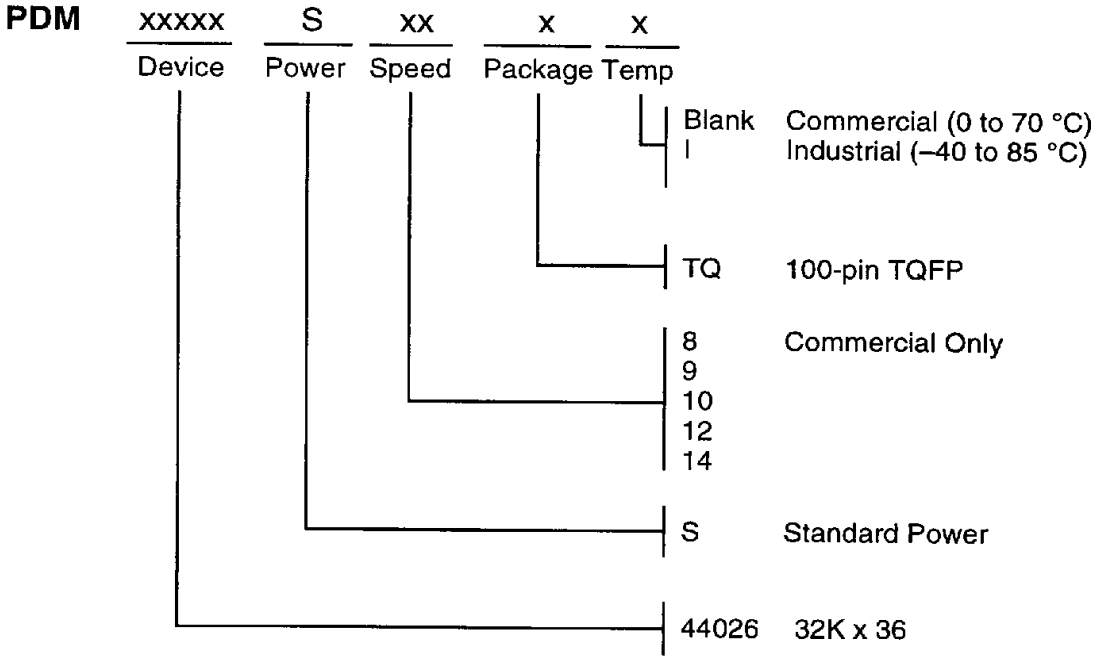
ADSC Write Timing Diagram



NOTES:

1. $\overline{E}$ is the AND of $\overline{CE}$, CE2 and $\overline{CE2}$ valid.
2. $\overline{UW}$ and $\overline{LW}$ are ignored for the first cycle when $\overline{ADSP}$ initiates the burst. $\overline{ADSP}$ active loads a new address into the address counter and forces the first cycle to be a read cycle.

Ordering Information



Chip	Description
PDM44026	100-pin TQFP