

**PD70100/PD70200**  
**Datasheet**  
**IEEE 802.3af/at PD Front End IC**



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# 1 Revision History

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## 1.1 Revision 3.0

Revision 3.0 was published in January 2018. The following is a summary of changes in revision 3.0 of this document.

- The formatting of this document was updated to the latest template.
- MSL level updated.
- Part marking was updated. For more information, see [Ordering Information \(see page 15\)](#).
- [Absolute Maximum Ratings \(see page 8\)](#) updated.

## 1.2 Revision 2.0

Revision 2.0 was published in October 2015. In revision 2.0 of this document, the IC part number was updated from PD70100A to PD70100 (PDN 152044).

## 1.3 Revision 1.1

Revision 1.1 was published in October 2014. In revision 1.1 of this document, the description of Pin 2 was updated.

## 1.4 Revision 1.0

Revision 1.0 was published in March 2012. The following is a summary of changes in revision 1.0 of this document.

- The document address footer was updated.
- Characteristics were updated.

## 1.5 Revision 0.6

Revision 0.6 was published in July 2011. In revision 0.6 of this document, the specification was updated.

## 1.6 Revision 0.5

Revision 0.5 was published in January 2011. In revision 0.5 of this document, the package was updated.

## 1.7 Revision 0.4

Revision 0.4 was published in December 2010. In revision 0.4 of this document, the package was updated.

## 1.8 Revision 0.3

Revision 0.3 was published in November 2010. The following is a summary of changes in revision 0.3 of this document.

- Classification Pulse diagrams were added.
- Catalog numbers metrology was changed.
- Extensive changes were made to document format and Theory of Operation section.
- Package drawing was corrected.
- Product Highlight and Typical Characteristics were added.

## 1.9 Revision 0.1

Revision 0.1 was published in April 2010. It was the first publication of this document.

## 2 Product Overview

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The PD70100 and PD70200 devices are part of Microsemi's series of Power over Ethernet (PoE) Powered Devices chips (PD). The PD70100 and PD70200 devices transmit integrated power and analog data in a single 12-pin package. They are used in Powered Devices (PD), thus enabling next generation network devices to share power and data over the same cable.

Microsemi's new PD family offers a solution to any PD application compliant with IEEE802.3af and IEEE802.3at standards and 4-pairs extra power applications. The IC family's components can be used in both indoor and outdoor applications.

The device family meets all PD-side-standards such as:

- Detection
- Classification
- Integrated isolation switch with inrush current limiter, and over-current protection
- Two-events classification recognition and AT flag generation (PD70200 only).

In addition, the devices have a discharge mechanism for a DC/DC input capacitor, ensuring quick redetection capability in case the RJ-45 plug is disconnected and reconnected within a short time span.

PD70200 IC design specifically supports IEEE802.3at standard, including two events classification detection that enables the PD to distinguish whether the connected power source equipment (PSE) is IEEE802.3at or IEEE802.3af based.

The PD70100/PD70200 ICs are designed to support 4 pair applications for PDs that require higher power.

### 2.1 Features

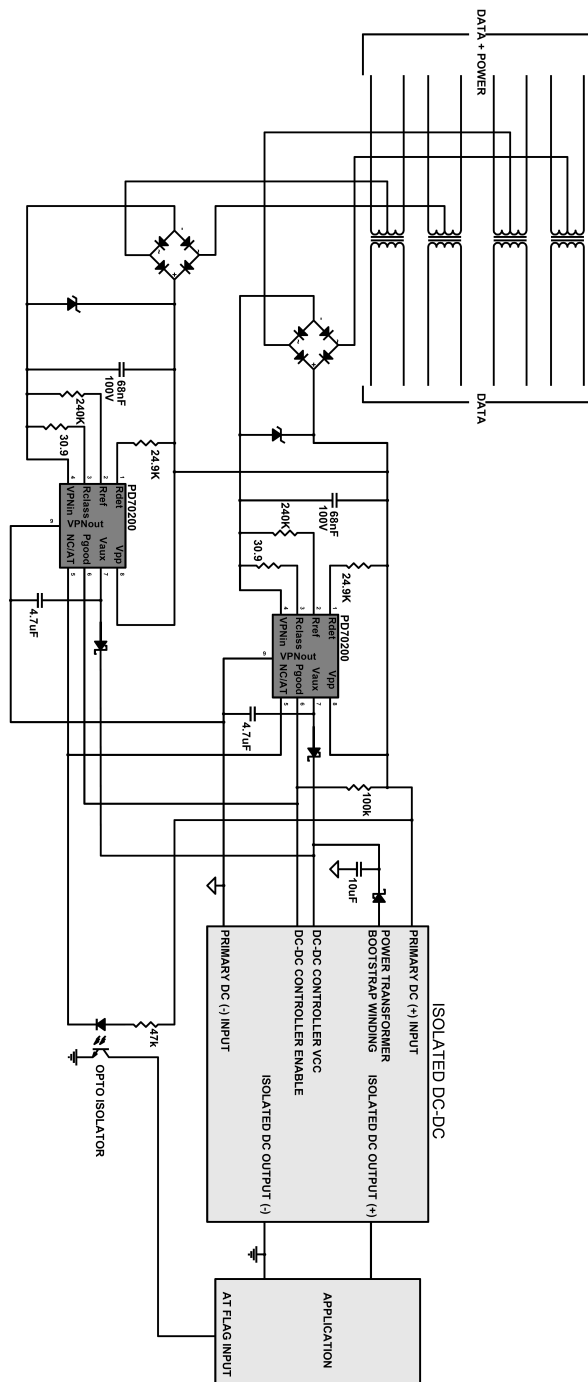
- Designed to Support IEEE802.3af and IEEE802.3at standards
- PD Detection & Programmable Classification Signature
- Two-events Classification Flag
- Signature Resistor Disconnection after Detection
- Integrated 0.6  $\Omega$  Isolating Switch and Inrush Current Limiter.
- 4-pairs support with a single PD70200 IC for up to 48 W
- 4-pairs support with two PD70200 ICs for up to 96 W
- Less than 10  $\mu$ A Offset Current during Detection
- Single DC Voltage Input (37 V – 57 V)
- Wide Operating Temperature Range: –40 to 85 °C
- On-chip Thermal Protection
- 12-pin 3 × 4mm Package
- RoHS Compliant
- MSL3

### 2.2 Applications

- Power over Ethernet Powered Devices
- IEEE802.3af & at 10/100/1000 BASE-T
- 4-pair extra power applications
- Indoor and outdoor applications

The following illustration shows a typical PD70100 /PD70200 application.

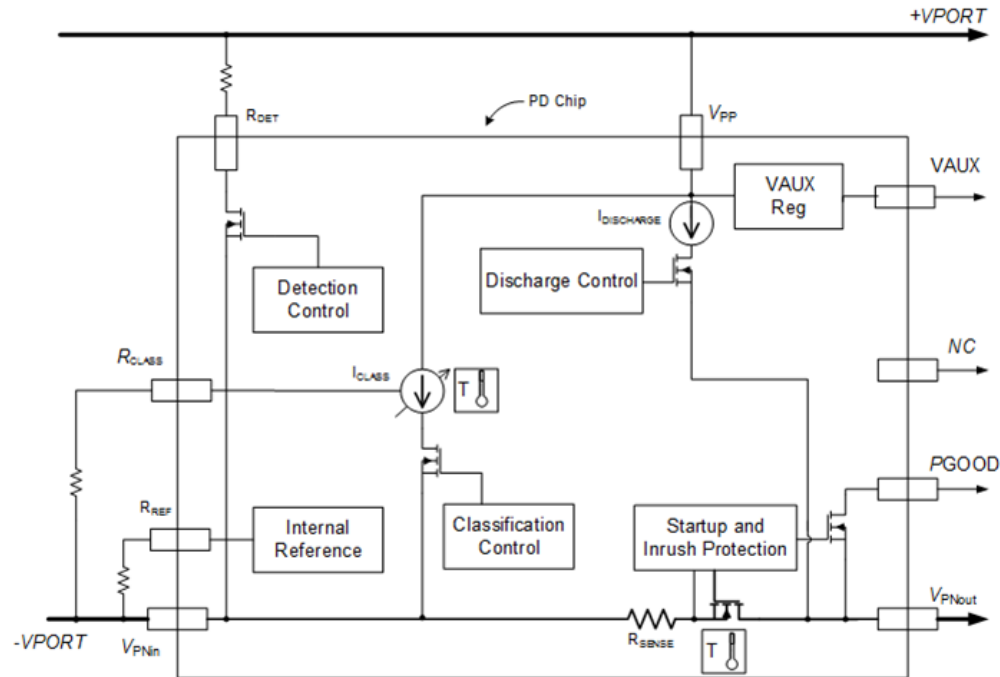
### Figure 1 • Typical Application with IEEE802.3at PSE



### 3 Functional Descriptions

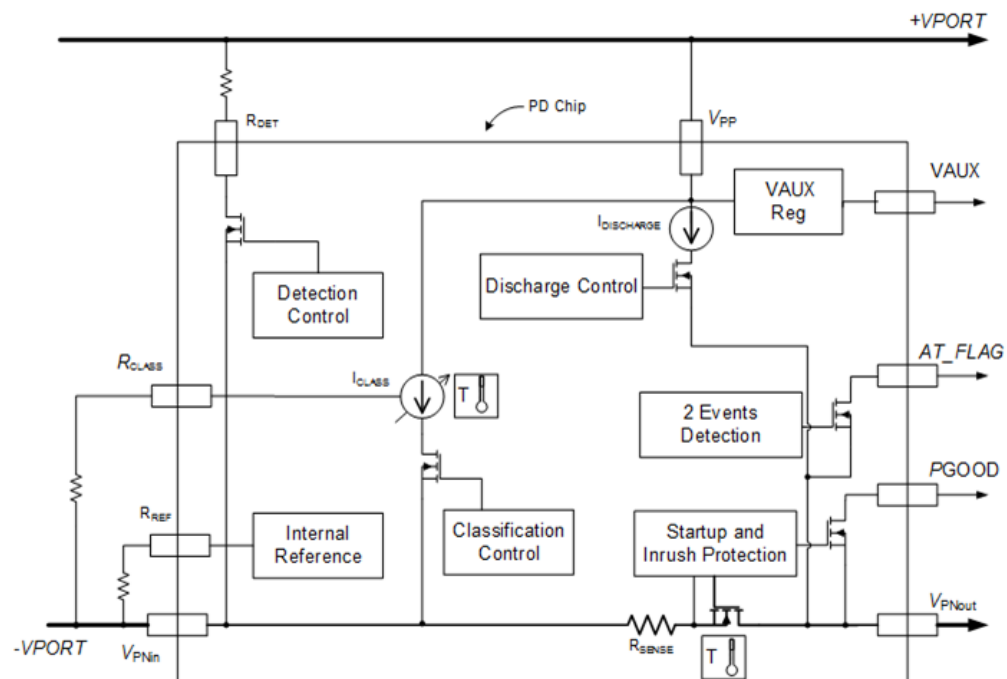
The following illustration shows the functional blocks of the PD70100.

**Figure 2 • PD70100 Functional Block Diagram**



The following illustration shows the functional blocks of the PD70200.

**Figure 3 • PD70200 Functional Block Diagram**



### 3.1 Detail Description

PD70100/PD70200 IC provides IEEE 802.3af/at compliant PD Front-End functions including Detection, Physical Layer Classification, Two-Events Classification (PD70200 only), Auxiliary Voltage Output, Power Good, Soft Start Current Limiting, Over-Current Protection, and Bulk Capacitor Discharge.

#### 3.1.1 Detection

IEEE 802.3af/at compliant detection is provided by a 24.9 K $\Omega$  resistor connected between  $V_{PP}$  and  $R_{DET}$  pin.  $R_{DET}$  pin is connected to  $VPN_{IN}$  via an open drain MOSFET with a maximum specified  $R_{DS(on)}$  of 50  $\Omega$ . Internal logic monitors  $V_{PP}$  to  $VPN_{IN}$  and connects the  $R_{DET}$  pin to  $VPN_{IN}$  when the rising  $V_{PP}$  to  $VPN_{IN}$  voltage is between 2.5 V and 10.1 V. When rising  $V_{PP}$  to  $VPN_{IN}$  voltage exceeds 10.1 V, the MOSFET is switched off. Once above 10.1 V, falling  $V_{PP}$  to  $VPN_{IN}$  voltage between 2.45 V and 4.85 V will reconnect  $R_{DET}$  pin to  $VPN_{IN}$ .

#### 3.1.2 Physical Layer Classification

Physical Layer (hardware) Classification per IEEE 802.3af/at is generated via a regulated reference voltage of 1.2 V, switched onto the  $R_{CLASS}$  pin. Internal logic monitors the  $V_{PP}$  to  $VPN_{IN}$  voltage and connects the 1.2 V reference to  $R_{CLASS}$  pin at a rising  $V_{PP}$  to  $VPN_{IN}$  voltage threshold between 11.1 V and 13.5 V. Once  $V_{PP}$  to  $VPN_{IN}$  has exceeded the rising threshold, there is a 1 V minimum hysteresis between the  $V_{PP}$  rising (turn-on) threshold and the  $V_{PP}$  falling (turn-off) threshold.

The 1.2 V reference stays connected to the  $R_{CLASS}$  pin until the  $V_{PP}$  to  $VPN_{IN}$  rising voltage exceeds the upper turn-off threshold of 20.9 V to 23.9 V. The 1.2 V reference voltage is disconnected from the  $R_{CLASS}$  pin at  $V_{PP}$  to  $VPN_{IN}$  voltages above the upper threshold.

Classification current signature is provided via a resistor connected between  $R_{CLASS}$  pin and  $VPN_{IN}$ . The classification current is therefore the current drawn by the PD70100/PD70200 IC during the classification phase, and is simply the 1.2 V reference voltage divided by the  $R_{CLASS}$  resistor value. The maximum current available at the  $R_{CLASS}$  pin is current limited to 55 mA (typical).

#### 3.1.3 Two-Events Detection and AT Flag

The PD70200 IC provides IEEE 802.3at Type 2 compliant detection of the “Two Events Classification Signature”, and generation of the AT flag. This feature is available on the PD70200 IC only.

Simply put, the “Two Events Classification Signature” is a means by which an IEEE 802.3at Type 2 Power Source can inform a compliant Power Device (PD) that it is AT Type 2 compliant, and as such is capable of providing AT Type 2 power levels.

The Power Source communicates with a Type 2 compliant signature by toggling the  $V_{PP}$  to  $VPN_{IN}$  voltage twice (2 “events”) during the Physical Layer Classification phase. The  $V_{PP}$  to  $VPN_{IN}$  voltage is toggled from the Physical Layer Classification’s voltage level (13.5 V to 20.9 V) down to a voltage “Mark” level. Voltage “Mark” level is specified as a  $V_{PP}$  to  $VPN_{IN}$  voltage of 4.9 V to 10.1 V.

PD70200 IC recognizes a  $V_{PP}$  to  $VPN_{IN}$  falling edge from Classification level to Mark level as being one event of the Two-Events Signature. If two such falling edges are detected, PD70200 will assert AT flag by means of an open drain MOSFET connected between  $AT\_FLAG$  pin and  $VPN_{OUT}$ .

$AT\_FLAG$  pin is active low; a low impedance state between  $AT\_FLAG$  and  $VPN_{OUT}$  indicates a valid Two-Events Classification Signature was received, and the Power Source is AT Type 2 compliant.

$AT\_FLAG$  MOSFET is capable of 5 mA of current and can be pulled up to  $V_{PP}$ .

#### 3.1.4 Soft Start and Inrush Current Protection

PD70100/PD70200 IC contains an internal isolation switch, that provides ground isolation between Power Source and PD application during Detection and Classification phases. The isolation switch is a N-channel MOSFET, wired in a common source configuration where the MOSFET’s Source is connected to Power Source ground at  $VPN_{IN}$ , and the MOSFET’s Drain is connected to application’s primary ground at  $VPN_{OUT}$ .

Internal logic monitors  $V_{PP}$  to  $VP_{NIN}$  voltage and keeps the MOSFET in a high impedance state until  $V_{PP}$  to  $VP_{NIN}$  voltage reaches turn-on threshold of 36 V to 42 V. Once  $V_{PP}$  to  $VP_{NIN}$  voltage exceeds this threshold, the MOSFET is switched into one of two modes.

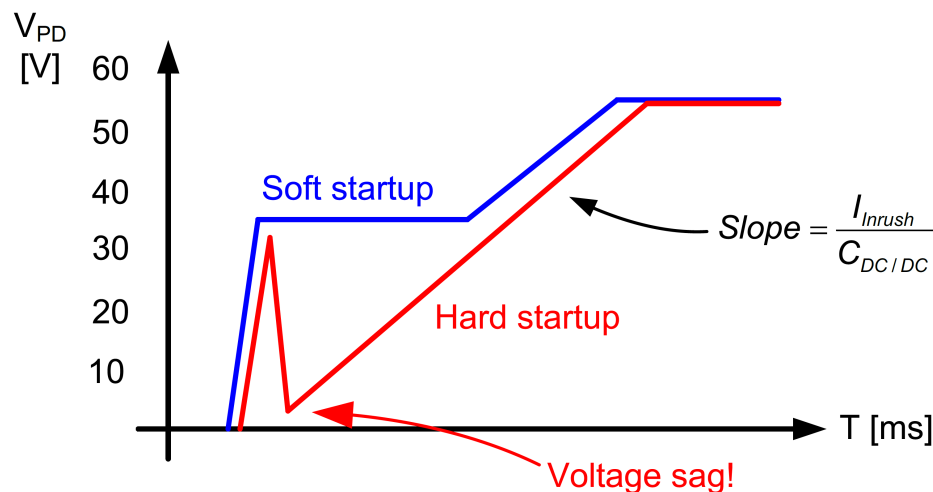
The mode into which the MOSFET is switched is determined by the voltage developed across the MOSFET, or put another way, the  $VP_{NOUT}$  to  $VP_{NIN}$  differential voltage. Two modes are defined below:

**Table 1 • Isolation Switch Modes**

$VP_{NOUT}$ to $VP_{NIN}$	Mode	Description
> 0.7 V	Soft Start Mode	Limits $VP_{NOUT}$ current to 240 mA (typical)
≤ 0.7 V	Normal Operating Mode	Limits $VP_{NOUT}$ current to 1.8 A (typical)

By controlling the MOSFET current based on  $VP_{NOUT}$  to  $VP_{NIN}$  voltage, inrush currents generated by fully discharged bulk capacitors can be limited. This method limits current to a maximum of 350 mA, compliant with IEEE 802.3af/at specification.

Soft Start current limiting is required to reduce occurrences of voltage sag at the PD input during device power-up. A comparison is shown in the figure below.



Once bulk capacitance has charged up to a point where  $VP_{NOUT}$  to  $VP_{NIN}$  differential voltage is less than 0.7 V, the isolation MOSFET is switched into normal operating mode with MOSFET current limit set at 1.8 A (typical), to provide over-current protection.

PD70100 and PD70200 ICs are different in their respective isolation MOSFET's continuous current handling capability:

- PD70100: 450 mA (max.)
- PD70200: 1123 mA (max.)

An adequate heat sink for the PD70100/PD70200 IC's exposed pad must be provided to achieve these current levels without damaging the IC. A large, heavy copper fill area and/or a heavy ground plane with Thermal Vias is recommended. Electrically the exposed pad ground plane should be connected to  $VP_{NIN}$ .

Internal logic monitoring  $V_{PP}$  to  $VP_{NIN}$  will place the isolation switch MOSFET in a high impedance state if voltage between  $V_{PP}$  and  $VP_{NIN}$  drops below 31 V to 34 V.

### 3.1.5 Over-Current Protection

Over-current protection is provided on the PD70100/PD70200 IC using the Isolation MOSFET Switch, which limits the  $VP_{NOUT}$  current to 1.8 A during normal operation. See previous description of Soft Start.

### 3.1.6 Power Good

During Soft Start mode, the PD70100/PD70200 IC monitors  $V_{PNOUT}$  to  $V_{PNIN}$  differential voltage. When this voltage is less than 0.7 V (max.), the IC enters normal operation mode and the isolation switch current limit is increased to 1.8 A (typical). At this same 0.7 V (max.) threshold the Power Good signal is asserted by means of an open drain MOSFET between PGOOD and  $V_{PNOUT}$ .

PGOOD pin is active low; a low impedance state between PGOOD and  $V_{PNOUT}$  indicates the Soft Start mode has finished and the isolation switch has transitioned into normal operating mode.

PGOOD MOSFET can handle current of 5 mA and can be pulled up to  $V_{PP}$ .

### 3.1.7 Auxiliary Voltage Output

PD70100/PD70200 IC provides a 10.5 V (typical) regulated output to be used as a start-up supply for DC/DC controllers whose  $V_{CC}$  is provided via a bootstrap winding. This regulated supply is available at  $V_{AUX}$  pin, and is referenced to  $V_{PNOUT}$  pin.  $V_{AUX}$  supply is designed for low-duty operation, and should not be designed as a primary housekeeping supply. The current capability is continuous 2 mA, with 10 mA peak ( $\leq 10$  ms).  $V_{AUX}$  output is current-limited at 10 mA (min.).

For stability, the  $V_{AUX}$  regulator requires a minimum of 4.7  $\mu$ F ceramic capacitor connected directly between  $V_{AUX}$  and  $V_{PNOUT}$  pins.

### 3.1.8 Thermal Protection

Both PD70100 and PD70200 IC include temperature sensors which individually monitor both the isolation MOSFET and the Classification Current Source for over temperature conditions. In case of an over temperature condition, the sensor will activate protection circuitry which will disconnect its respective monitored function.

### 3.1.9 Bulk Capacitor Discharge

The bulk capacitor discharge circuitry eliminates the need to place a diode in series with the  $V_{PP}$  line to prevent an application's bulk capacitance from discharging through the detection resistor and the isolation switch MOSFET's body diode. Discharge current through the detection resistor can cause failure of the detection signature in cases where a PD is connected and the bulk capacitance is not fully discharged.

During normal operation, PD70100/PD70200 IC continuously monitors voltage at  $V_{PP}$  to  $V_{PNIN}$ . Should  $V_{PP}$  to  $V_{PNIN}$  voltage fall below isolation switch turn-off threshold (31 V to 34 V), isolation switch MOSFET is immediately placed in a high-impedance state. At this point the internal logic monitors the voltage at  $V_{PP}$  to  $V_{PNOUT}$ . If  $V_{PP}$  to  $V_{PNOUT}$  voltage is between 1.5 V to 32 V, a 23 mA (min.) constant current source is connected across the  $V_{PP}$  and  $V_{PNOUT}$  pins. This constant current source provides bulk capacitor discharge.

A 220  $\mu$ F bulk capacitance can be discharged from 32 V to 1.5 V in a maximal period of 292 ms.

## 4 Electrical Specifications

### 4.1 Absolute Maximum Ratings

**Table 2 • Absolute Maximum Ratings**

Supply Input Voltage ( $V_{PP}$ ) Continuous	-0.3 V to 74 V <sub>DC</sub>
Supply Input Voltage ( $V_{PP}$ ) 1 ms pulse	-0.3 V to 88 V <sub>DC</sub>
Port Negative Out Voltage (V <sub>PNOUT</sub> )	-0.3 V to 74 V <sub>DC</sub>
R <sub>DET</sub> Continuous	-0.3 V to 74 V <sub>DC</sub>
R <sub>DET</sub> 1 mS pulse	-0.3 V to 88 V <sub>DC</sub>
R <sub>CLASS</sub> , R <sub>REF</sub>	-0.3 V to 5 V <sub>DC</sub>
V <sub>AUX</sub>	-0.3 V to 30 V <sub>DC</sub>
PGOOD, AT_FLAG (with respect to V <sub>PNOUT</sub> ) Continuous	-0.3 V to 74 V <sub>DC</sub>
PGOOD, AT_FLAG (with respect to V <sub>PNOUT</sub> ) 1 mS pulse	-0.3 V to 88 V <sub>DC</sub>
ESD Protection*	±1.5 kV HBM
Maximum Operating Junction Temperature (T <sub>A</sub> )	150 °C
Operating Ambient Temperature	-40 °C to 85 °C
Storage Temperature Range	-65 °C to 150 °C
Peak Package Solder Reflow Temp (40 seconds max exposure)	260 °C

\* All pins except pin 11 (V<sub>AUX</sub>). Pin 11 ESD Protection ±150 V HBM.

\*\* No pin voltage can be higher than V<sub>pp</sub>.

**Note:** Exceeding these ratings could cause damage to the device. All voltages are with respect to V<sub>PNIN</sub> except for V<sub>AUX</sub>, PGOOD and AT\_FLAG with respect to V<sub>PNOUT</sub>. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

### 4.2 Typical Electrical Performance

Unless otherwise specified, the following specifications apply over the operating ambient temperature -40 °C ≤ T<sub>AMB</sub> ≤ 85 °C. Production tests are done at 25 °C T<sub>A</sub>.

#### 4.2.1 Power Supply

**Table 3 • Power Supply**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions/Comment
Input Voltage	V <sub>PP</sub>	0	55	57	V	Supports Full IEEE802.3 af/at functionality
Power Supply Current at Operating Mode			1	3	mA	V <sub>PP</sub> = 55 V

## 4.2.2 Detection Mode

**Table 4 • Detection Mode**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions/Comment
Detection is connected. At this voltage range R <sub>DET</sub> must be on.	DET <sub>RANGE</sub>	1.3		10.1	V	Measured between V <sub>PP</sub> and V <sub>PNIN</sub>
Detection Switch ON Resistance PD-detection	R <sub>DET-on</sub>			50	Ω	2.5 V ≤ (ΔV <sub>PP</sub> to V <sub>PNIN</sub> ) ≤ 10.1 V Measured between R <sub>DET</sub> and V <sub>PNIN</sub>
Detection is Disconnected	R <sub>DET-off</sub>	10.1		12.8	V	Measured between V <sub>PP</sub> and V <sub>PNIN</sub>
Detection Switch OFF Resistance	R <sub>DET-off</sub>	2.0			MΩ	12.8 V ≤ (ΔV <sub>PP</sub> to V <sub>PNIN</sub> ) ≤ 57.0 V Measured between R <sub>DET</sub> and V <sub>PNIN</sub>
Input Offset Current	I <sub>OFFSET</sub>			16	μA	1.1 V to 10.1 V -40 °C ≤ T <sub>J</sub> ≤ 85 °C
	I <sub>OFFSET</sub>			10	μA	1.1V to 10.1V -40 °C ≤ T <sub>J</sub> ≤ 55 °C

## 4.2.3 Classification Mode

**Table 5 • Classification Mode**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions/Comment
Classification Current Source, Turn ON ThresholdRangeMeasured at V <sub>PP</sub>	V <sub>TH-low-on</sub>	11.4		13.7	V	Turn on for any I <sub>CLASS</sub> while V <sub>PP</sub> increases
Classification Current Source, Turn OFF ThresholdRangeMeasured at V <sub>PP</sub>	V <sub>TH-high-off</sub>	20.9		23.9	V	Turn off while V <sub>PP</sub> increases
Current Limit Threshold	I <sub>CLASS-LIM</sub>	50.0	68	80.0	mA	
Input Current I <sub>PP</sub> When Classification Function is Disabled	I <sub>CLASS-DIS</sub>			4.0	mA	Class 0 R <sub>CLASS</sub> = Disconnect
Input Current I <sub>PP</sub> When Classification Function is Enabled	I <sub>CLASS-EN</sub>	9.0	10.5	12.0	mA	Class 1 R <sub>CLASS</sub> = 133 Ω ± 1%
		17.0	18.5	20.0	mA	Class 2 R <sub>CLASS</sub> = 69.8 Ω ± 1%
		26.0	28.0	30.0	mA	Class 3 R <sub>CLASS</sub> = 45.3 Ω ± 1%
		36.0	40.0	44.0	mA	Class 4 R <sub>CLASS</sub> = 30.9 Ω ± 1%

#### 4.2.4 Mark

**Table 6 • Mark**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions/Comment
Mark, Working Voltage Range	V <sub>MARK</sub>	4.9		10.1	V	When voltage decreases Measured between V <sub>PP</sub> to V <sub>PNIN</sub>
Mark Current	I <sub>MARK</sub>	0.25		4	mA	Chip current

#### 4.2.5 Isolation Switch

**Table 7 • Isolation Switch**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions/Comment
Isolation Switch MOSFET Switches from Off to I <sub>LIM-LOW</sub>	V <sub>SW-START</sub>	36		42	V	
Isolation Switch MOSFET Switched Off	V <sub>SW-OFF</sub>	30.5		34.5	V	
Startup Current Limit, I <sub>LIM</sub>	I <sub>LIM-LOW</sub>	105	240	325	mA	
V <sub>PNIN</sub> to V <sub>PNOUT</sub> Threshold Voltage for I <sub>LIM-LOW</sub> to I <sub>LIM-HIGH</sub> Switchover	V <sub>DIFF</sub>			0.7	V	When V <sub>PNIN</sub> to V <sub>PNOUT</sub> ≤ V <sub>DIFF</sub> , Isolating switch switches over from I <sub>LIM-LOW</sub> to I <sub>LIM-HIGH</sub> .
Over Current Protection Current Limit	OCP	1500	1800	2000	mA	
Continuous Operation Load Current (PD70100)	I <sub>LOAD</sub>		350	450	mA	Isolating switch at I <sub>LIM-HIGH</sub>
Continuous Operation Load Current (PD70200)			600	1123		
Continuous Operation Total R <sub>DSon</sub>	SW-R <sub>DSon</sub>			0.6	Ω	Total resistance between V <sub>PNIN</sub> and V <sub>PNOUT</sub> Isolating switch at I <sub>LIM-HIGH</sub>

#### 4.2.6 DC/DC Capacitor Discharger

**Table 8 • DC/DC Capacitor Discharger**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions /Comment
DC/DC Input Capacitance			220		μF	For reference only Guaranteed by design (not tested in production)
Discharge Current		22.8	32	50	mA	7.0V ≤ V <sub>PP</sub> to V <sub>PNOUT</sub> ≤ 30 V
Full Discharge Time for Full Discharge of Input Capacitance	T <sub>DSC</sub>			500	ms	V <sub>PP</sub> < UVLO threshold Guaranteed by design (not tested in production)

#### 4.2.7 AT\_FLAG

**Table 9 • AT\_FLAG**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions/Comment
Output Low Voltage				0.4	V	I <sub>OL</sub> = 0.75 mA
				2.5	V	I <sub>OL</sub> MAX = 5 mA
Leakage Current				1.7	μA	V <sub>ATFLAG</sub> = 57 V

#### 4.2.8 PGOOD

**Table 10 • PGOOD**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions/Comment
Output Low Voltage				0.4	μF	I <sub>OL</sub> = 0.75 mA
				2.5	mA	I <sub>OL</sub> MAX = 5 mA
Leakage Current				1.7	μA	V <sub>PGOOD</sub> = 57 V

#### 4.2.9 Thermal Shutdown

**Table 11 • Thermal Shutdown**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions/Comment
Thermal Shutdown Temperature		180	200	220	°C	

#### 4.2.10 VAUX

Reference to VPN<sub>OUT</sub>.

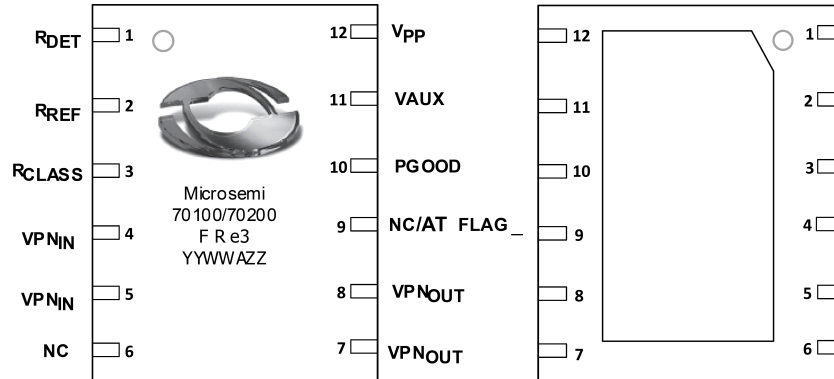
**Table 12 • VAUX**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions/Comment
V <sub>AUX</sub> Output Voltage On	V <sub>AUX-on</sub>	9.5	10.5	11.8	V	Isolating switch at I <sub>LIM-HIGH</sub> and PGOOD = Low
Output Current Peak	I <sub>VAUXP</sub>	0		10	mA	Capacitor = 30 μF
						When T <sub>LOAD</sub> ≤ 5 mS
Output Continuous Current	I <sub>VAUXC</sub>	0		2	mA	Isolating switch at I <sub>LIM-HIGH</sub> and PGOOD = Low
						When T <sub>LOAD</sub> ≤ 10 mS
V <sub>AUX</sub> Output Current Limit	I <sub>VAUX</sub>	10		32	mA	Isolating switch at I <sub>LIM-HIGH</sub> and PGOOD = Low

## 5 Pin Description

The following illustration shows the device pinout, from the top view and bottom view.

**Figure 4 • Pinout Top View and Bottom View**



The following table lists the pin descriptions for the PD70100/PD70200 devices.

**Table 13 • Pin Descriptions**

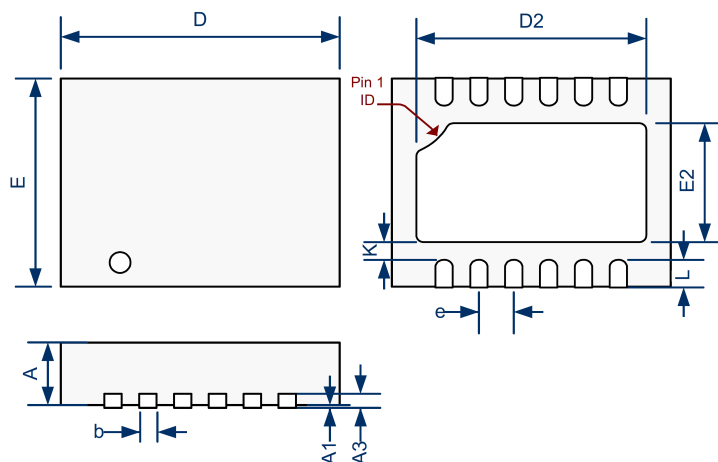
Pin	Pin Name (PD70100)	Pin Name (PD70200)	Type	Description
1	R <sub>DET</sub>	R <sub>DET</sub>		Valid Detection resistor. Connect external 24.9 kΩ detection resistor between R <sub>DET</sub> and V <sub>PP</sub> .
2	R <sub>REF</sub>	R <sub>REF</sub>		Bias current resistor. Connect a 243 k 1% resistor between this pin and VPN <sub>IN</sub> .
3	R <sub>CLASS</sub>	R <sub>CLASS</sub>		Power classification setting. Connect external class resistor between R <sub>CLASS</sub> and VPN <sub>IN</sub> .
4	VPN <sub>IN</sub>	VPN <sub>IN</sub>	Power	V <sub>Port</sub> Negative input. Connected to the isolating SW input. N-channel MOSFET source. The exposed thermal pad should be connected to these pins.
5				
6	N.C.	N.C.		
7	VPN <sub>OUT</sub>	VPN <sub>OUT</sub>	Power /Gnd	V <sub>Port</sub> Negative output. Connected to the isolating SW output. N-channel MOSFET Drain. Primary side Ground.
8				A decent ground plane should be deployed around this pin whenever is possible.
9	N.C	AT_FLAG	Open drain	The two-event detector should discern between AF and AT classification waveforms and outputs the AT_FLAG (PD70200 only).
10	PGOOD	PGOOD	Open drain	After startup, a PGOOD flag is generated in order to optionally inform the application DC/DC converter that the power rails are ready.
11	V <sub>AUX</sub>	V <sub>AUX</sub>	Power	Auxiliary output voltage to VPN <sub>OUT</sub> . Can be used for DC-DC startup for bootstrap initiation.
12	V <sub>PP</sub>	V <sub>PP</sub>	Power	High voltage positive input, reference to VPN <sub>IN</sub> and high voltage positive input, reference to VPN <sub>OUT</sub> during capacitor discharge.
EP	EPAD	EPAD		Connect to VPN <sub>IN</sub> . EPAD should be connected to a large copper area for improved thermal management.

## 6 Package Specifications

This section provides information about the available package.

**Note:** Dimensions do not include mold flash or protrusions; these shall not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage. Dimensions are in millimeters, inches for reference only.

**Figure 5 • Package Drawing Dimensions and Measurements**



**Table 14 • Package Dimensions: DFN**

Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
D	4.00 BSC		0.157 BSC	
E	3.00 BSC		0.118 BSC	
D2	3.00	3.70	0.118	0.146
E2	1.40	1.80	0.055	0.071
e	0.50 BSC		0.0197 BSC	
K	0.20 MIN		0.008 MIN	
L	0.30	0.50	0.012	0.020
b	0.18	0.30	0.007	0.012

## 6.1 Thermal Specifications

The following table lists the thermal specifications for the PD70100 and PD70200 devices.

**Table 15 • Thermal Specifications**

Parameter	Value
Typical thermal resistance: junction to ambient	40 °C/W
Typical thermal resistance: junction to case	4 °C/W

The  $\theta_{JA}$  numbers are guidelines for the thermal performance of the device/pc-board system. All specifications assume no ambient airflow.

## 7 Ordering Information

**Table 16 • Ordering Information**

Part Number	Packaging Type	Package	Part Marking
PD70100ILD	Bulk	DFN	MSC
PD70100ILD-TR	Tape and Reel	4 mm × 3 mm	70100
		12 pins	F R e3 <sup>1</sup>
		RoHS Compliant / Pb-free	YYWWAZZ <sup>2</sup>
PD70200ILD	Bulk	DFN	MSC
PD70200ILD-TR	Tape and Reel	4 mm × 3 mm	70200
		12 pins	F R e3 <sup>1</sup>
		RoHS Compliant / Pb-free	YYWWAZZ <sup>2</sup>

1. F R e3: F = FAB Code, R = Product revision code, and e3 = 2nd level interconnect.

2. YY = Year, WW = Week, A = Assembly location, and ZZ = Assembly Lot sequence code.

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