

Version :1.0

<p>TECHNICAL SPECIFICATION</p> <p>MODEL NO : PD080SY1</p>

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Revision History

Rev.	Eng.	Issued Date	Revised Content
0.1	黄秀晶	May 16, 2007	Preliminary
0.2	黄秀晶	May 18, 2007	Add Page8 7. Electrical Characteristics all power Page22 15. Reliability Test data
1.0	黄秀晶	July 31, 207	Add Page24 16. Packing Diagram

TECHNICAL SPECIFICATION**CONTENTS**

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1. Application

This data sheet applies to a color TFT LCD module, PD080SY1. This module applies to OA product, computer peripheral, image communication and multi-media. If you must use in severe reliability environment, please don't extend over PVI's reliability test conditions.

If you use PD080SY1, Prime View advises your systems use PVI's timing controller IC (PVI-2003A), which will generate proper timing, signals to control it.

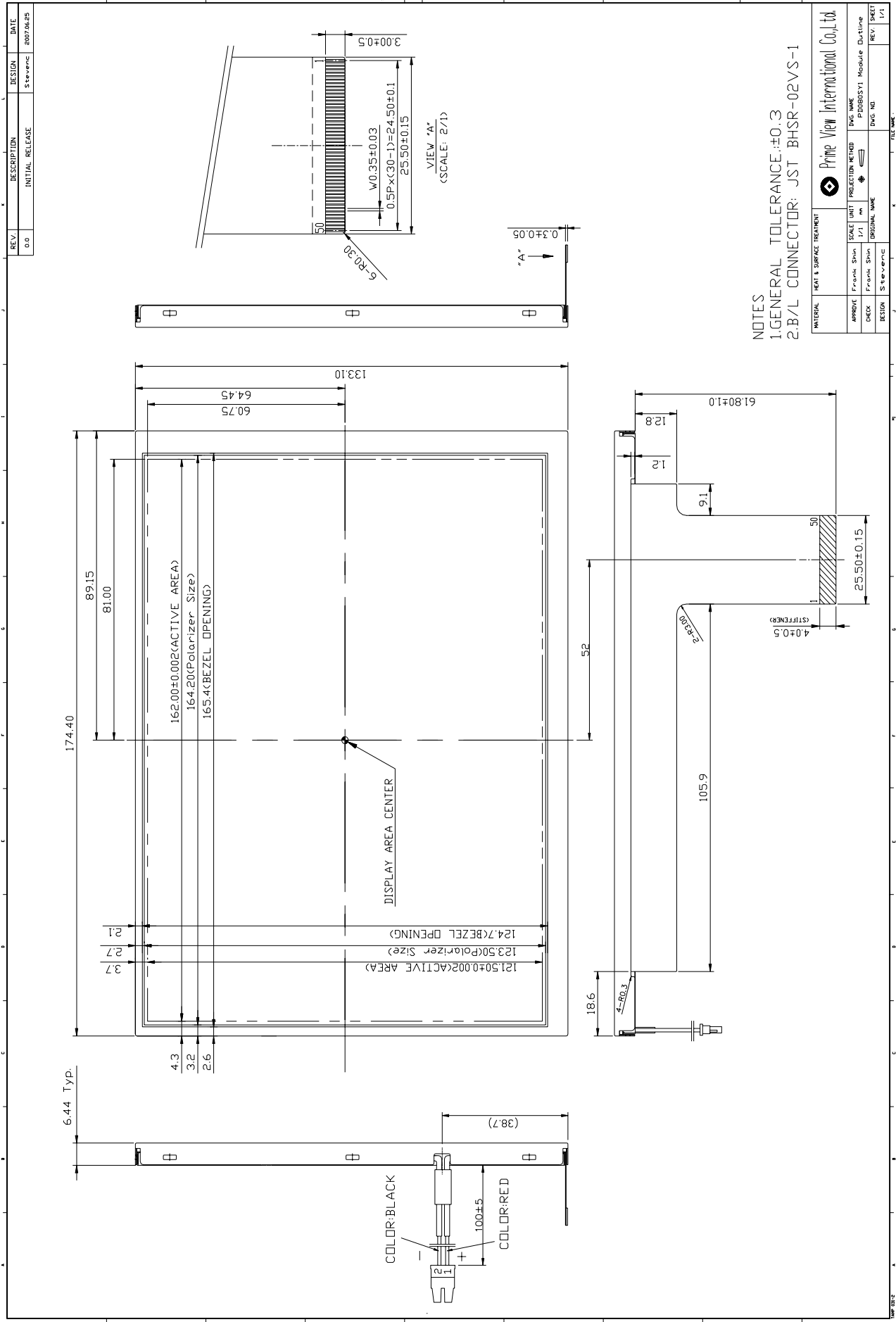
2. Features

- . Amorphous silicon TFT LCD panel with LED backlight unit
- . Pixel in stripe configuration
- . Slim and compact, designed for O/A application
- . Support TTL interface
- . Display Colors : 262,144 colors

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	8.0" (diagonal)	inch
Display Format	800 X(RGB) X600	dot
Display Colors	262K	
Active Area	162(H) X121.5 (V)	mm
Pixel Pitch	0.2025(H) X0.2025(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	174.4(W) X133.1(H) X6.44(D) (typ.)	mm
Weight	200±15	g
Back-light	30- LED	
Surface treatment	Anti-Glare+ EWW	
Display mode	Normally white	
Gray scale inversion direction	6 (ref to Page 18 viewing angle)	o'clock

4.Mechanical Drawing of TFT-LCD Module



5. Input / Output Terminals

5-1) TFT-LCD Panel Driving

Pin No.	Symbol	Function	Remark
1	VCOM	Common Voltage	
2	XON	Output all-on control	Note 5-10
3	DIO1	Horizontal start Pulse Signal I/O	Note 5-6
4	VCC(S)	Power Supply for Digital Circuit of Source IC	
5	CLK	Horizontal Clock	
6	SHL	Select Left / Right Shift	Note 5-6
7	D00	Red Data (LSB)	
8	D01	Red Data	
9	D02	Red Data	
10	D03	Red Data	
11	D04	Red Data	
12	D05	Red Data (MSB)	
13	D10	Green Data (LSB)	
14	D11	Green Data	
15	D12	Green Data	
16	D13	Green Data	
17	D14	Green Data	
18	D15	Green Data (MSB)	
19	AVDD(S)	Power Supply for Analog Circuit	Note 5-11
20	VR1	Gamma Voltage Level 1	
21	VR 2	Gamma Voltage Level 2	
22	VR 3	Gamma Voltage Level 3	
23	VR 4	Gamma Voltage Level 4	
24	VR 5	Gamma Voltage Level 5	
25	VR 6	Gamma Voltage Level 6	
26	VR 7	Gamma Voltage Level 7	
27	VR 8	Gamma Voltage Level 8	
28	VR 9	Gamma Voltage Level 9	
29	VR 10	Gamma Voltage Level 10	
30	AVSS(S)	Power Ground	
31	D20	Blue Data (LSB)	
32	D21	Blue Data	
33	D22	Blue Data	
34	D23	Blue Data	
35	D24	Blue Data	
36	D25	Blue Data (MSB)	
37	LD	Latch The Polarity of Output and Switch The New Data to Output	Note 5-7
38	REV	Control Signals are Inverted or not	Note 5-8
39	POL	Polarity Selection	Note 5-9
40	GND(S)	Power Ground	
41	DIO2	Horizontal start Pulse Signal I/O	Note 5-6
42	OEV	Output Enable	Note 5-5
43	UD	Up / Down Control Pin	Note 5-3
44	VCLK	Vertical Clock	Note 5-4
45	STVU	Vertical start Pulse Signal I/O	Note 5-3
46	STVD	Vertical start Pulse Signal I/O	
47	VDDG	Gate ON Voltage	Note 5-2
48	VEEG	Gate OFF Voltage	Note 5-1
49	VCC(G)	Power Supply for Digital Circuit of Gate IC	
50	GND(G)	Power Ground	

Note 5-1: $VEEG_{(TYP.)} = -6V$

Note 5-2: $VDDG_{(TYP.)} = 18V$

Note 5-3: Select up or down shift

UD	STVU	STVD	Shift
1	Hi-Z	Input	Up
0	Input	Hi-Z	Down

Note 5-4: Gate driver shift clock

Note 5-5: When OEV is connected to high “1”, the driver outputs are disabled (Gate output = VEEG). Under this condition, the operation of registers will not be affected.

Note 5-6: Select left or right shift

SHL	DIO1	DIO2	Shift
1	Input	Hi-Z	Right
0	Hi-Z	Input	Left

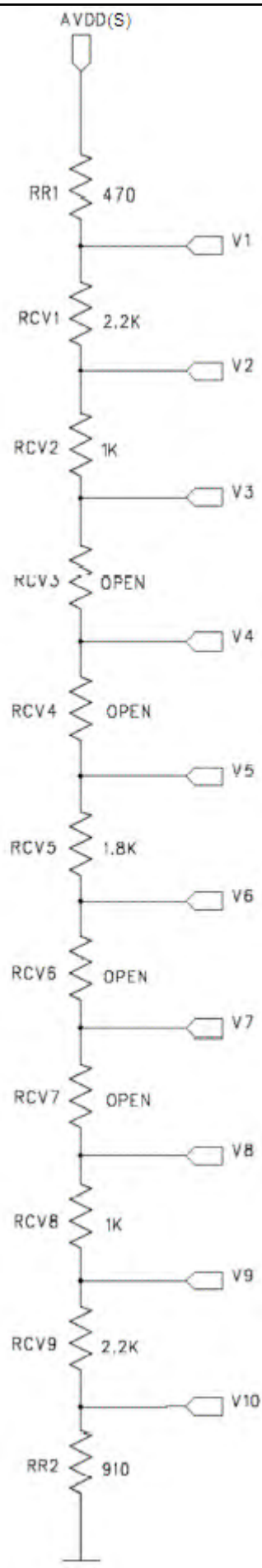
Note 5-7: Latch the polarity of outputs and switch the new data to outputs. At the rising edge (LD), latch the “POL” signal to control the polarity of the outputs.

Note 5-8: Control whether the Data R0~G5 are inverted or not. (PVI suggests connecting to GND)
When “REV=1”, these data will be inverted.
EX: “00”→”3F”, “07”→”38”, “15”→”2A”

Note 5-9: Polarity selector for dot-inversion control. Available at the rising edge of LD.
When POL=1: Even outputs range from V1~V7, and Odd outputs range from V8~V14;
When POL=0: Even outputs range from V8~V14, and Odd outputs range from V1~V7.

Note 5-10: Output all-on control. As XON is low then all output pins are forced to VDDG level.

Note 5-11: Typical Application Circuit (When $AVDD(S)_{(TYP.)} = 9.6V$)



5-2) Backlight driving

Connector type: JST BHSR-02VS-1, PIN No 2 pin

Pin No	Symbol	Description	Remark
1	+	Input terminal (HV)	Wire color : Red
2	-	Input terminal (GND)	Wire Color : Black

6.Absolute Maximum Ratings:

AVSS(S) =GND=0V,Ta=25°C

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	VCC(S)	-0.3	4.0	V	
	VCC(G)	-0.3	7.0	V	
	AVDD(S)	-0.3	13.5	V	
	VDDG	-0.3	40.0	V	
	VDDG-VEEG	-0.3	40.0	V	
	VEEG	-20	0.3	V	

7.Electrical Characteristics

7-1) Recommended Operating Conditions:

AVSS(S)=GND = 0V , Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver	VCC(S)	3.0	3.3	3.6	V	
	AVDD(S)	9.3	9.6	9.9	V	
Supply Voltage for Gate Driver	VDDG	17	18	19	V	
	VEEG	-6.6	-6	-5.4	V	
	VCC(G)	3.0	3.3	3.6	V	
VCOM Voltage	VCOM	3.5	4.0	4.5	V	
Digital Input Voltage	V _{IH}	0.7 VCC(G)	-	VCC(G)	V	
	V _{IL}	0	-	0.3 VCC(G)	V	

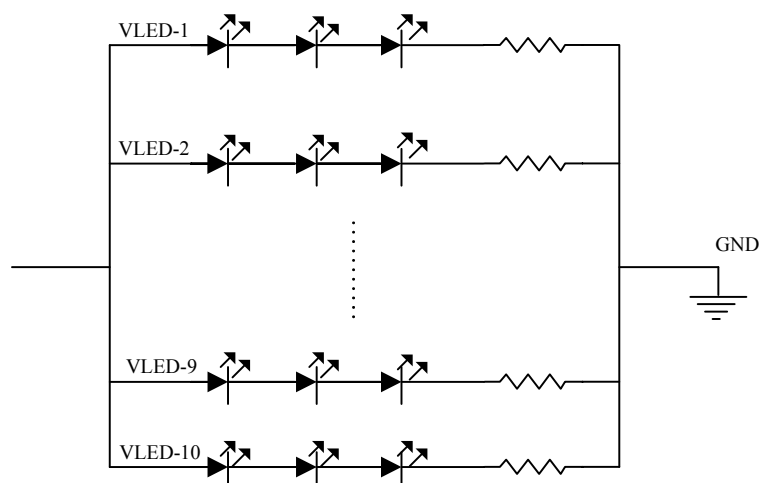
7-2) Recommended Driving Condition for Back Light

GND = 0 V , Ta = 25°C

Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	V _{LED-1~10}	-	11	11.5	V	I _{LED} = 20 mA
Supply current of LED backlight	I _{LED-1~10}	-	20	-	mA	Note 7-1
Backlight Power Consumption	P _{LED}	-	2.2	2.3	W	Note 7-2

Note 7-1 : The LED driving condition is defined for each LED module. (3 LED Serial)

Note 7-2 : $P_{LED} = V_{LED-1} * I_{LED-1} + V_{LED-2} * I_{LED-2} \dots V_{LED-9} * I_{LED-9} + V_{LED-10} * I_{LED-10}$



7-3) Power Consumption

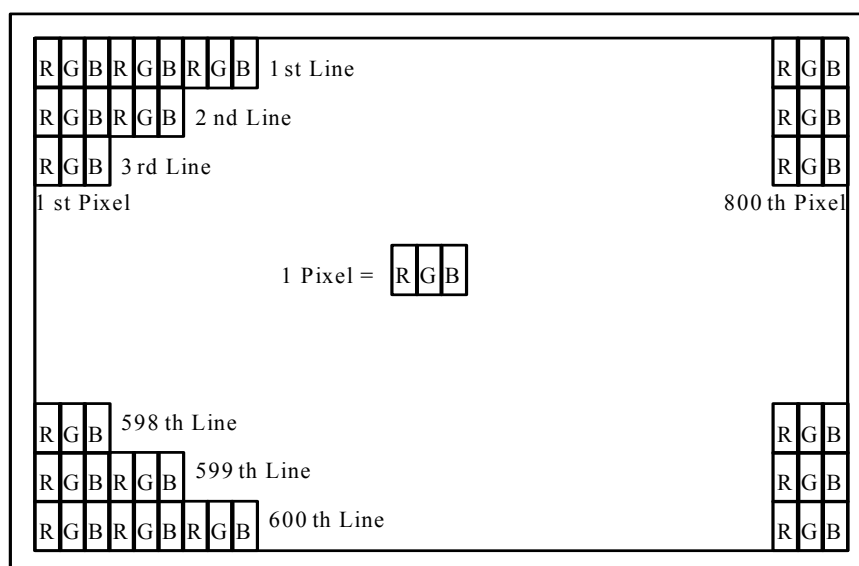
Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current for Gate Driver (Hi level)	IDDG	VDDG =18V	0.5	1	mA	
Supply Current for Gate Driver (Low level)	IIEG	VEEG =-6V	0.5	1	mA	
Supply Current for Source Driver (Digital)	ICC(S)	VCC(S)=3.3V	150	250	mA	
Supply Current for Source Driver (Analog)	IVDD(S)	AVDD(S)=9.6V	30	50	mA	
Supply Current for Gate Driver (Digital)	ICC(G)	VCC(G)=3.3V	150	250	mA	
LCD Panel Power Consumption	-	-	1.29	2.16	W	Note 7-4
LED Back Light Power Consumption	-	-	2.2	2.3	W	Note 7-5

Note 7-4: The power consumption for back light is not included.

Note 7-5: Back light lamp power consumption is calculated by $I_L \times V_L$.

8. Pixel Arrangement

The LCD module pixel arrangement is the stripe.

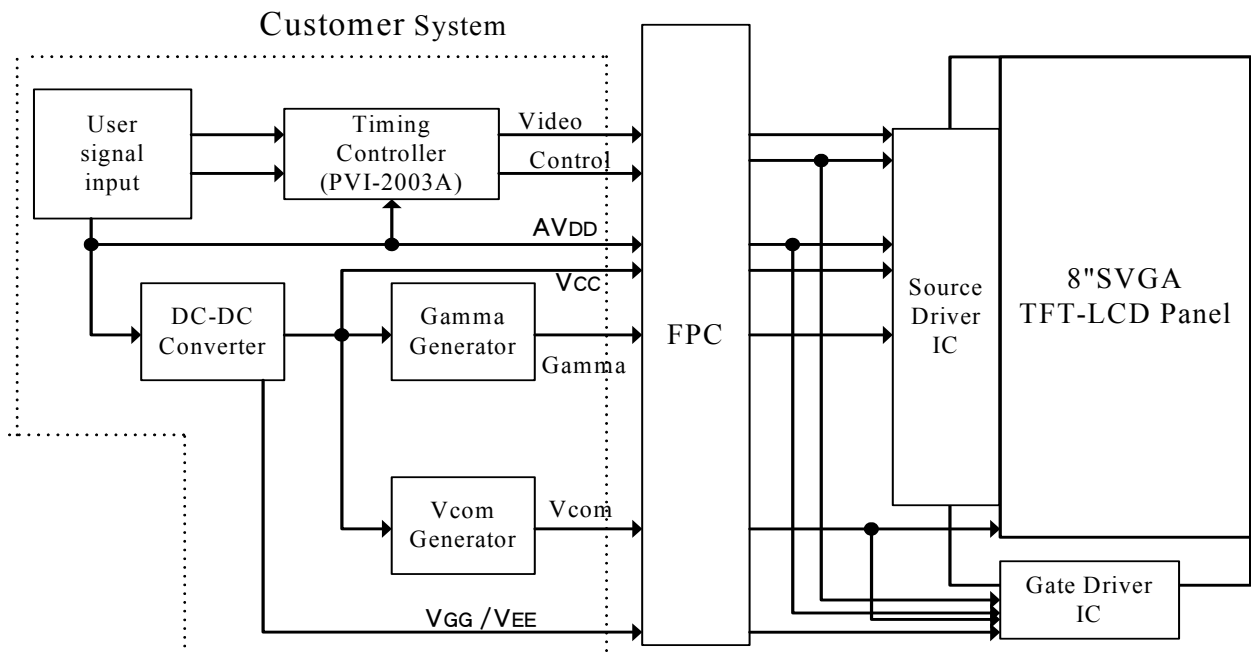


9. Display Color and Gray Scale Reference

Color		Input Color Data																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Red (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Green (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

10. Block Diagram

10-1) TFT-module Block Diagram



If you use PD080SY1, you can apply PVI-2003A (Timing controller) which will generate timing signals to support PD080SY1.

11. Interface Timing
11-1) Timing Parameters
AC Electrical Characteristics

(VCC(G)=VCC(S)=3.3V, AVDD(S)=9.6V, GND=AVSS(S) =0V, Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Frequency	F _{clk}	-	40	45	MHz
CLK Pulse Width	T _{cw}	22	-	-	ns
Data Set-up Time	T _{su}	4	-	-	ns
Data Hold Time	T _{hd}	2	-	-	ns
Propagation Delay of DIO2/1	T _{phl}	6	10	15	ns
Time That The Last Data to LD	T _{ld}	1	-	-	T _{cw}
Pulse width of LD	T _{wld}	2	-	-	T _{cw}
Time That LD to DIO1/2	T _{lds}	5	-	-	T _{cw}
POL Set-up Time	T _{psu}	6	-	-	ns
POL Hold Time	T _{phd}	6	-	-	ns
OE Pulse Width	T _{OE}	1	-	-	μs
CKV Pulse Width	T _{CKV}	500	-	-	ns
STV Set-up Time	T _{SUV}	400	-	-	ns
STV Hold Time	T _H	400	-	-	ns
Horizontal Display Period	T _{HDP}	800	800	800	T _{cw}
Horizontal Period Timing Range	T _{HP}	920	1056	1064	T _{cw}
Horizontal Lines Per Field	T _V	604	628	800	T _{HP}
Vertical Display Timing Range	T _{DV}	600	600	600	T _{HP}

11-2) Timing Diagram

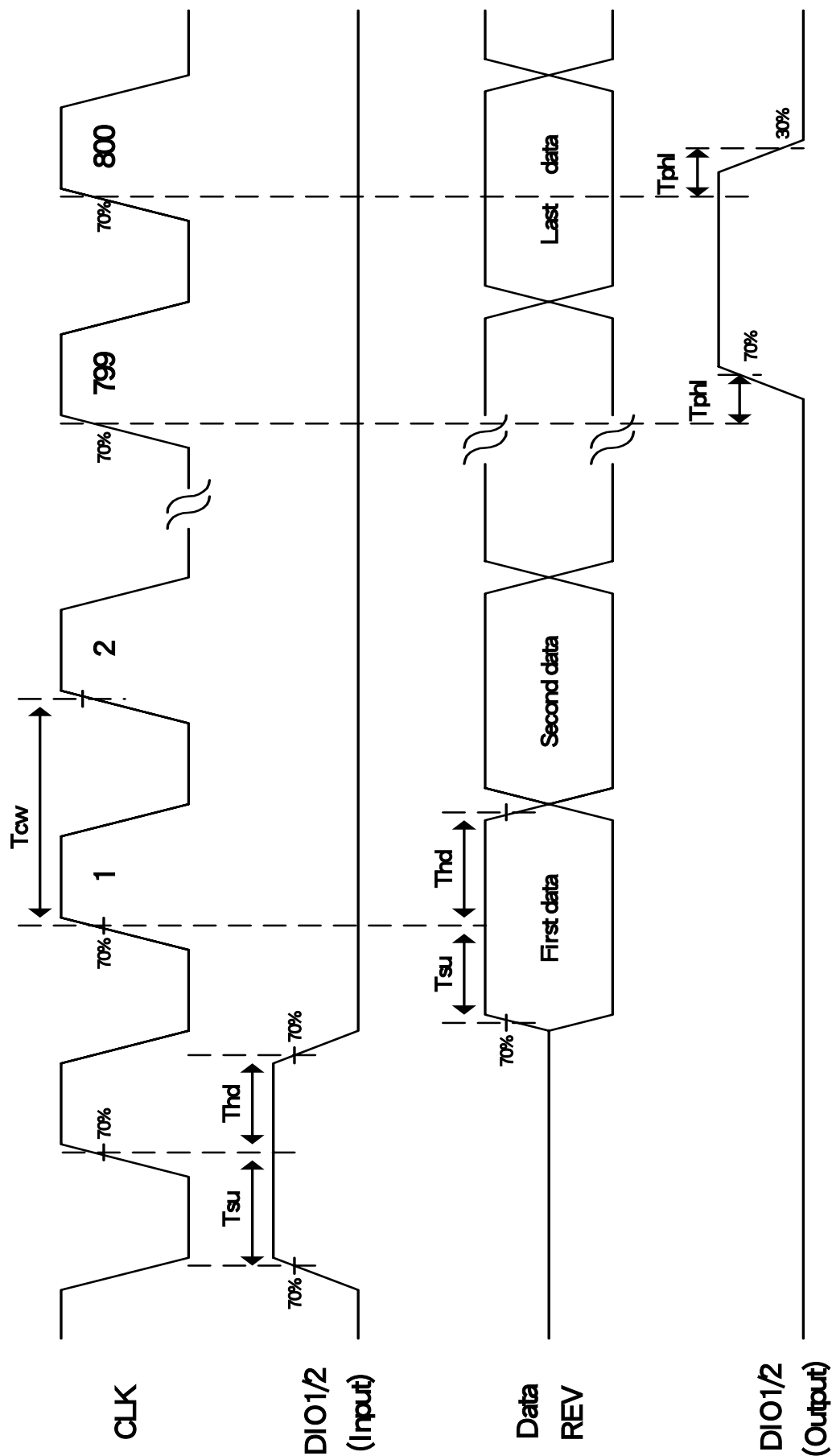


Fig. 11-1 Horizontal timing (1)

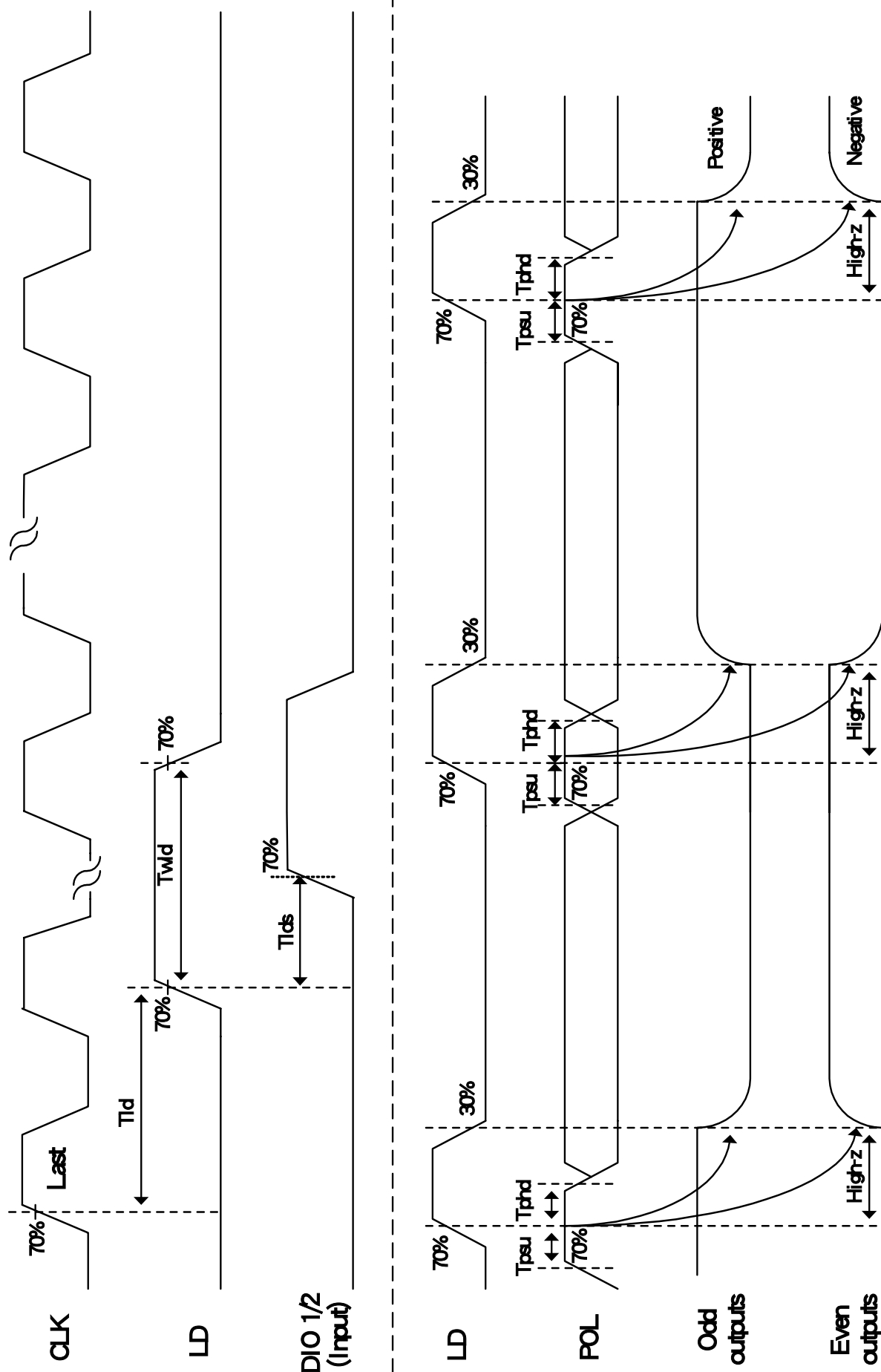


Fig. 11-2 Horizontal timing(2)

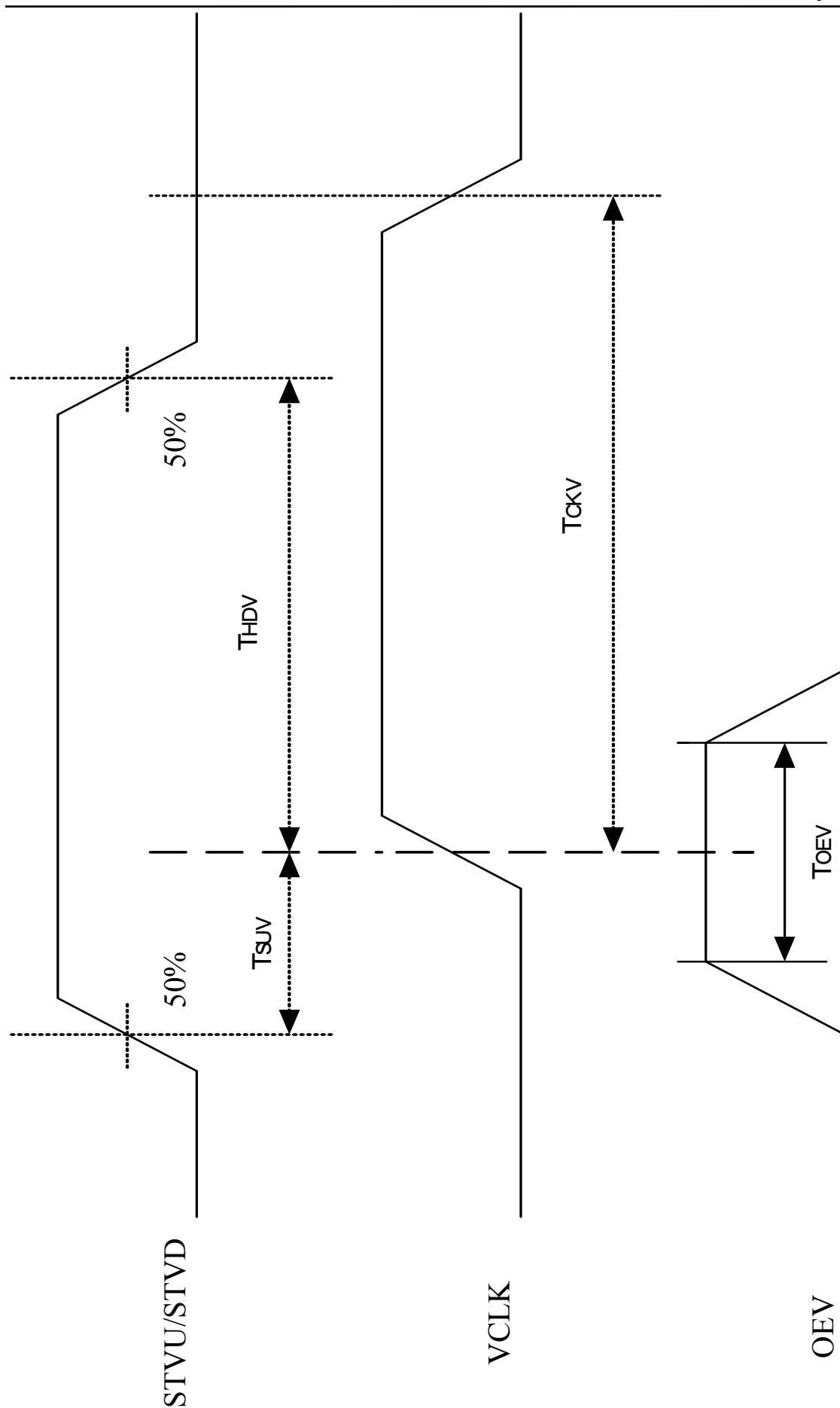


Fig. 11-3 Vertical shift clock timing

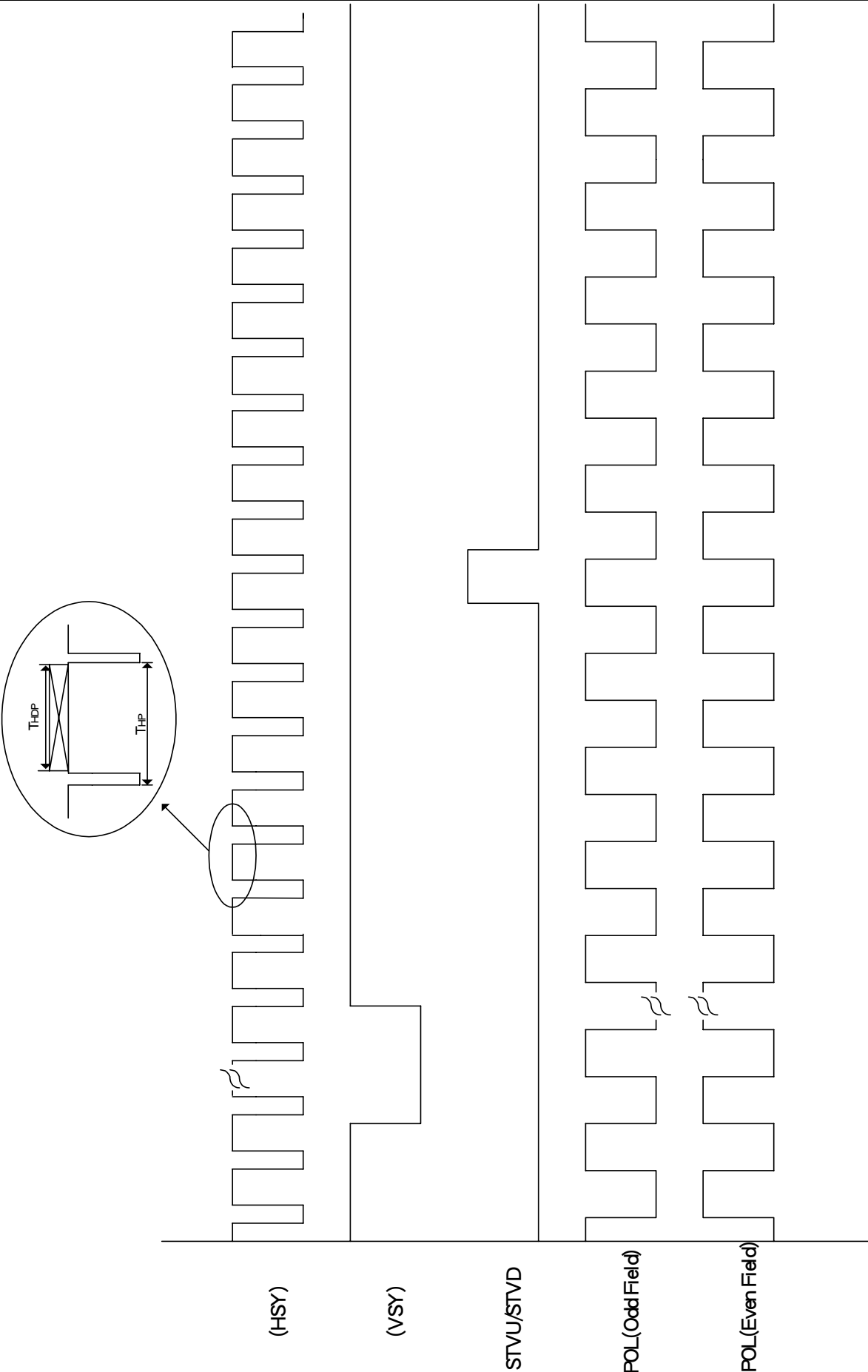
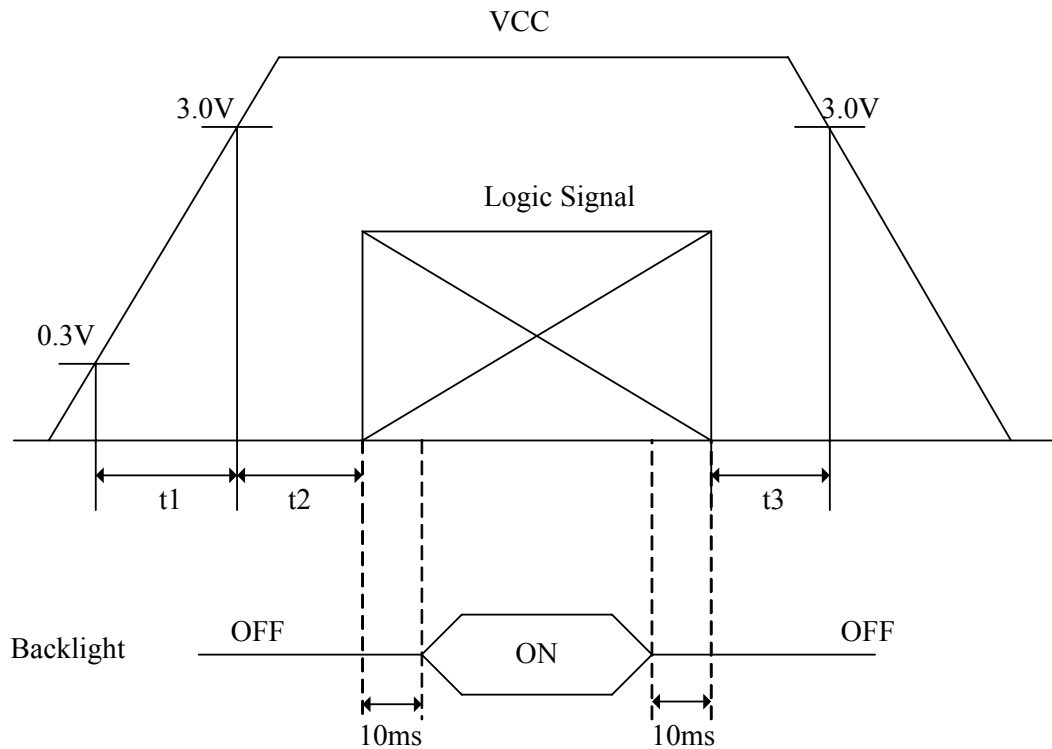


Fig. 11-4 Vertical timing

12. Power On Sequence



1. $0 < t_1 \leq 20\text{ms}$
2. $0 < t_2 \leq 50\text{ms}$
3. $0 < t_3 \leq 1\text{s}$

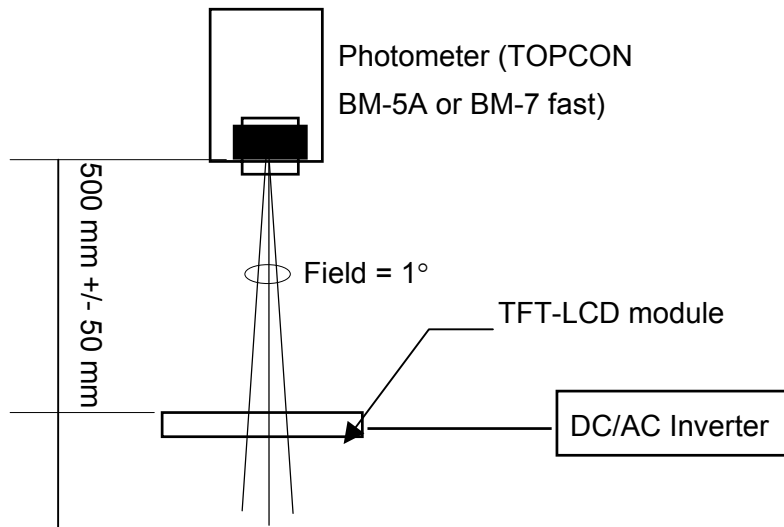
13. Optical Characteristics

13-1) Specification:

$T_a = 25^\circ\text{C}$

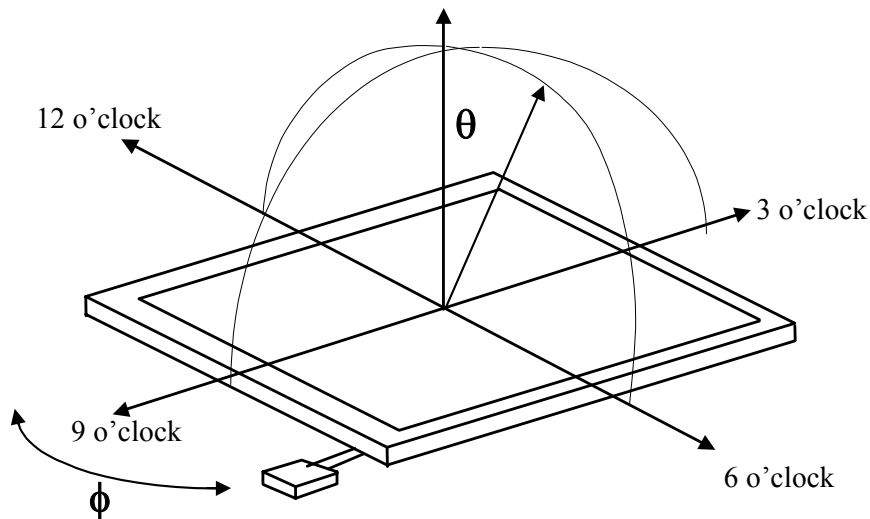
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ	CR≥10	55	60	-	deg	Note 13-1
	Vertical	θ (to 12 'clock)		35	40	-	deg	
		θ (to 6 o'clock)		50	55	-	deg	
Contrast Ratio		CR	Optimum direction	400	500	-	-	Note 13-2
Response time	Rise	Tr	$\theta = 0^{\circ}$	-	15	30	ms	Note 13-4
	Fall	Tf	$\phi = 0^{\circ}$	-	25	50	ms	
Luminance		L	$\theta = 0^{\circ} / \phi = 0^{\circ}$	250	300	-	cd/m ²	Note 13-3
Luminance Uniformity		U	-	75	80	-	%	Note 13-6
White Chromaticity		x	$\theta = 0^{\circ} / \phi = 0^{\circ}$	0.26	0.30	0.34	-	Note 13-3
		y	$\theta = 0^{\circ} / \phi = 0^{\circ}$	0.30	0.34	0.38	-	
LED Life Time		-	25°C	20000	-	-	hrs	Note 13-5
Cross Talk Ratio		CTK	-	-	-	3.5	%	Note 13-7

All the optical measurement shall be executed 30 minutes after backlight being turn-on. The optical characteristics shall be measured in dark room (ambient illumination on panel surface less than 1 Lux). The measuring configuration shows as following figure.



Optical characteristics measuring configuration

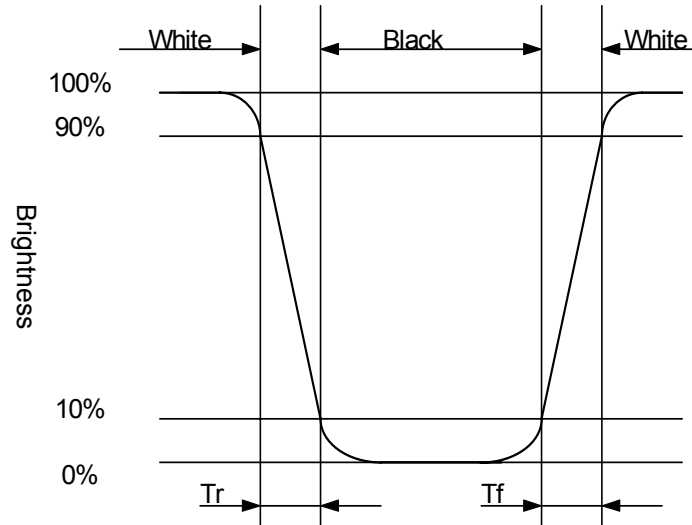
Note 13-1: The definitions of viewing angles are as follow



Note 13-2: The definition of contrast ratio $CR = \frac{\text{Luminance at gray level 63}}{\text{Luminance at gray level 0}}$

Note 13-3: Topcon BM-5A or BM-7 fast luminance meter 1° field of view is used in the testing (after 30 minutes' operation). The typical luminance value is measured at LED current 20 mA.

Note 13-4: Definition of Response Time T_r and T_f

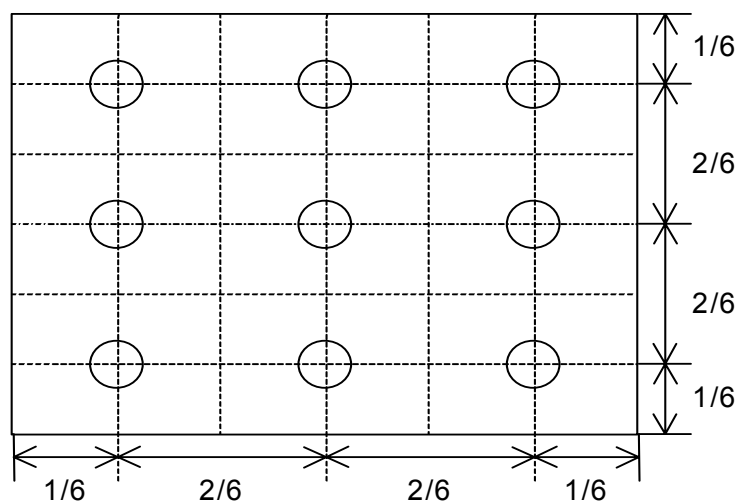


Note 13-5: The “LED Life time “ is defined as the module brightness decrease to 50% original Brightness that the ambient temperature is 25°C and $I_{LED} = 20$ mA.

Note 13-6: The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

 Luminance meter : BM-5A or BM-7 fast(TOPCON)
 Measurement distance : 500 mm +/- 50 mm
 Ambient illumination : < 1 Lux
 Measuring direction : Perpendicular to the surface of module
 The test pattern is white (Gray Level 63).



Note 13-7: Cross Talk (CTK) = $\frac{|YA-YB|}{YA} \times 100\%$

YA: Brightness of Pattern A

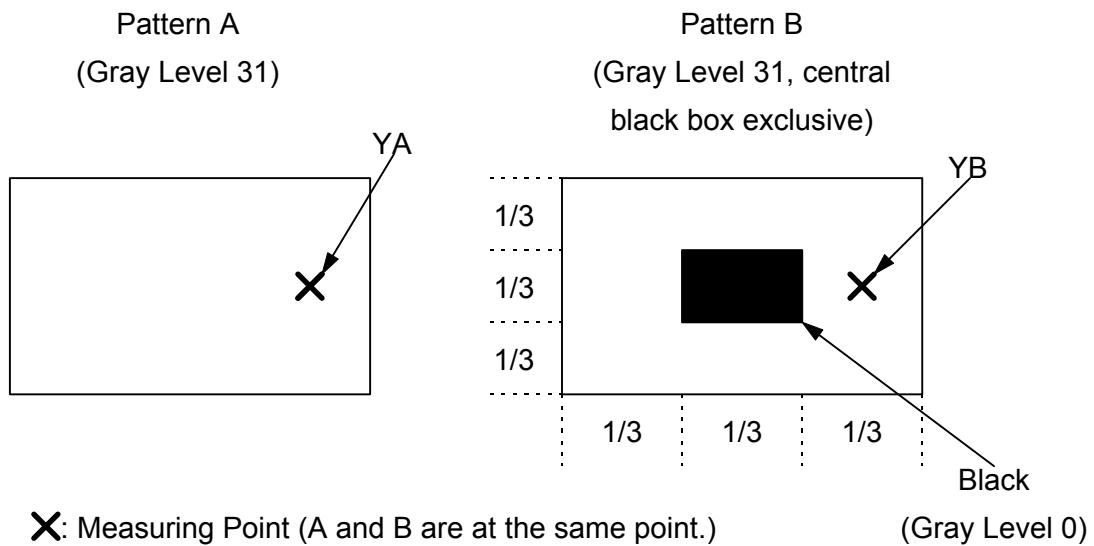
YB: Brightness of Pattern B

Luminance meter : BM 5A or BM-7 fast (TOPCON)

Measurement distance : 500 mm +/- 50 mm

Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module



14. Handling Cautions

14-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
 - 1. The noise from the backlight unit will increase.
 - 2. The output from inverter circuit will be unstable.
 - 3. In some cases a part of module will heat.
- c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

14-2) Precautions in mounting

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

14-3) Adjusting module

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

14-4) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.

14-5) Polarizer mark

The polarizer mark is to describe the direction of wide view angle film how to mach up with the rubbing direction.

15. Reliability Test

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = 80°C, 240 hrs
2	Low Temperature Storage Test	Ta = -30°C, 240 hrs
3	High Temperature Operation Test	Ta = 70°C, 240 hrs
4	Low Temperature Operation Test	Ta = -30°C, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = 60°C, 90%RH, 240 hrs (No Condensation)
6	Thermal Cycling Test (non-operating)	-30°C→80°C, 200 Cycles 30min 30min
7	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz, Amplitude : 1 mm Sweep time: 11 min Test Period: 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction: $\pm X$, $\pm Y$, $\pm Z$ Cycle: 3 times
9	Electrostatic Discharge Test (non-operating)	200pF, 0 Ω $\pm 200V$ 1 time / each terminal

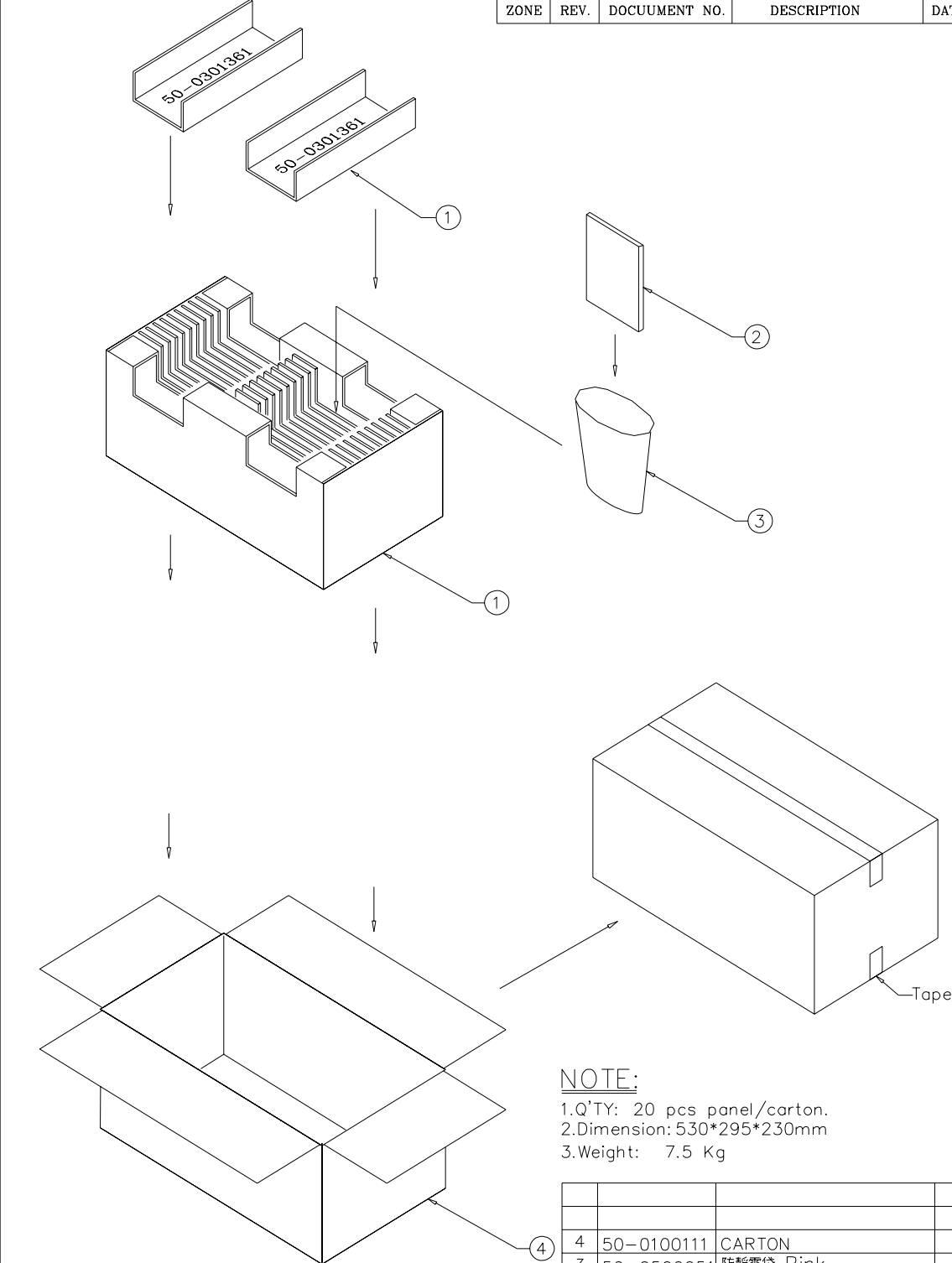
Ta: ambient temperature


Note : The protective film must be removed before temperature test.

[Criteria]

In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image).All the cosmetic specification is judged before the reliability stress.

16. Packing Diagram

ZONE	REV.	DOCUMENT NO.	DESCRIPTION	DATE	REV. BY																									
																														
<p>NOTE:</p> <p>1.Q'TY: 20 pcs panel/carton. 2.Dimension: 530*295*230mm 3.Weight: 7.5 Kg</p>																														
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>ITEM</th> <th>PART NO.</th> <th>DESCRIPTION</th> <th>QTY</th> <th>REMARK</th> </tr> </thead> <tbody> <tr> <td>4</td> <td>50-0100111</td> <td>CARTON</td> <td>1</td> <td></td> </tr> <tr> <td>3</td> <td>50-0500051</td> <td>防静电袋 Pink</td> <td>20</td> <td>抗静电</td> </tr> <tr> <td>2</td> <td></td> <td>PD080SY1 Module</td> <td>20</td> <td></td> </tr> <tr> <td>1</td> <td>50-0301361</td> <td>瓦楞隔板缓冲材</td> <td>1</td> <td>上盖+底座</td> </tr> </tbody> </table>						ITEM	PART NO.	DESCRIPTION	QTY	REMARK	4	50-0100111	CARTON	1		3	50-0500051	防静电袋 Pink	20	抗静电	2		PD080SY1 Module	20		1	50-0301361	瓦楞隔板缓冲材	1	上盖+底座
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4	50-0100111	CARTON	1																											
3	50-0500051	防静电袋 Pink	20	抗静电																										
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MTL.SPEC.		UNSPECIFIED TOL'S		REMARK																										
		ANGLE																												
		ROUGHNESS																												
APPROVE	Frank	'07.07.02	SCALE	UNIT	SHEET																									
CHECK	Frank	'07.07.02			1 OF 1																									
DRAWN	Stevenc	'07.07.02	MTL.NO.		DWG. TITLE																									
					PD080SY1 Module Packing Draw																									
			DWG FILE:		REV. 01																									
					A ₄ SIZE																									


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 Prime View International Co., Ltd.