LCD DIRECT/DUPLEX DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).

The PCF8577 and PCF8577A differ only in their slave addresses.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 9 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A)
- Power-on-reset blanks display

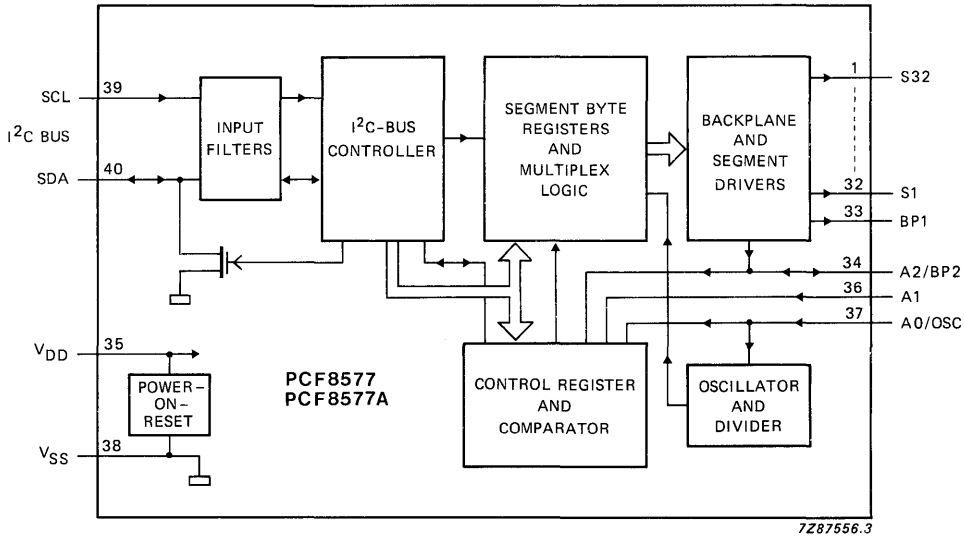


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8577P, PCF8577AP: 40-lead DIL; plastic (SOT129).
PCF8577T, PCF8577AT: 40-lead mini-pack; plastic (VSO40; SOT158A).
PCF8577T, PCF8577AT: in blister tape.
PCF8577U/5, PCF8577AU/5: wafer unsawn.
PCF8577U/10, PCF8577AU/10: chip-on-film frame carrier (FFC).

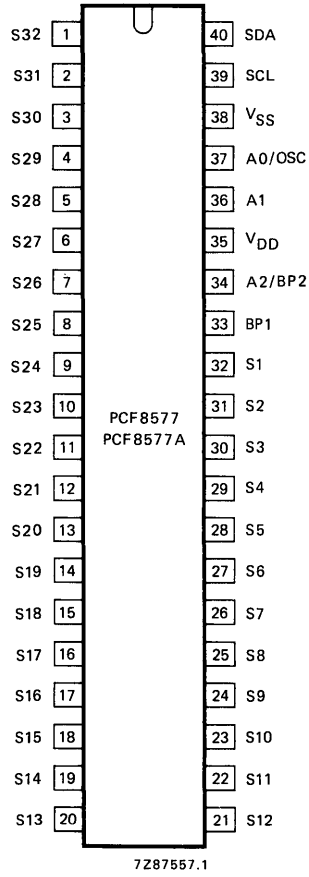


Fig.2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C-bus

40	SDA	I^2C-bus data line
39	SCL	I^2C-bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S32 – S1	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware subaddress A0, A1, A2

The hardware subaddress lines A0, A1, A2 are used to program the device subaddress for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577 the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the cascade mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the cascade mode each PCF8577 is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accesible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There are two slave addresses, one for PCF8577, and one for PCF8577A (see Fig.6). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I²C-bus protocol Fig.7), i.e. all addressed devices respond to control commands sent on the bus.

The control register is shown in more detail in Fig.3. The least-significant bits select which device and which segment byte register is loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware subaddress input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

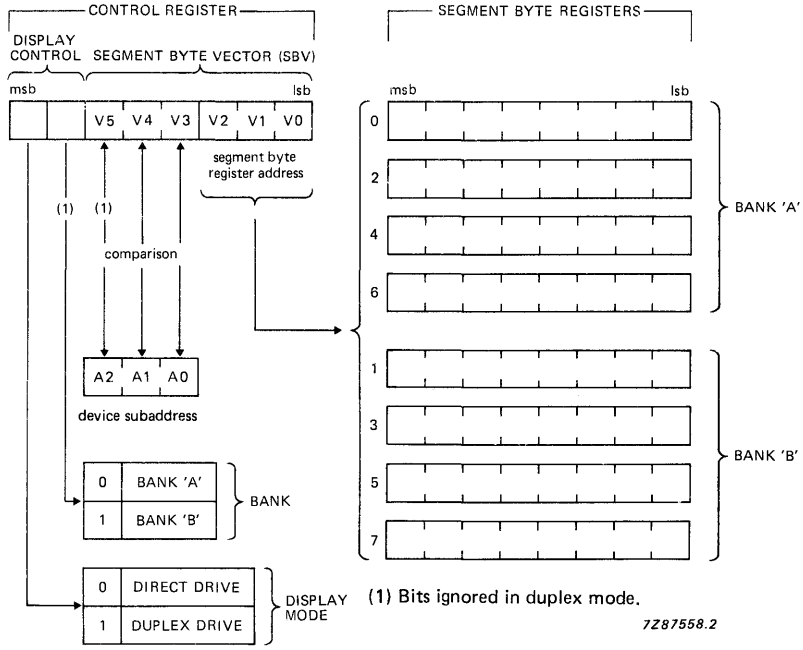


Fig.3 PCF8577 register organization.

FUNCTIONAL DESCRIPTION (continued)

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

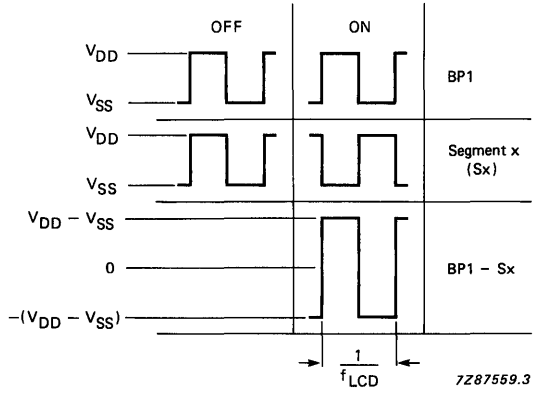
After each segment byte is loaded the SBV is incremented automatically. Thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers in all addressed chips, auto-incremented loading may proceed across device boundaries provided that the hardware subaddresses are arranged contiguously.

Direct drive mode

The PCF8577 is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig.4.



$V_{on(rms)} = V_{DD} - V_{SS}$
$V_{off(rms)} = 0$

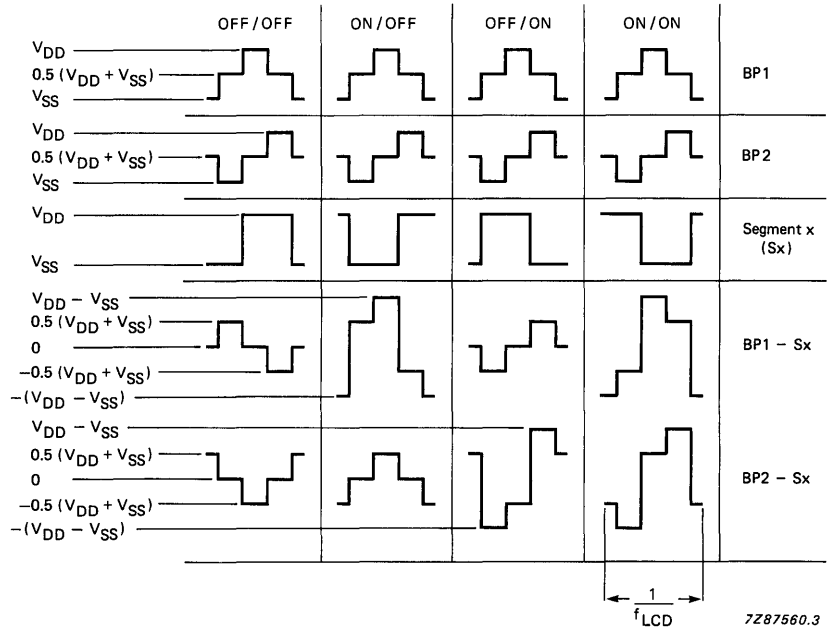
Fig.4 Direct drive mode display output waveforms.

Duplex mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig.5.



$$V_{on(rms)} = 0.791\,(V_{DD} - V_{SS})$$
$$V_{off(rms)} = 0.354\,(V_{DD} - V_{SS})$$
$$\frac{V_{on(rms)}}{V_{off(rms)}} = 2.236$$

Fig.5 Duplex mode display output waveforms.

DEVELOPMENT DATA

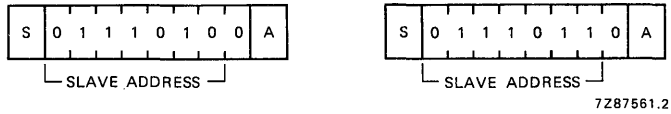
Power-on reset

At power-on reset the PCF8577 resets to a defined starting condition as follows:

1. Both backplane outputs are set to V_{SS} in master mode; to 3-state in cascade mode.
2. All segment outputs are set to V_{SS}.
3. The segment byte registers and control register are cleared.
4. The I²C-bus interface is initialized.

Slave address

The slave address for PCF8577 and PCF8577A are shown in Fig.6.



(a) PCF8577 (b) PCF8577A

Fig.6 PCF8577 and PCF8577A slave addresses.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

I²C-bus protocol

The PCF8577 I²C-bus protocol is shown in Fig.7.

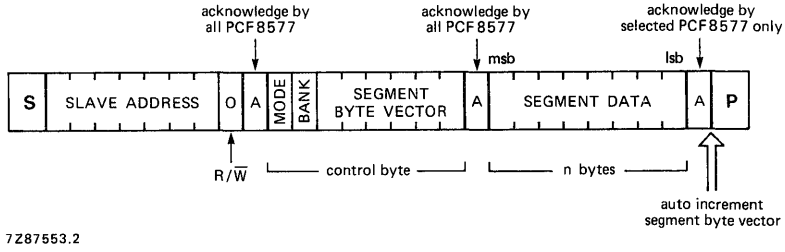


Fig.7 I²C-bus protocol.

The PCF8577 is a slave receiver and has a fixed slave address (Fig.6). All PCF8577s with the same slave address acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. All addressed devices acknowledge the control byte. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

DEVELOPMENT DATA

Display memory mapping

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode.

Table 1 Segment byte-segment driver mapping in the direct drive mode

MODE	BANK	V2	V1	V0	segment register / bit	MSB 7	6	5	4	3	2	1	LSB 0	backplane
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

In duplex mode even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2 Segment byte; segment driver mapping in the duplex mode

MODE	BANK	V2	V1	V0	segment register / bit	MSB 7	6	5	4	3	2	1	LSB 0	backplane
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

X = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

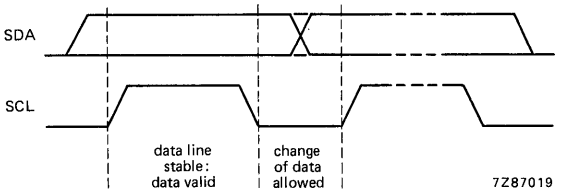


Fig.8 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

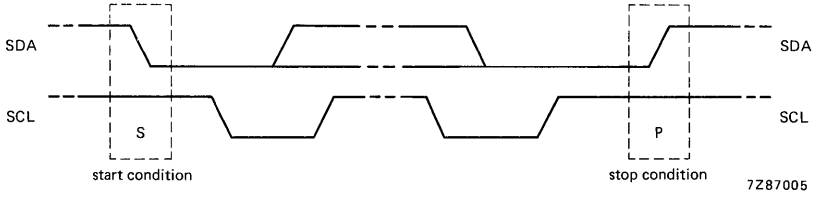


Fig.9 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

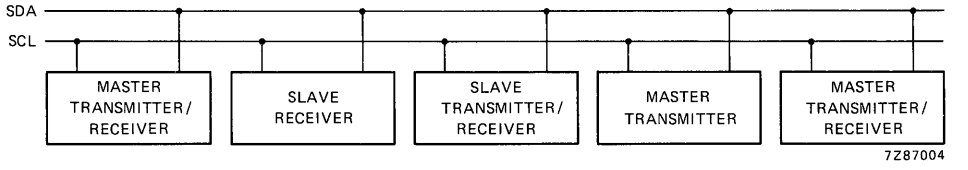


Fig.10 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

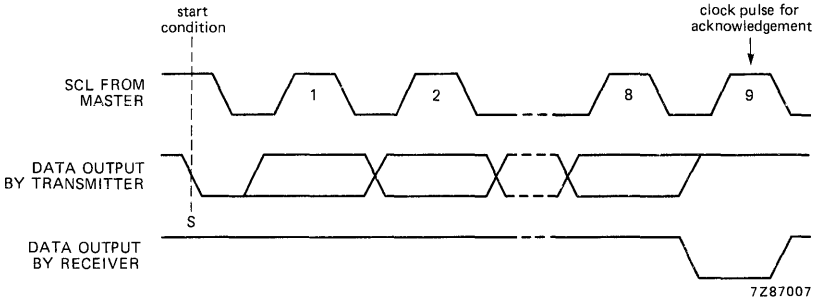


Fig.11 Acknowledgement on the I²C-bus.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+11.0	V
Voltage on pin	V_I	−0.5	V_{DD} + 0.5	V
V_{DD} or V_{SS} current	I_{DD}; I_{SS}	−50	+ 50	mA
DC input current	I_I	−20	+ 20	mA
DC output current	I_O	−25	+ 25	mA
Power dissipation per package	P_{tot}	−	500*	mW
Power dissipation per output	P_o	−	100	mW
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* Derate 7.7 mW/K when $T_{amb} > 60$ °C.

DC CHARACTERISTICS

V_{DD} = 2.5 to 9.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.*	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	9.0	V
Supply current	non specified inputs at V_{DD} or V_{SS}					
at f_{SCL} = 100 kHz	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF	I_{DD1}	–	80	250	μA
at f_{SCL} = 0	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF	I_{DD2}	–	25	150	μA
at f_{SCL} = 0	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD3}	–	25	40	μA
at f_{SCL} = 0	no load; A0/OSC = V_{DD} or V_{SS}	I_{DD4}	–	10	20	μA
Power-on reset level	note 1	V_{POR}	–	1.1	2.0	V
Input A0						
Input voltage LOW		V_{IL1}	0	–	0.05	V
Input voltage HIGH		V_{IH1}	V_{DD}−0.05	–	V_{DD}	V
Input A1						
Input voltage LOW		V_{IL2}	0	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH2}	0.7 V_{DD}	–	V_{DD}	V
Input A2						
Input voltage LOW		V_{IL3}	0	–	0.10	V
Input voltage HIGH		V_{IH3}	V_{DD}−0.10	–	V_{DD}	V
Inputs SCL; SDA						
Input voltage LOW		V_{IL4}	0	–	0.08	V
Input voltage HIGH		V_{IH4}	2.0	–	9.0	V
Input capacitance	note 2	C_I	–	–	7	pF
Output SDA						
Output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	3.0	–	–	mA
A1; SCL; SDA						
Leakage current	V_I = V_{DD} or V_{SS}	$+I_{L1}$	–	–	1	μA
A2; BP2						
Leakage current	V_I = V_{SS}	I_{L2}	–	–	1	μA
Pull-down current	V_I = V_{DD}	$-I_{L2}$	–	1.5	5	μA

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

parameter	conditions	symbol	min.	typ.*	max.	unit
A0/OSC						
Leakage current	$V_I = V_{DD}$	$-I_{L3}$	–	–	1	μA
Oscillator						
Start-up current	$V_I = V_{SS}$	I_{OSC}	–	1.2	5	μA
LCD outputs						
DC component of LCD driver		$\pm V_{BP}$	–	20	–	mV
Segment output current	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	0.3	–	–	mA
	$V_{OH} = V_{DD}$ −0.4 V; V_{DD} = 5 V	$-I_{OH}$	0.3	–	–	mA
Backplane output resistance (BP1; BP2)	$V_O = V_{SS}$, V_{DD}, $(V_{SS}+V_{DD})/2$; note 3	R_{BP}	–	0.4	5	kΩ

AC CHARACTERISTICS (note 2)

V_{DD} = 2.5 to 9.0 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.*	max.	unit
Display frequency	C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz
Driver delays with test loads	V_{DD} = 5 V	t_{BS}	–	20	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time		$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	1.3	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.7	–	–	μs

DEVELOPMENT DATA

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

Notes to the characteristics

1. Resets all logic when $V_{DD} < V_{POR}$.
2. Periodically sampled, not 100% tested.
3. Outputs measured one at a time; V_{DD} = 5 V; I_{load} = 100 μA.
4. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

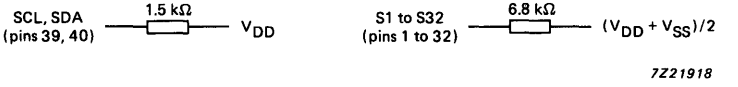


Fig.12 Test loads.

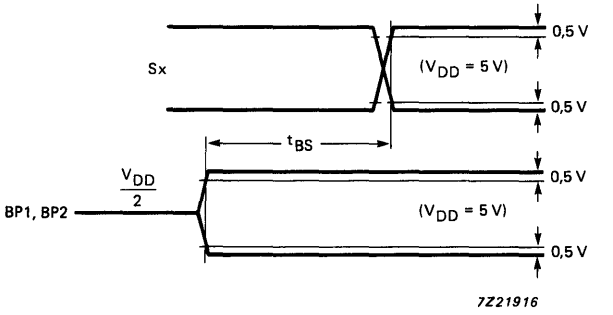


Fig.13 Driver timing waveforms.

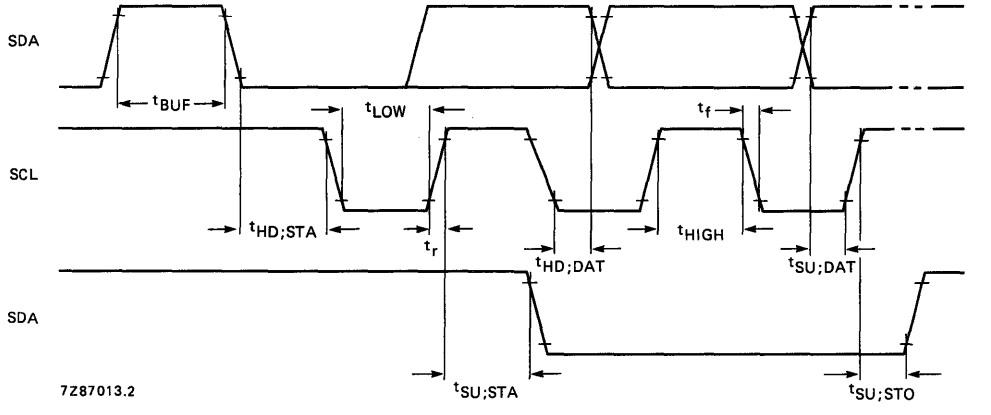


Fig.14 I^2C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

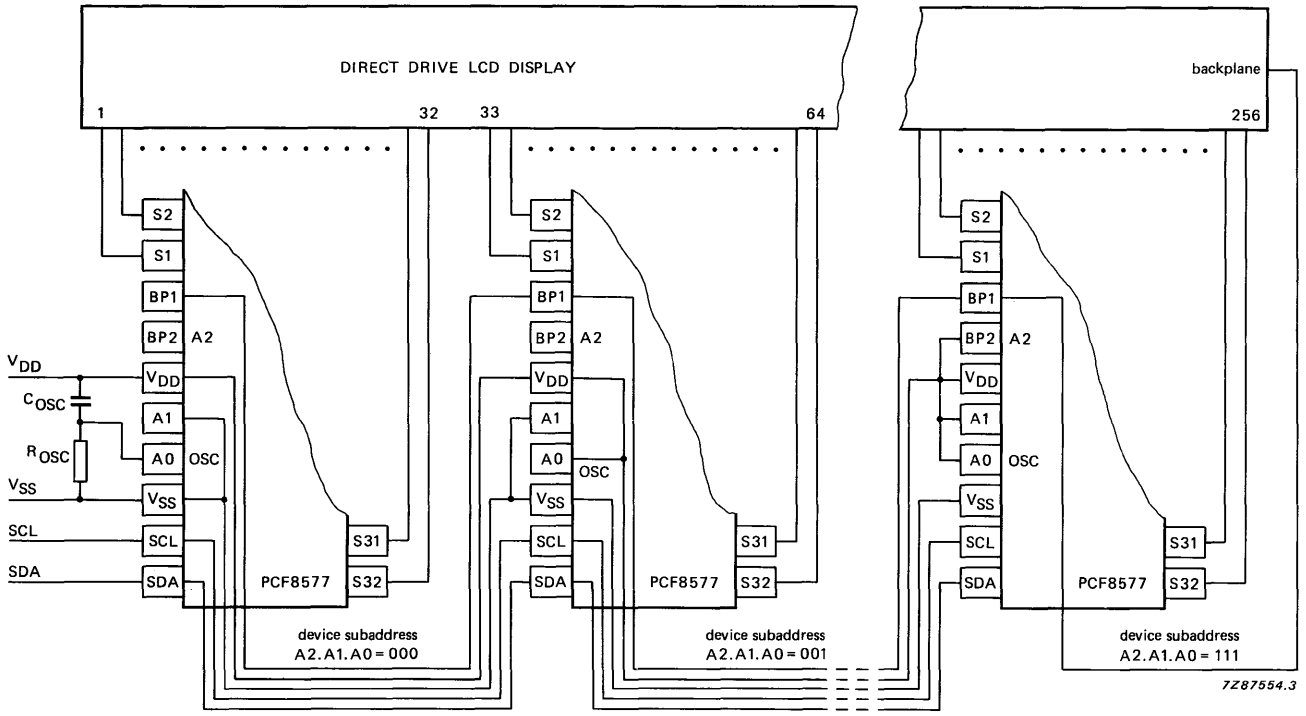


Fig.15 Direct drive display; expansion to 256 segments using eight PCF8577.

APPLICATION INFORMATION (continued)

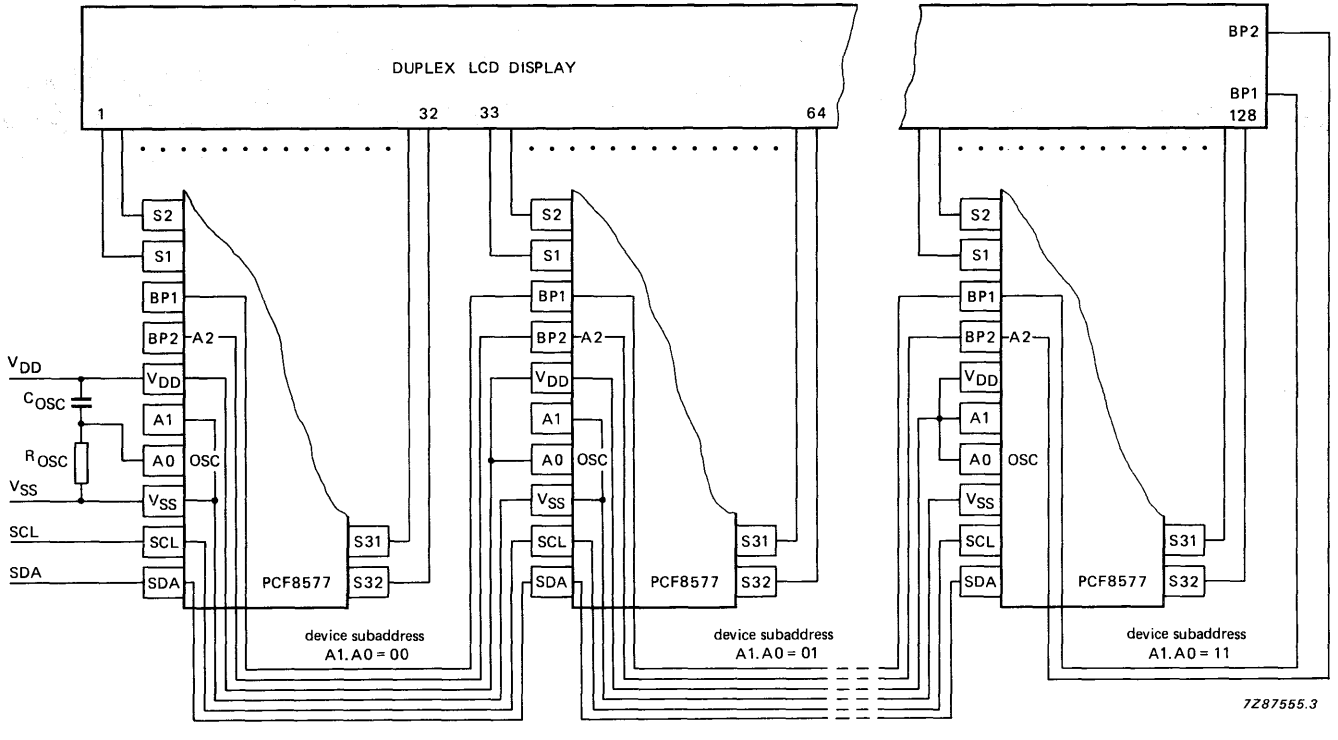
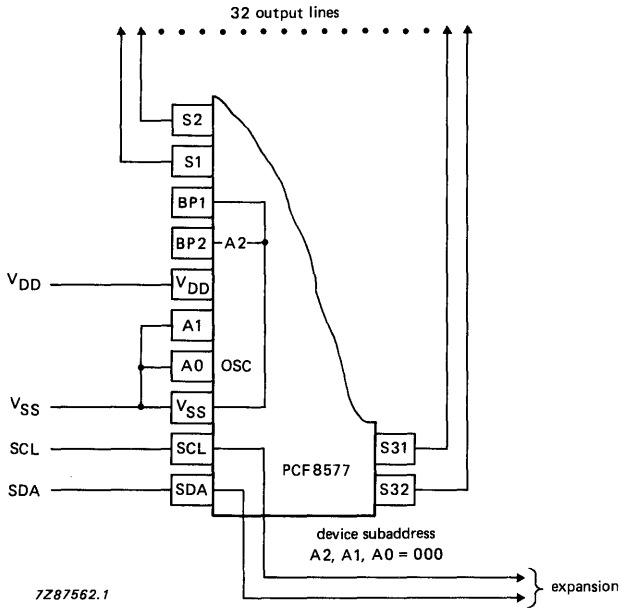


Fig.16 Duplex display; expansion to 2 x 128 segments using four PCF8577.



Notes

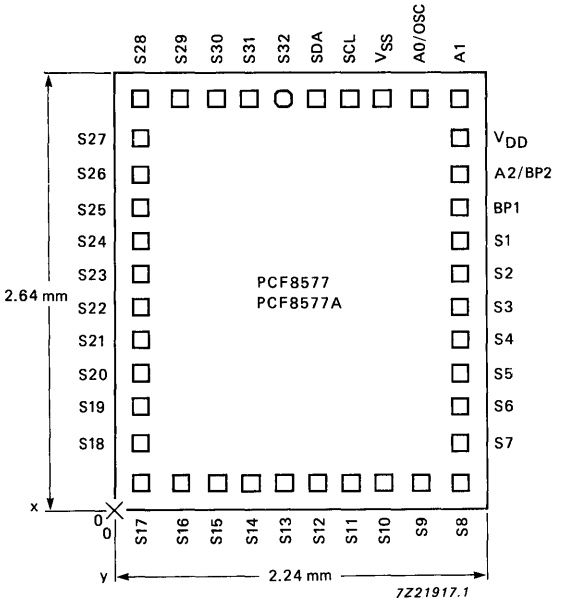
1. MODE bit must always be set to logic 0 (direct drive).
2. BANK switching is permitted.
3. BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation).

Fig.17 Use of PCF8577 as 32-bit output expander in I²C-bus application.

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 5.91 mm^2

Bonding pad dimensions: 120 μm x 120 μm

Fig.18 Bonding pad locations.

Table 3 Bonding pad locations (dimensions in μm)

All x/y coordinates are referenced to bottom corner, see Fig.18.

pad	X	Y	pad	X	Y
S32	1020	2480	S12	1220	160
S31	820	2480	S11	1420	160
S30	620	2480	S10	1620	160
S29	400	2480	S9	1840	160
S28	160	2480	S8	2080	160
S27	160	2240	S7	2080	400
S26	160	2020	S6	2080	620
S25	160	1820	S5	2080	820
S24	160	1620	S4	2080	1020
S23	160	1420	S3	2080	1220
S22	160	1220	S2	2080	1420
S21	160	1020	S1	2080	1620
S20	160	820	BP1	2080	1820
S19	160	620	A2/BP2	2080	2020
S18	160	400	V_{DD}	2080	2240
S17	160	160	A1	2080	2480
S16	400	160	A0/OSC	1840	2480
S15	620	160	V_{SS}	1620	2480
S14	820	160	SCL	1420	2480
S13	1020	160	SDA	1220	2480