Crystal Image through
Imaging Innovation
PIXELPLUS

Preliminary
Datasheet

1/3 inch SD Single Chip
CMOS Image Sensor with NTSC/PAL Transmitter

PC4089K

Rev 0.2

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Features

- 728 x 488 effective pixel array with RGB bayer color filters and micro-lens
- Interface
  - Composite Output
    - CVBS(NTSC/PAL)
  - Digital Output
    - YCbCr422 / RGB565 / RGB444 / Bayer
  - Analog/Digital Output
    - ITU-R. BT656 / CVBS
- Image processing on chip : lens shading compensation, gamma correction, defect correction, color correction, NR(2D noise reduction), color interpolation, edge enhancement, brightness, contrast, de-color, auto black level compensation, auto white balance, auto exposure control, back light compensation
- Programmable frame size, window size and position
- Free scaling (scale down)
- Horizontal/Vertical mirroring
- Automatic flicker cancellation
- Smart IR-LED/TDN(moving) filter controller
- 4 overlay functions by using SPI ROM
- I2C master included
- SPI master included
- Software reset
- On chip regulator for core
- Crystal input support
- CLCC package type supports

General Description

The PC4089K is a 1/3-inch CMOS image sensor with NTSC/PAL Transmitter. It is a single chip with effective pixel array of 728 (width) x 488 (height). The PC4089K can generate analog/digital/composite outputs at maximum frame rate of 60. On-chip sensor functions can be controlled through I2C interface.

Table 1 Key Performance Parameter

Parameter	Typical value
Pixel size	6.2 [um] x 7.40 [um]
Effective pixel array	728 (H) x 488 (V)
Effective image area	4.623 [mm] x 3.611 [mm]
Optical format	1/3 [inch]
Input clock frequency	27~54 [MHz]
Output interface	10/8-bit parallel
	CVBS(NTSC/PAL)
Max. frame rate	60fps : ITU-R. BT656 @ 27[MHz] (for NTSC)
	50fps : ITU-R. BT656 @ 27[MHz] (for PAL)
	60fields/sec : NTSC @ 27[MHz]
	50fields/sec : PAL @ 27[MHz]
	60fps : YCbCr422/RGB565/RGB444 @ 54[MHz]
	60fps : Bayer @ 27[MHz]
Dark signal	37.9 [mV/sec]
Sensitivity	19.5 [V/Lux.sec]
Power supply	AVDD : 3.3 [V]
	HVDD : 3.3 [V]
	CVDD : 3.3 [V]
	DVDD : 1.5 [V]
Power consumption	298 [mW] @ dynamic
	534.9 [uW] @ standby
Operating Temp. (fully functional Temp.)	-40~105 [°C]
Dynamic range	64.4 [dB] @ 60 [°C]
SNR	50 [dB]

Chip Architecture

The PC4089K has a 732 x 504 total pixel array and includes column/row driver circuits for reading out pixel data progressively. CDS circuit reduces noises generated from various sources, which mainly are resulted from process variations. The fixed errror signal level caused by pixel process variation can be reduced by sampling the defference between the output and the reset level of the pixel. Each of R, G, and B pixel output can be multiplied by different gain factors to balance the color of images under various light conditions. The analog signals are converted into digital data of one line at a time and each line data is streamed out column by column. The Bayer RGB data passes through a sequence of image signal processing to produce various output datas. Image signal processing includes operations such as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. The PC4089K supports various interfaces such as composite, analog, and digital output. The control of internal functions and output signal timings can be enabled by modifying registers directly through a 2-wire serial interface called I2C or by programming the internal/external ROMs which contain device settings.

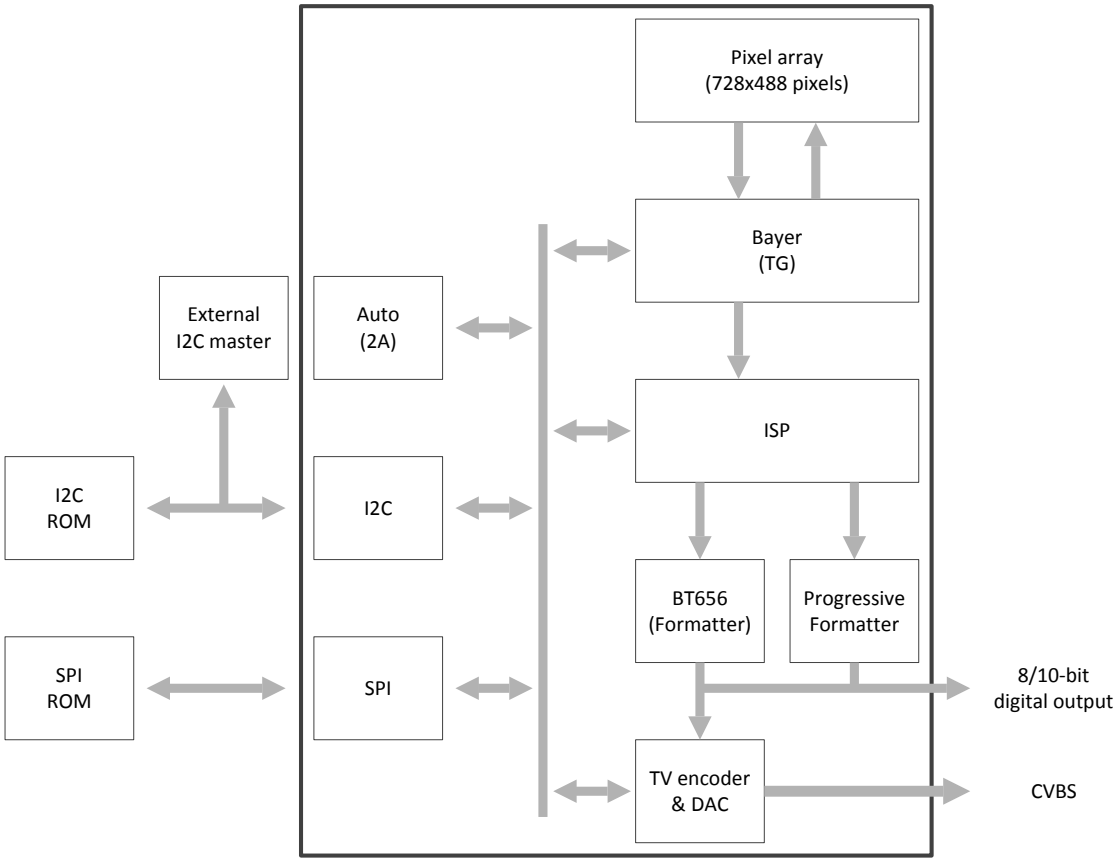

Figure 1 Chip architecture

Frame Structure

The size of a frame is determined by framewidth and frameheight registers. One frame consists of (framewidth + 1) columns and (frameheight + 1) rows, where the size of one frame is allowed to be larger than the total pixel array size. Window determines the output image size, and its default size is 720 x 480 pixels. It is possible to define a specific region of the frame by a determined window. Pixel scanning is performed row by row on entire frame. Frame row counter and frame column counter, which are limited by framewidth and frameheight values respectively, are used to indicate the current coordinate of pixel being scanning. The column counter value increase by every pixel clock (pclk). every time the column counter reaches maximum value, the row counter value increase. Figure 2 shows the default frame structure and the window position of the PC4089K with origin point (0,0) in the top right corner .

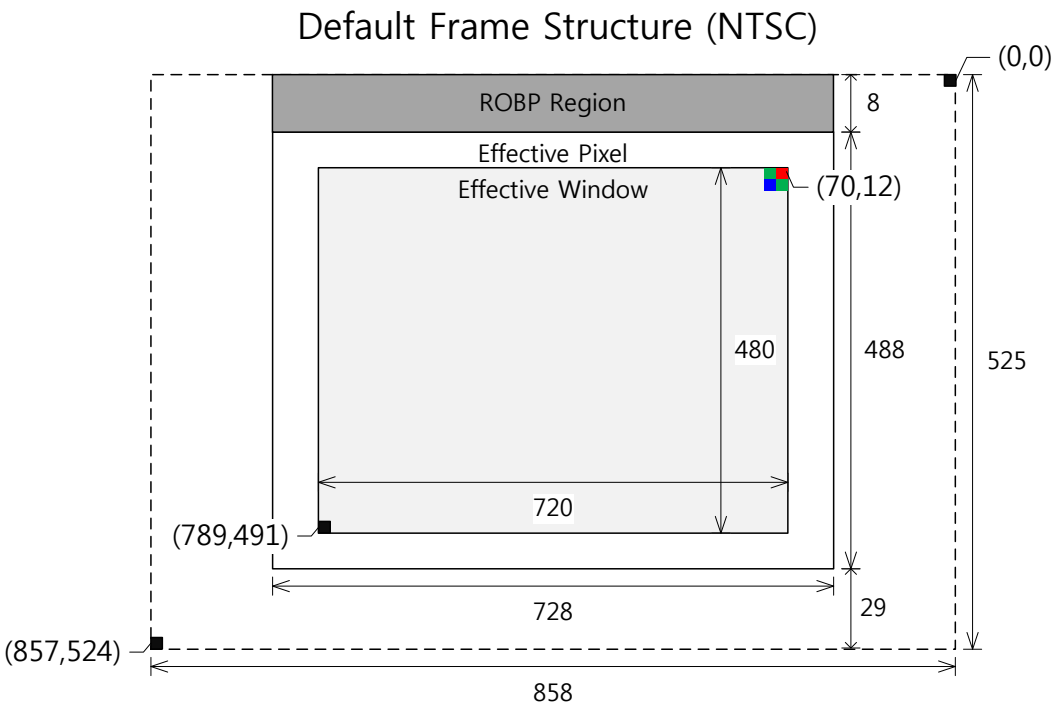

Figure 2 Default frame structure(top view)