PIXELPLUS CO., LTD.

Preliminary
Data sheet

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

PC3030K

Rev 0.5

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6th Floor, Gyeonggi R&DB Center, 906-5 Iui-dong, Yeongtong-gu,
Suwon-si, Gyeonggi-do, 443-766, Korea
Tel : 82-31-888-5300, FAX : 82-31-888-5398

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ *Revision History*

Version	Date [D/M/Y]	Notes	Writer
0.0	29/11/2010	*(Preliminary)*	Changwoo Seo
0.1	23/12/2010	Revised typical parameter (page.5)	Heungseok Park
0.2	24/02/2011	Edited register table and detail information	Chang hui Ye
0.3	07/03/2011	Add typical parameter (DC,Optical item)(page. 5)	Heungseok Park
0.4	14/03/2011	Edited register table and detail information	DS Min
0.5	27/04/2011	Modified register table on page 120	Soo-Beom Son
0.6	28/11/2011	Change HVDD Power (page. 5~6)	Heungseok Park

Caution : This datasheet can be changed without prior notice !! If you want to get up-to-date version, please contact localized pixelplus agent.

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

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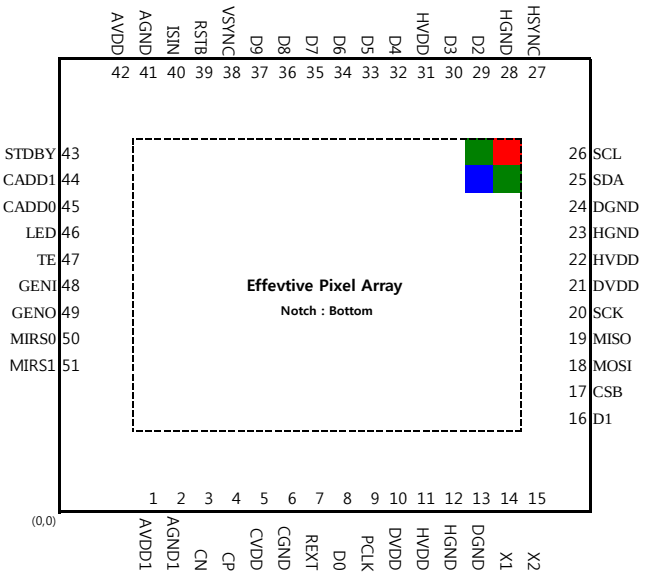
1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Features

- ▷ 682 x 504 total pixel array with RGB bayer color filters and micro-lens.
- ▷ Power supply : AVDD : 2.8V, HVDD : 3.3V, CVDD : 2.8V
- ▷ Output formats :
  - ◆ Composite Output mode :
    - CVBS (NTSC/PAL),
  - ◆ Digital Output mode :
    - max. VGA (640x480) YCbCr422/RGB565/ RGB444. (progressive, 60 fps @ 54MHz)
    - max. VGA (640x480) Bayer (progressive, 60 fps @ 27MHz)
  - ◆ Analog/Digital Output mode :
    - ITU-R. BT656 (720x240/288) (interlaced, 60 fields @ 27MHz)
    - CVBS (30 fps @ 27MHz)
- ▷ Image processing on chip : lens shading, gamma / defect / color correction, low pass filter, color interpolation, saturation, edge enhancement, brightness, contrast, special effects, auto black level , auto white balance, auto exposure control and back light compensation.
- ▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus.
- ▷ VGA / QVGA / QQVGA / CIF / QCIF Scaling.
- ▷ High Image Quality and Ultra low light performance.
- ▷ I2C master include.
- ▷ Motion detection support
- ▷ Alarm mode, Privacy mode support
- ▷ Artificial Intelligence power save mode.
- ▷ Chip Address Selection PADs
- ▷ Horizontal / Vertical mirroring.
- ▷ 50Hz, 60Hz flicker automatic cancellation.
- ▷ Software Reset.
- ▷ External Sync (Gen. Lock) support
- ▷ Off-chip IR-LED control.
- ▷ Crystal input support.
- ▷ On chip regulator for DVDD.
- ▷ CSP/CLCC/PLCC Package type supports



[Fig. 1] PIN Description

Total Pixel Array	682 (H) x 504(V)
Effective Pixel Array	648(H) x 488(V)
Pixel Size	6 um x 6 um
Effective Image Area	3.8 mm x 2.9 mm (Diagonal :4.86mm)
Optical Format	1/3.7 inch , RGB Bayer filter
Max. Clock frequency	54 MHz
Max. Frame Rate	- 60fps, 640x480 YCbCr @ 54MHz - 60fps, 640x480 Bayer @ 27MHz - 60field, 720x240(288) YCbCr @ 27MHz - CVBS 30 fps @ 27MHz
Dark Signal	11.0 [mV/sec] @60℃
Sensitivity	8.0 [V/Lux.sec]
Power Supply	Analog : 2.8V, HVDD : 3.3V, CVDD : 2.8V
Power Consumption	225.9 mW @Dynamic 416.9 uW @Standby
Operating Temp. (Fully Functional Temp)	-40 ~ 105 [℃]
Dynamic Range	64.4 [dB]
SNR	47.2 [dB]

[Table 1] Typical Parameters

▶ PIN Descriptions

Num	NAME	I/O Type	PAD Description
1	AVDD1	P	Analog VDD1 :2.8V DC.
2	AGND1	P	Analog Ground1
3	CN	O	Composite Differential Negative signal (75 ohm single termination(LCD), 37.5 ohm double termination (CRT))
4	CP	O	Composite Differential Positive signal. (75 ohm single termination(LCD), 37.5 ohm double termination (CRT))
5	CVDD	P	DAC power supply : 2.8V DC
6	CGND	P	DAC power ground
7	REXT	I	External Resistor. The resistor value can be changed by user tuning. (Typically 30k ohm when CN/CP 37.5 ohm termination, 60k ohm when CN/CP 75 ohm termination)
8	D0	I/O	Mirror Strap Input bit 0 / Digital Output bit 0, Motion detection signal out
9	PCLK	O	Pixel clock. Data can be latched by external devices at the rising or falling edge of PCLK. The polarity can be controlled anyway.
10	DVDD	P	Digital Power supply : In case of using on-chip digital regulator, DVDD must be tied to DGND by total 1uF bypass capacitor. Otherwise, 1.5V DC must be supplied with 100nF to DGND.
11	HVDD	P	Digital VDD for I/O : 3.3V. Voltage range for all output signals is (0V or HVDD)
12	HGND	P	Digital GND for I/O
13	DGND	P	Digital GND for core
14	X1	I	Crystal input pad or Master clock input pad
15	X2	O	Crystal output pad *(1)
16	D1	I/O	Mirror Strap Input bit 1 / Digital Output bit 1
17	CSB	O	Chip Select Signal for Serial Peripheral Interface(SPI)
18	MOSI	O	Data Output for Serial Peripheral Interface(SPI)
19	MISO	I	Data Input Signal for Serial Peripheral Interface(SPI)
20	SCK	O	Clock Signal for Serial Peripheral Interface(SPI)

(1) In case of using External clock, crystal output pad(X2) must be floated and clock input PAD is X1.

[Table 2] Pin Descriptions (continue)

21	DVDD	P	Digital Power supply : In case of using on-chip digital regulator, DVDD must be tied to DGND by total 1uF bypass capacitor. Otherwise, 1.5V DC must be supplied with 100nF to DGND.
22	HVDD	P	Digital VDD for I/O. Voltage range for all output signals is (0V~HVDD)
33	HGND	P	Digital GND for I/O
24	DGND	P	Digital GND for core
25	SDA	I/O	2-wire serial interface data.
26	SCL	I/O	2-wire serial interface clock.
27	HSYNC	O	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
28	HGND	P	Digital GND for I/O
29	D2	I/O	TV Strap Input bit 0 / Digital Output bit 2
30	D3	I/O	TV Strap Input bit 1 / Digital Output bit 3
31	HVDD	P	Digital VDD for I/O. Voltage range for all output signals is (0V~HVDD)
32	D4	I/O	TV Strap Input bit 2 / Digital Output bit 4
33	D5	I/O	Flicker Strap Input bit 0 / Digital Output bit 5
34	D6	I/O	Flicker Strap Input bit 1 / Digital Output bit 6
35	D7	I/O	BLC Strap Input / Digital Output bit 7
36	D8	I/O	Indoor/Outdoor Strap Input / Digital Output bit 8
37	D9	I/O	OSD Strap Input / Digital Output bit 9
38	VSYNC	I/O	Master Enable Strap Input / Vertical sync : Indicates the start of a new frame
39	RSTB	I	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
40	ISIN	I	Illumination sensor input (must be under 1.1V).
41	AGND	P	Analog Ground
42	AVDD	P	Analog VDD : 2.8V DC
43	STDBY	I	Power stdby mode. When Stdby ='1', there's no current flow in any analog circuit branch, neither any beat of digital clock.
44	CADD1	I	Chip Address selection bits [1:0], Default [11]
45	CADD0	I	
46	LED	O	LED provides the enable signal which can turn-on LED device when low light condition
47	TE	I	Chip Test mode enable.
48	GENI	I	External Frame sync input. Slave chip can receive the external frame sync signal from master chip
49	GENO	O	External Frame sync output. Master chip can output the external frame sync signal through this pad to synchronize all digital outputs of two or more chips
50	MIRS0	O	Moving IR/AR Transition Switch Control PADs
51	MIRS1	O	

[Table 2] Pin Descriptions

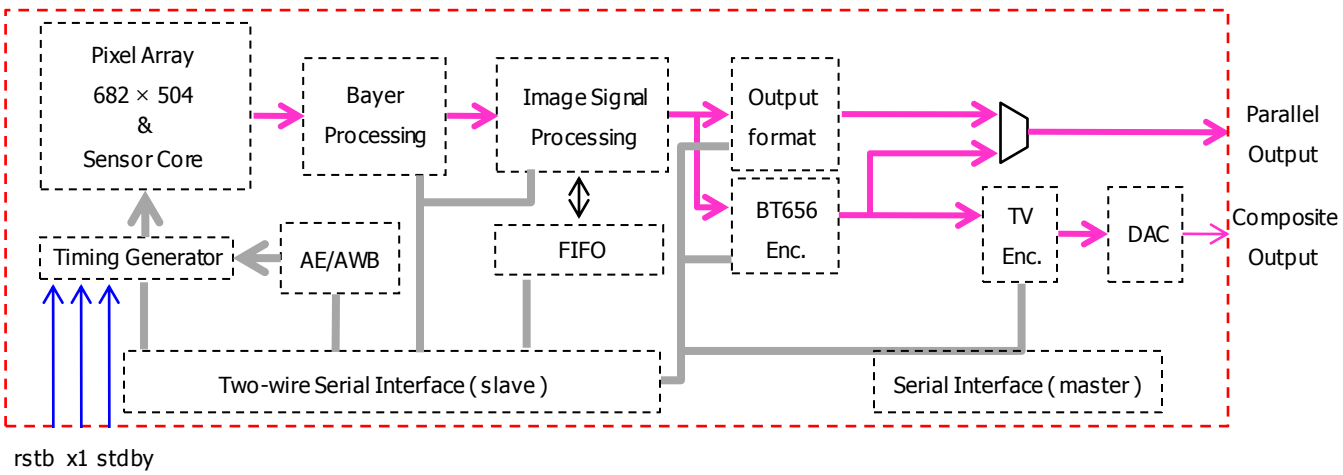
1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Signal Environment

PC3030K has 2.8V tolerant Input pads. Input signals must be higher than or equal to HVDD but cannot be higher than 2.8V. PC3030K input pad has built in reverse current protection circuit, which makes it possible to apply input voltage even if the HVDD is disconnected or floating. Voltage range for all output signals is 0V ~ HVDD.

▶ Chip Architecture

PC3030K has 682 x 504 total pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.



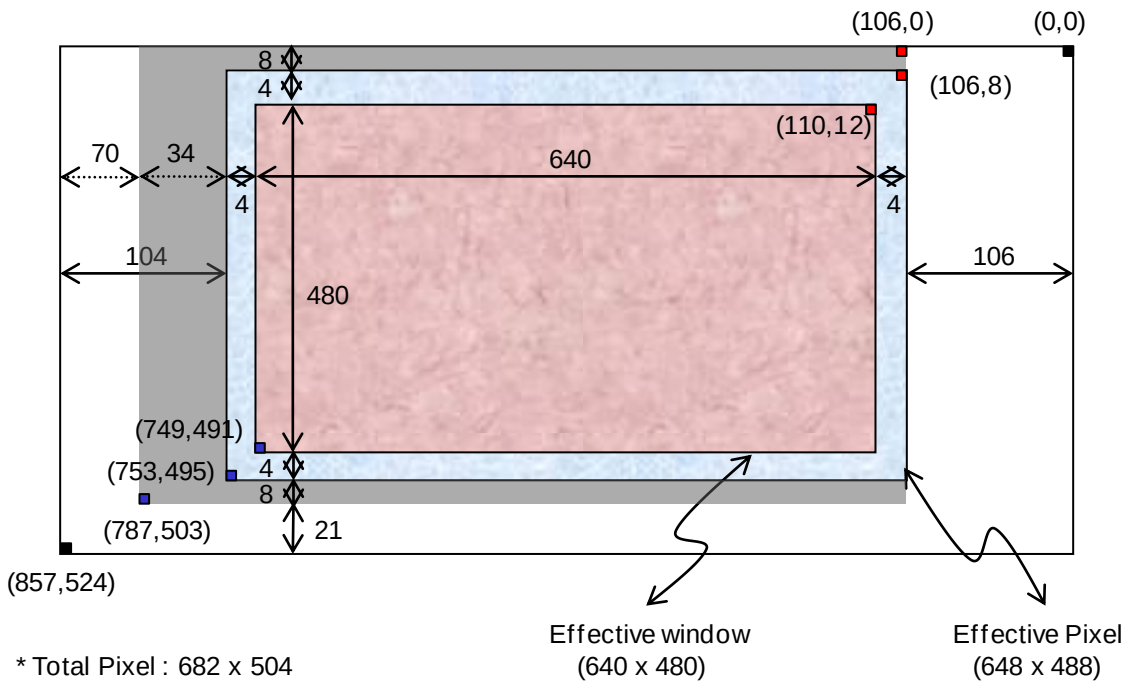
[Fig. 2] Block Diagram

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Frame Structure and Windowing

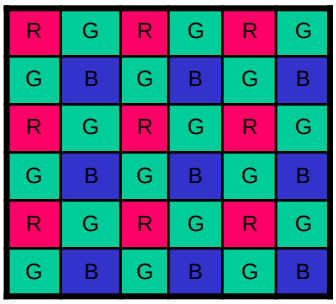
Origin *(0, 0)* of the frame is at the upper right corner. Size of the frame is determined by two registers : *framewidth(Reg.A-06h, A-07h)* and *frameheight(Reg.A-08h, A-09h).* One frame consists of *framewidth + 1* columns and *frameheight + 1* rows. *framewidth* and *frameheight* can be programmed to be larger than total array size. Default window array of 640 x 480 pixels is positioned at *(110, 12).* It is possible to define a specific region of the frame as a window. Pixel scanning begins from *(0, 0)* and proceeds row by row downward, and for each line scan direction is from right to the left. Hsync signal indicates if the output is from a pixel that belongs to the window or not. There are two counters to indicate the present coordinate of frame scanning : Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *frameheight* , and 0 to *framewidth* respectively. The counter values increase at the pace of pixel clock (PCLK), which does not change as the frame size is altered. The pixel data rate is fixed and is independent of frame size. [Fig. 3] shows *window x, y start/stop(Reg.A-0Ch ~ A-13h)* registers value for default window and maximum window.

PC3030K Frame Structure



[Fig. 3] Default Data Structure of Frame and Window. (Top View)

▶ Data Formats



[Fig. 4] Bayer Color Filter Pattern

Pixel array is covered by Bayer color filters as can be seen in the [Fig. 4]. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PC3030K provides this Bayer pattern RGB data through an 10bit channel. It takes one PCLK to pass one pixel RGB data to output bus. But since it is necessary to know all 3 color components R, G, B to produce a color for a pixel, the other two components must be inferred from other pixel data. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as an average of its four nearest R neighbors. This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PC3030K adopts a low pass filter to prevent the interference patterns (called Moiré pattern) from degrading the image quality too much. After color interpolation, every pixel has all three color components. These three color components R, G, B can be routed to 10 bits output pins in such a way RGB565. It takes two PCLK's to pass one pixel RGB data to output bus.

It is possible to extract monochrome luminance data from RGB color components and the conversion equation is : Y = 0.299R + 0.587G + 0.114B where R,G and B are gamma corrected color components. And the color information is separated from luminance information according to following equations.

$$U = 0.492 (B – Y), \quad V = 0.877 (R – Y)$$

Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality.

[Fig. 5] shows 4:2:2 YUV data sequence. PC3030K supports 4:2:2 YUV data format where U and V components are horizontally sub-sampled such that U and V for every other pixel are omitted. PC3030K also supports ITU-R BT.601 YC_BC_R format which is a scaled, offset version of YUV. Y is the same in both formats but the C_BC_R is formed as follows.

U1	Y1	V1	Y2	U3	Y3	V3	Y4	…

[Fig. 5] 4:2:2 YUV Data Sequence.

$$C_B = 0.564 (B – Y) + 128$$
$$C_R = 0.713 (R – Y) + 128$$

▶ Data and Synchronization Timing

1) VGA

[Fig. 6] shows the default data sequence of PC3030K. In [Fig. 6] VSYNC/HSYNC/PCLK polarity can have any combinations possible. Data can be latched at the rising or falling edge of PCLK. HSYNC can be set to be active high or active low. The sequence default YUV data is [U,Y, V, Y, …] for common even / odd rows.

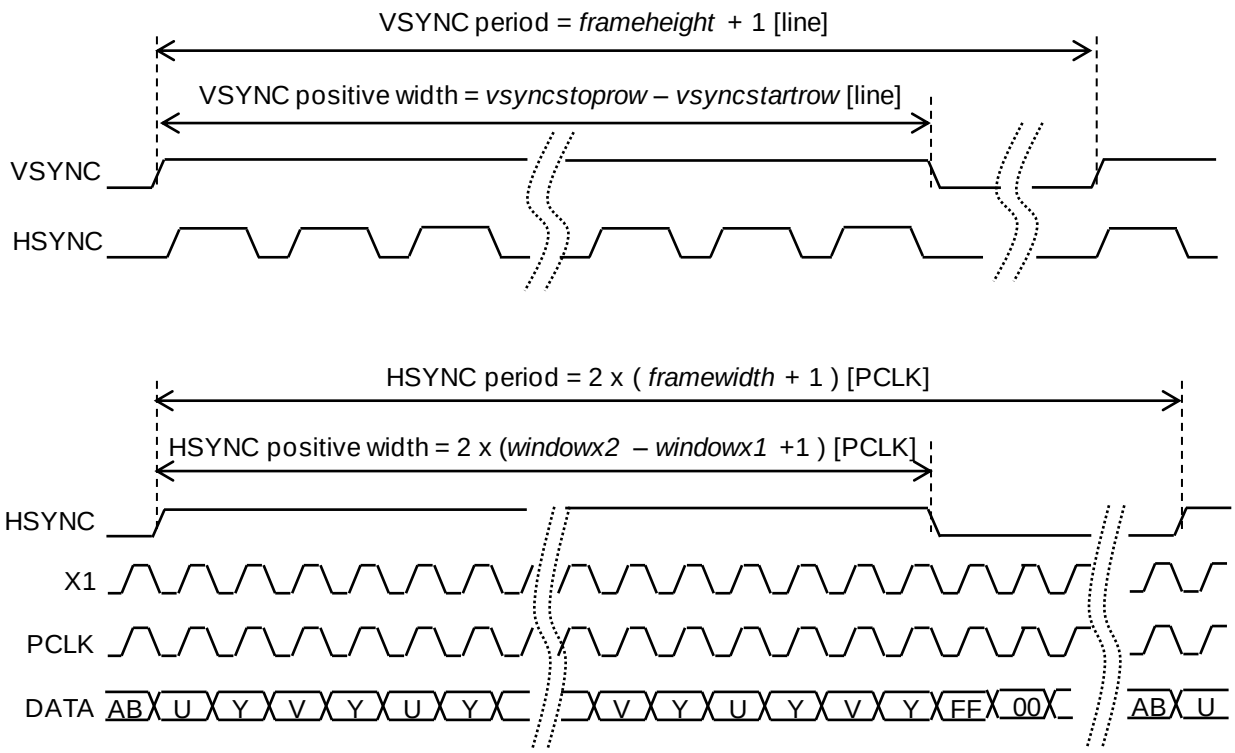
The positive width of VSYNC can be programmed by *vsyncstartrow* and *vsyncstoprow* (register value) and given by

VSYNC positive width = *vsyncstartrow* – *vsyncstoprow* [line]

The positive width of HSYNC can be programmed by *windowx1 / x2(Register Value)* and given by

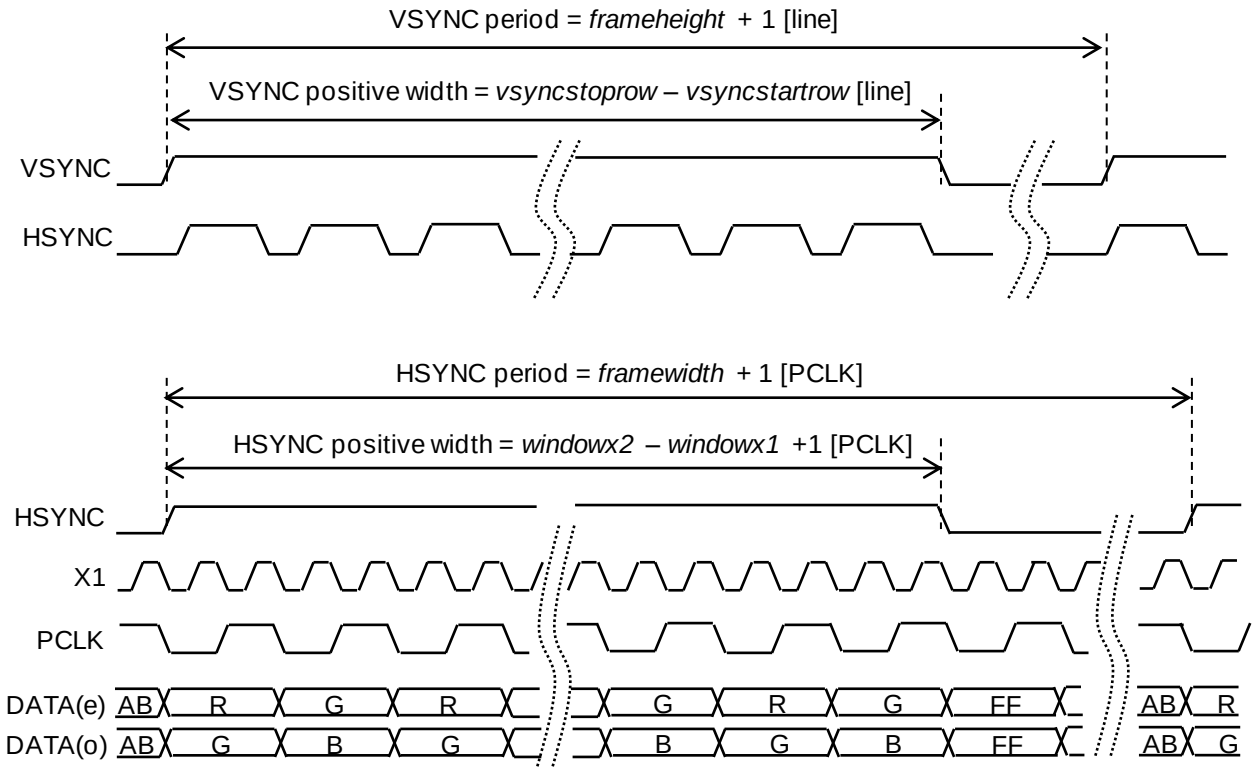
HSYNC positive width = 2 x (*windowx2 - windowx1 + 1)* [PCLK]

Data sequence of YUV format can change to [U, Y, V, Y], [V, Y, U, Y], [Y, U, Y, V] and [Y, V, Y, U] by *format* (register value). Data value can be selected in Invalid or blanking region.



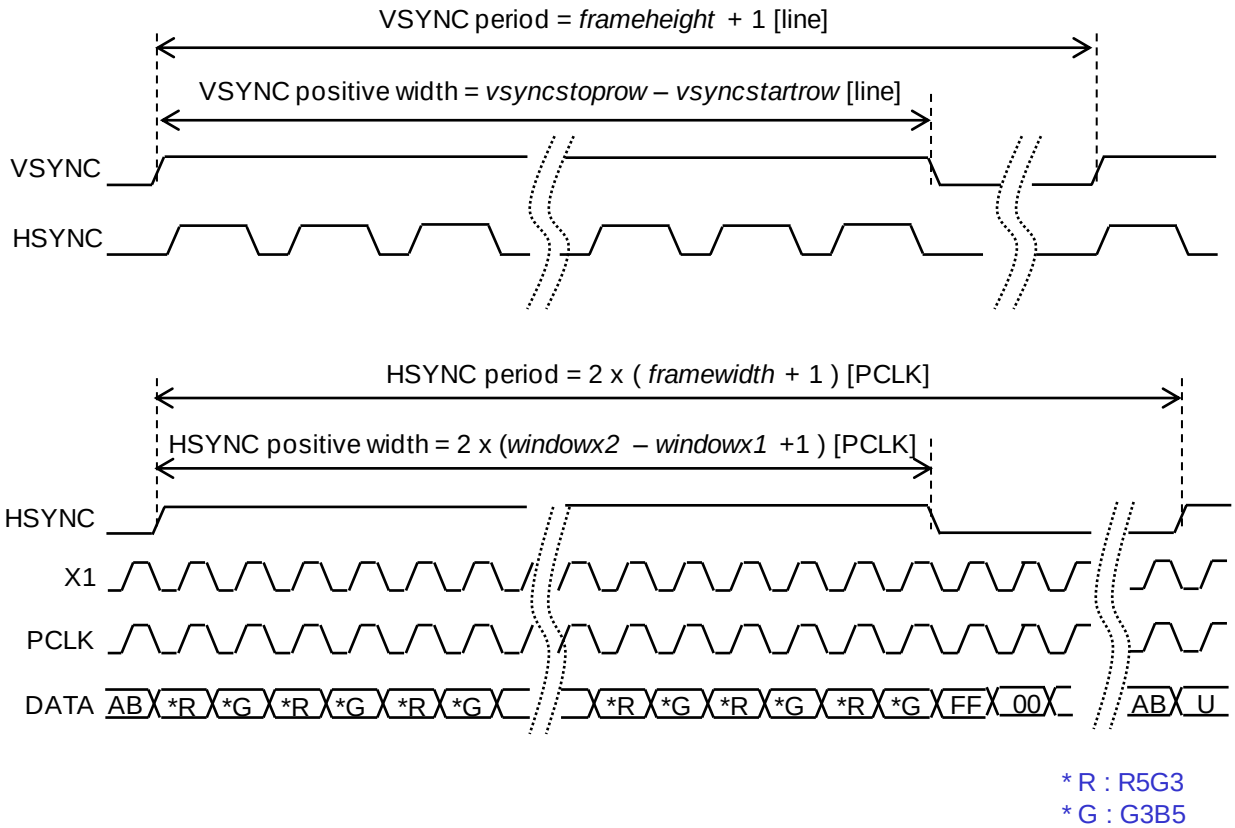
[Fig. 6] Timing Diagram for VSYNC, HSYNC, X1, PCLK and Data (YUV mode : default)

[Fig. 7] shows the bayer data sequence of PC3030K. The default sequence Bayer data is [RGRG…] for even rows and [GBGB…] for odd rows.



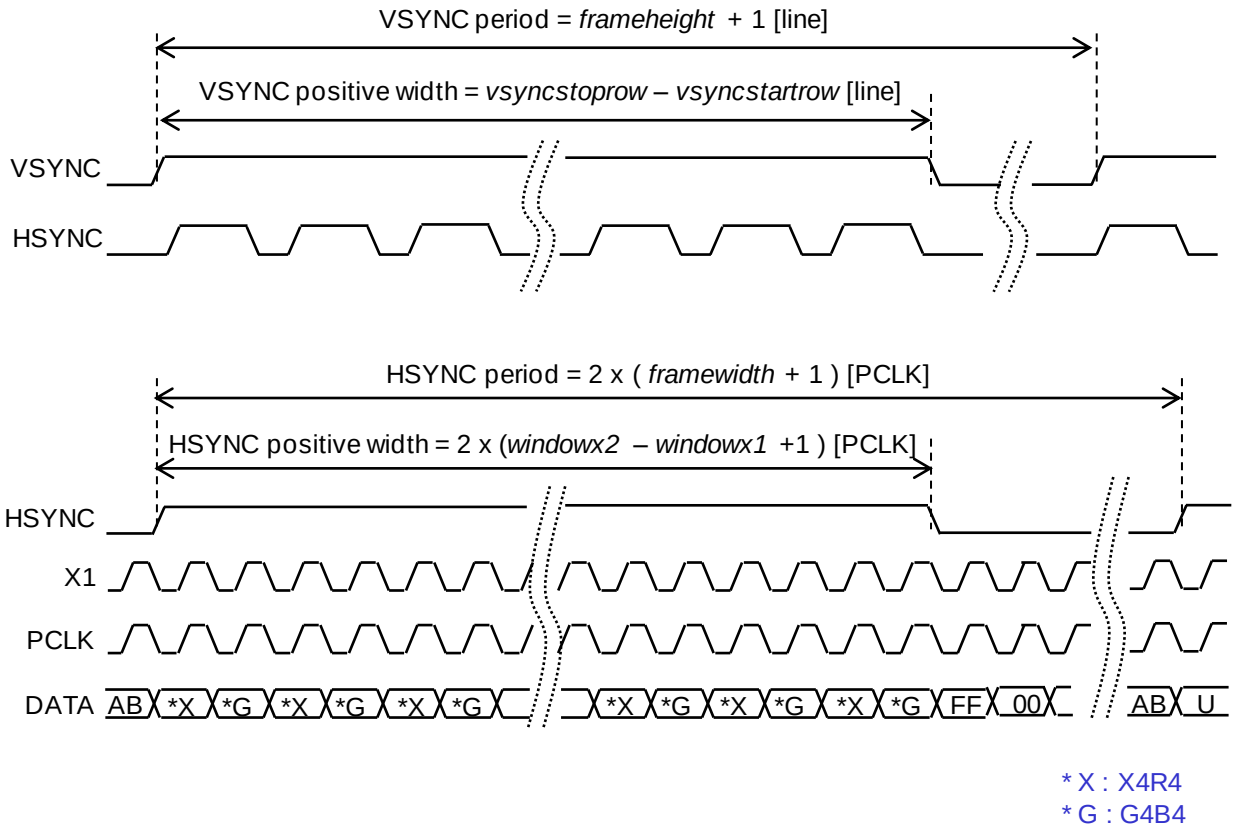
[Fig. 7] Timing Diagram for VSYNC, HSYNC, X1, PCLK and Data (Bayer mode)

[Fig. 8] shows the RGB565 data sequence of PC3030K. The RGB565 data sequence can change to [R5G3, G3R5], [G3R5, R5G3], [B5G3, G3R5] and [G3R5, B5G3] by *format* (register value).



[Fig. 8] Timing Diagram for VSYNC, HSYNC, X1, PCLK and Data (RGB565 mode)

[Fig. 9] shows the RGB444 data sequence of PC3030K. The RGB444 data sequence can change to [x4R4, G4B4] and [G4B4, X4R4] by *format* (register value).

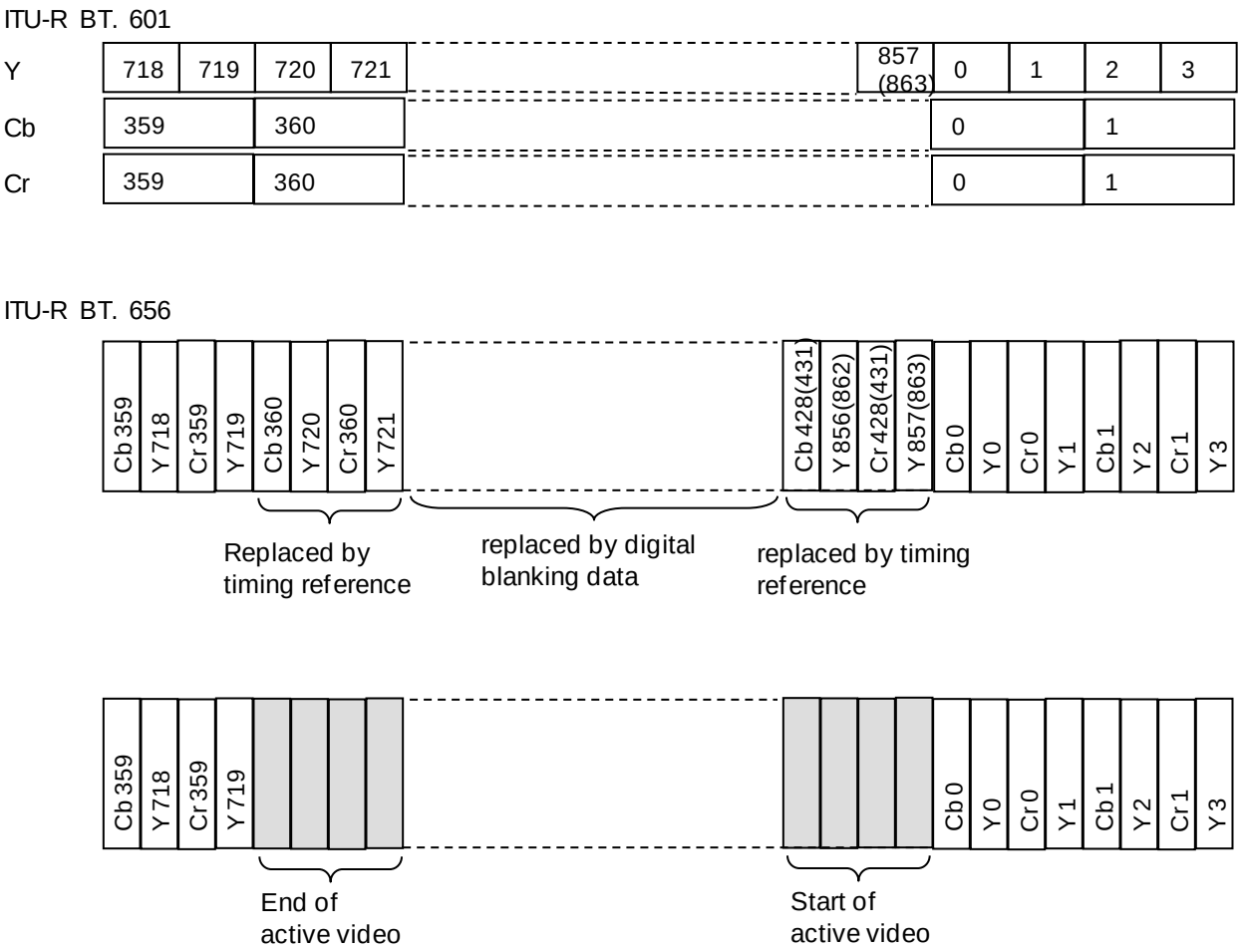


[Fig. 9] Timing Diagram for VSYNC, HSYNC, X1, PCLK and Data (RGB444 mode)

2) ITU-R BT656 (CCIR656)

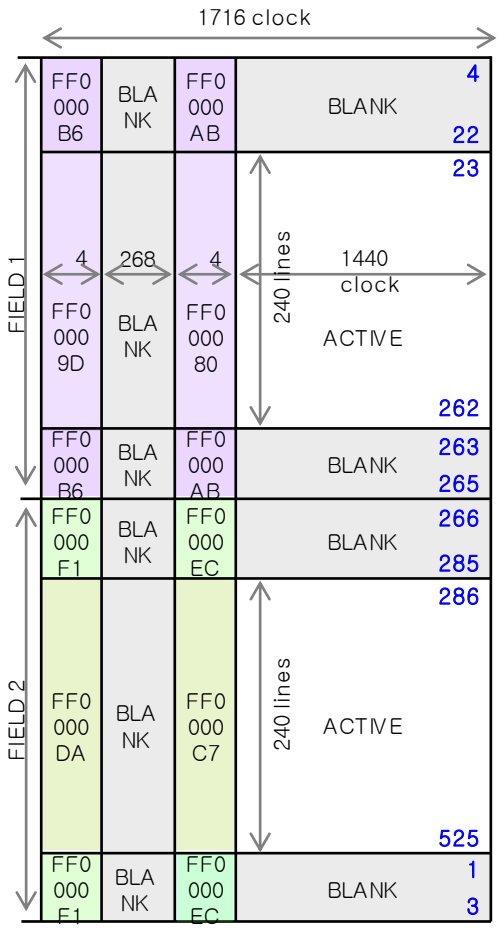
[Fig. 10] shows ITU-R BT601 and ITU-R BT656 timing diagram. Sampling clocks of ITU-R BT601 and ITU-R BT656 are 13.5MHz and 27MHz respectively. ITU-R BT656 format is generated from ITU-R BT601 format data by serialization and timing reference. Timing reference indicates Start or End of video. It includes field, vsync and hsync information.

PC3030K provides two kinds of active video sizes with BT656 format such as 720x480i and 720x576i ('i' stands for interlaced scan). The horizontal size is stretched from 640 to 720 pixels. When the horizontal line is 640,720 and 768 of the input data, register of the hscale_sel be specified depending on the scale mode. 720x480i size BT656 supports for 525-line video, and 720x576i size BT656 for 625-line video. Horizontal timing of 720x480i and 720x576i size BT656 is shown in [Fig. 10] and vertical Timing diagram is shown in [Fig. 11]

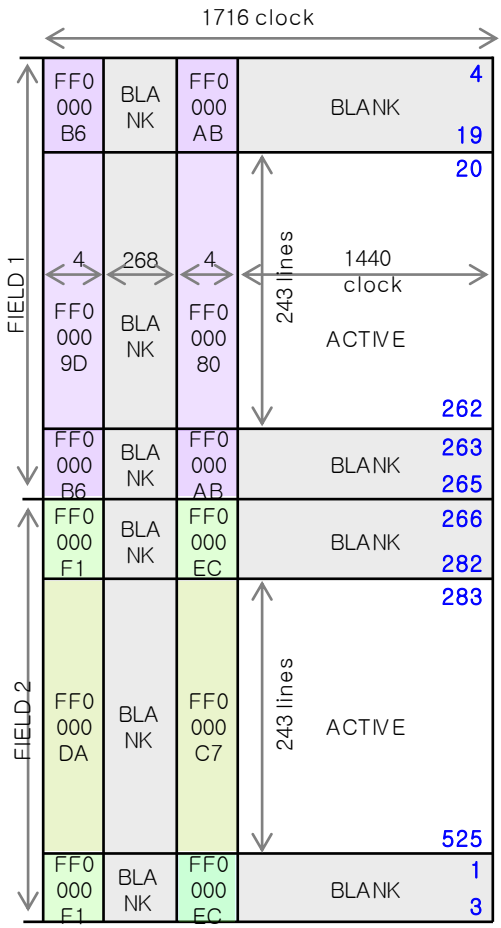


[Fig.10] Timing Diagram of ITU-R BT601 and ITU-R BT656

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array



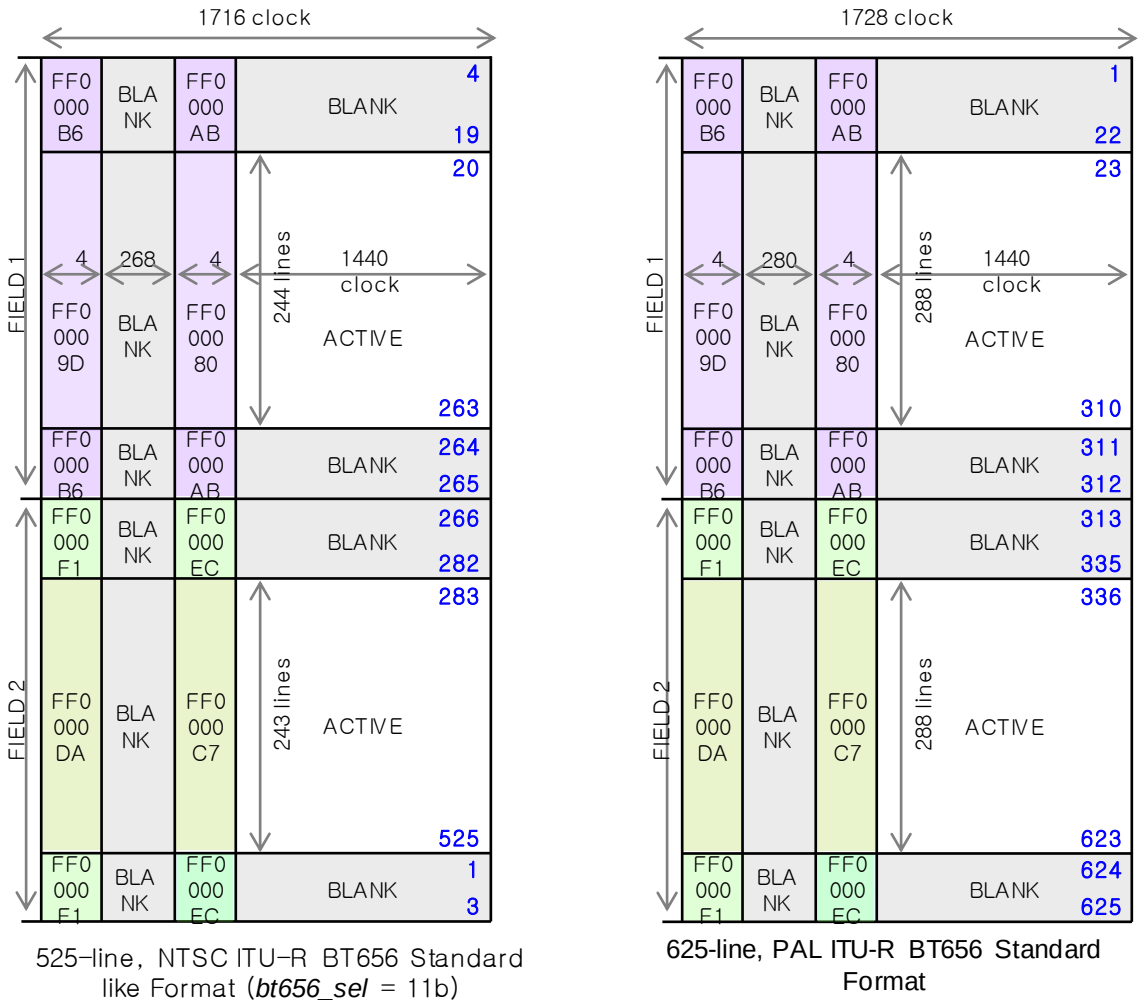
525-line, NTSC ITU-R BT656 Standard like Format (*bt656_sel* = 00b)



525-line, NTSC ITU-R BT656 Standard Format (*bt656_sel* = 10b)

[Fig. 11] Vertical Timing Diagram of ITU-R BT656 (continue)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array



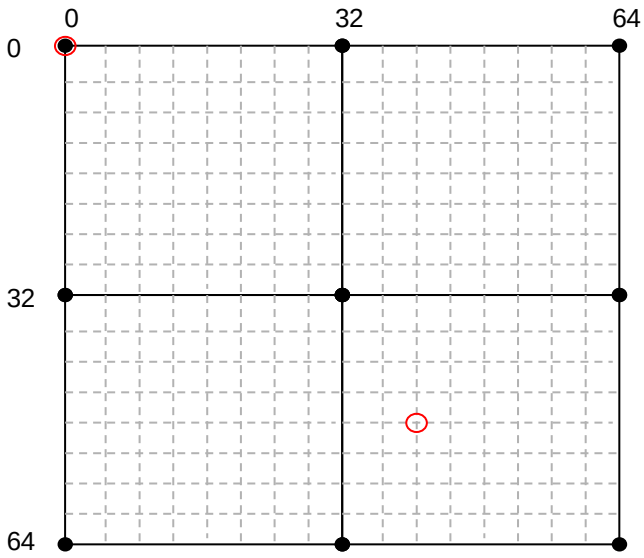
525-line, NTSC ITU-R BT656 Standard like Format (*bt656_sel* = 11b)

625-line, PAL ITU-R BT656 Standard Format

[Fig. 11] Vertical Timing Diagram of ITU-R BT656

- The numbers on the image indicate Line number.
- For 525-line format, active lines are 240, 243 or 244 per a field. For 625-line format, active lines are 288 per a field.
- Vertical Timing is slightly different to Typical BT.656 for 525-line format. In active data regions above [Fig. 11] they have only active pixel data not any fixed data (eg. black data).

▶ Scaling



[Fig. 12] Free Scaling

● Full image pixel locations

X points = 32 * M

Y points = 32 * N

○ Scaled image sampling points

X Sampling points = reg_scale_x * P

Y Sampling points = reg_scale_y * Q

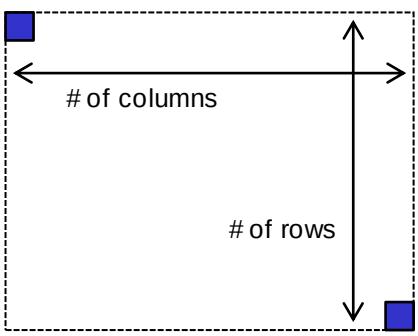
← Example

reg_scale_x = 40

reg_scale_y = 48

(reg_window_x1, reg_window_y1)

minimum = (1, 1)



[Fig. 13] Output Image Size

(reg_window_x2, reg_window_y2)

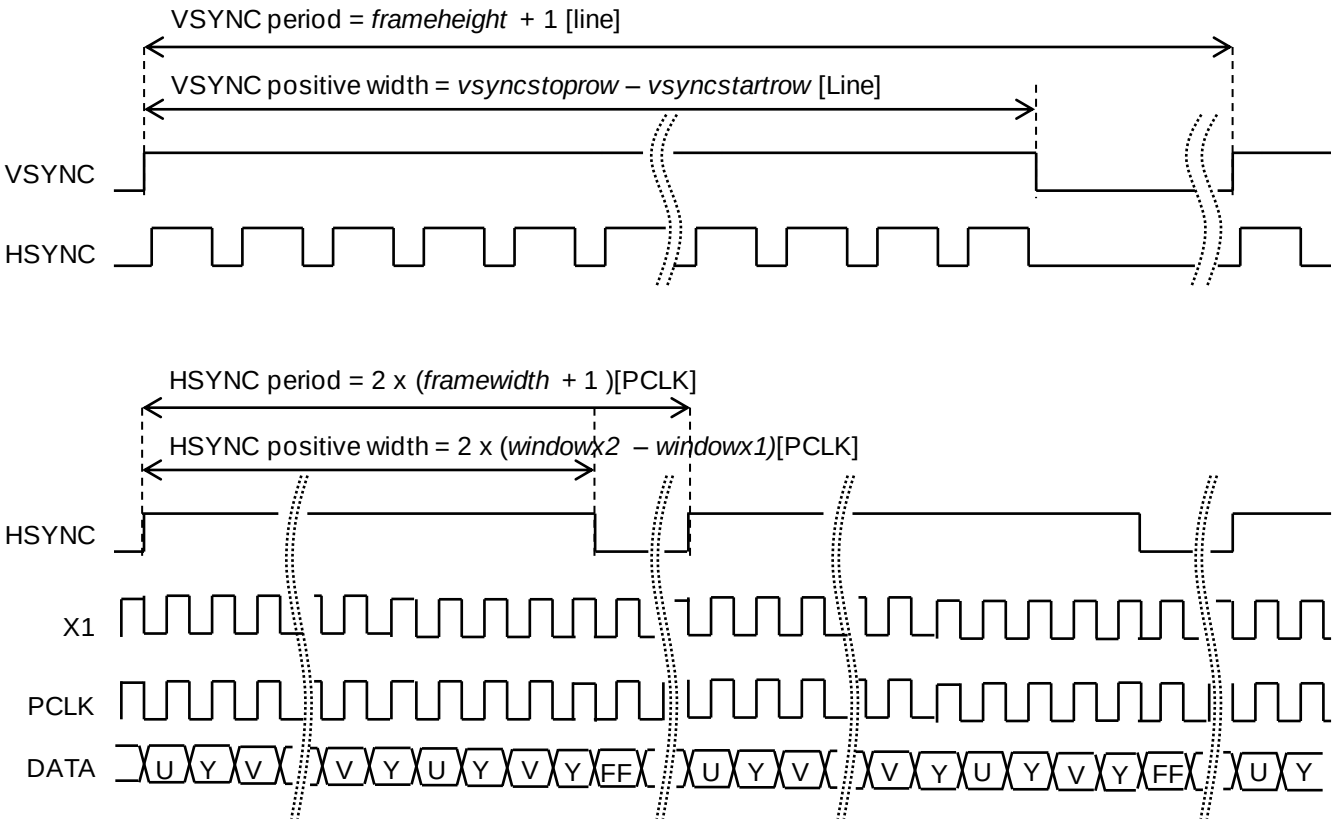
maximum = (640, 480)

Where,

Number of columns = reg_window_x2 - reg_window_x1 + 1

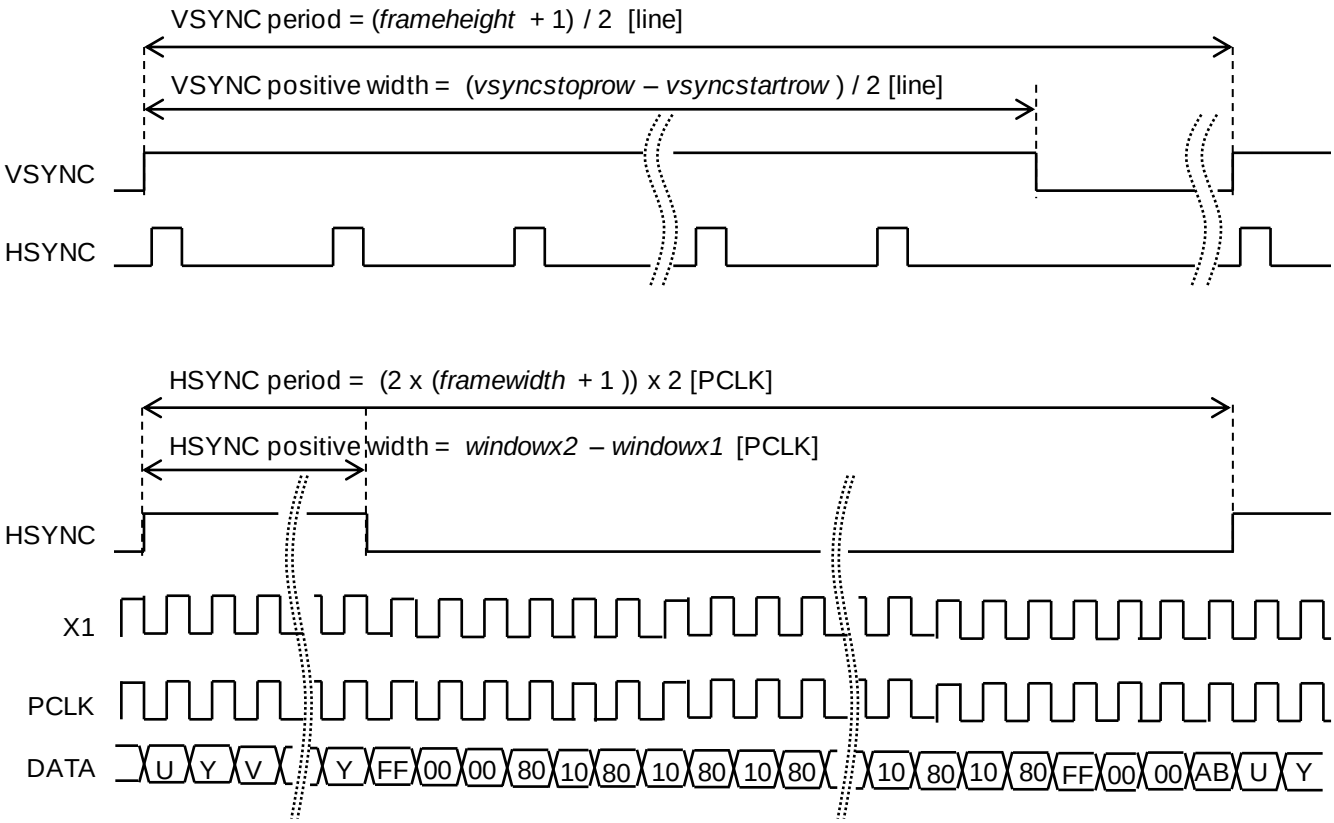
Number of rows = reg_window_y2 - reg_window_y2 + 1

(1) X Full Sampling Mode / Y Full Sampling Mode



[Fig. 14] Timing Diagram for Full Mode

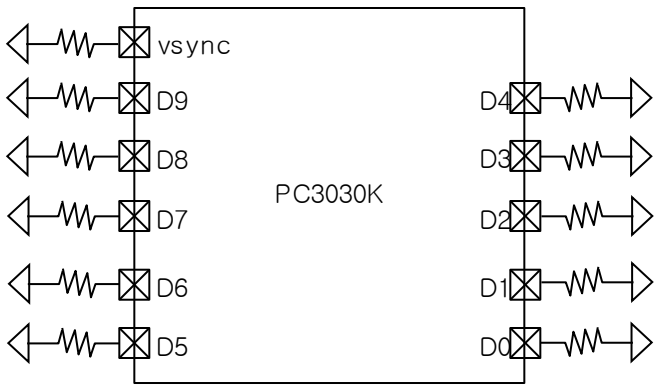
(2) X 1/2 Scale Mode / Y 1/2 Scale Mode



[Fig. 15] Timing Diagram for XY-Scaling Mode

▶ Wire-strapping

Wire-strapping is a function of chip mode selection. Chip mode is automatically selected according to D9~D0 pads wired with pull-up or pull-down. [Fig.16] shows one example of Wire-strapping configuration and [Table 3] shows chip mode selection by wire-strapping.



[Fig.16] Example of Wire-strapping

		vsync	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TV_MODE	(M)NTSC	-	-	-	-	-	-	L	L	L	-	-
	NTSC-J	-	-	-	-	-	-	L	L	H	-	-
	(M)PAL	-	-	-	-	-	-	L	H	L	-	-
	(Nc)PAL	-	-	-	-	-	-	L	H	H	-	-
	(N)PAL	-	-	-	-	-	-	H	L	L	-	-
	(B,D,G,H,I)PAL	-	-	-	-	-	-	H	L	H	-	-
FLICKER	No Flicker cancel	-	-	-	-	L	L	-	-	-	-	-
	Manual-A	-	-	-	-	L	H	-	-	-	-	-
	Manual-B	-	-	-	-	H	L	-	-	-	-	-
	Auto Flicker cancel	-	-	-	-	H	H	-	-	-	-	-
MIRROR	NO MIRROR	-									H	L
	MIRROR-V	-	-	-	-	-	-	-	-	-	L	L
	MIRROR-H	-	-	-	-	-	-	-	-	-	H	H
	MIRROR-VH	-	-	-	-	-	-	-	-	-	L	H
BLC	ON	-	-	-	L	-	-	-	-	-	-	-
	OFF	-	-	-	H	-	-	-	-	-	-	-
Indoor/ Outdoor	Indoor mode	-	-	H	-	-	-	-	-	-	-	-
	Outdoor mode	-	-	L	-	-	-	-	-	-	-	-

[Table 3] Wire-strapping (continue)

		vsync	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OSD	Enable	-	H	-	-	-	-	-	-	-	-	-
	Disable	-	L	-	-	-	-	-	-	-	-	-
MASTER MODE	ON	H	-	-	-	-	-	-	-	-	-	-
	OFF	L	-	-	-	-	-	-	-	-	-	-

[Table 3] Wire-strapping

[Table 4] shows TV_mode wire-strapping registers. These registers are changed by D4~D2.

	"000b"	"001b"	"010b"	"011b"	"100b"	"101b"
Register name	(M)NTSC	NTSC-J	(M)PAL	(Nc)PAL	(N)PAL	(OTHER)PALs
chip_mode	00	00	00	01	01	01
framewidth	0359	0359	0359	040D	040D	040D
frameheight	020C	020C	020C	0207	0207	0207
windowy2	00F0	00F0	00F0	0120	0120	0120
scale_y	40	40	40	35	35	35
fd_a_step	03E8	03E8	03E8	04BD	04BD	04BD
fd_b_step	0340	0340	0340	03F0	03F0	03F0
fd_period_a	01068B	01068B	01068B	00D8F8	00D8F8	00D8F8
fd_period_b	013B0D	013B0D	013B0D	01045D	01045D	01045D
fd_period_c	0627	0627	0627	0515	0515	0515
fd_fheight_a	020C	020C	020C	0207	0207	0207
fd_fheight_b	020C	020C	020C	0207	0207	0207
enc_scfreq	00	00	03	02	01	01
enc_blank	F0	F0	F0	FC	F0	FC
enc_pedestal	2A	00	2A	00	2A	00
enc_burst	70	70	75	75	75	75
enc_Ygain	82	8D	82	89	82	89
enc_Ugain	6F	78	6F	75	6F	75
enc_Vgain	9C	A9	9C	A6	9C	A6
enc_Crange_L	48	62	48	5B	48	5B
enc_chroma_max_L	CD	DF	CD	D7	CD	D7
enc_chroma_min_L	6D	35	6D	45	6D	45
expfrmH	0207	0207	0207	0202	0202	0202
midfrmheight	0207	0207	0207	0202	0202	0202
maxfrmheight	0207	0207	0207	0202	0202	0202
ae_win_fy2	00F0	00F0	00F0	0120	0120	0120
ae_win_cy1	0051	0051	0051	0061	0061	0061
ae_win_cy2	00A0	00A0	00A0	00C0	00C0	00C0
ae_yaxis	0079	0079	0079	0091	0091	0091
awb_win_fy2	00F0	00F0	00F0	0120	0120	0120
awb_win_cy1	0051	0051	0051	0061	0061	0061
awb_win_cy2	00A0	00A0	00A0	00C0	00C0	00C0

[Table 4] TV Mode Registers

[Table 5~8] show registers and setting values related with Flicker mode, Mirror mode, BLC mode and Indoor/Outdoor mode.

	"00b"	"01b"	"10b"	"11b"
Register name	Normal(off)	manual A	manual B	auto_fd
flicker_control_1	00	08	04	80

[Table 5] Flicker Mode Register

	"00b"	"01b"	"10b"	"11b"
Register name	V mirror	HV mirror	No mirror	H mirror
mirror	02	03	00	01

[Table 6] Mirror Mode Register

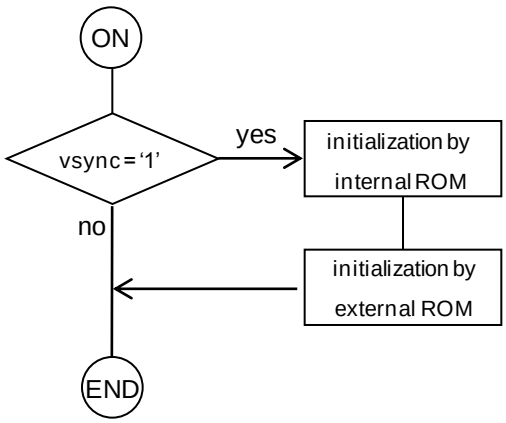
	"0b"	"1b"
Register name	BLC off	BLC on
ae_weight1	08	08
ae_weight2	08	08
ae_weight3	08	08
ae_weight4	08	08
ae_weightc	18	08
max_yt1	A0	A0
max_yt2	80	80
min_yt1	80	80
min_yt2	50	50

[Table 7] BLC Mode Register

	"0b"	"1b"
Register name	Outdoor	Indoor
awb_rgain_min1	40	2A
awb_rgain_min2	40	28
awb_rgain_max1	50	5A
awb_rgain_max2	50	5D
awb_bgain_min1	60	50
awb_bgain_min2	60	4D
awb_bgain_max1	A2	B7
awb_bgain_max2	A2	BA

[Table 8] Indoor/Outdoor Mode Register

[Table 9] show registers and setting values related with master mode.



[Fig. 17] shows initialization process of registers. When vsync is high, register default values are initialized by internal ROM and external ROM.

▶ If you want to see more processes, see [Fig. 20].

[Fig. 17] Initialization Process of Registers

	vsync=0b	vsync=1b
Registers	master mode off	master mode on
analog_control_4	42h	42h
lens_gaing1	00h	00h
lens_gaing2	00h	00h
edge_gain	14h	14h
ec_pgain	80h	80h
ec_mgain	80h	80h
ccr_m11	33h	33h
ccr_m12	8Bh	8Bh
ccr_m13	88h	88h
ccr_m21	86h	86h
ccr_m22	31h	31h
ccr_m23	8Ah	8Ah
ccr_m32	8Fh	8Fh
ccr_m33	32h	32h
y_weight	40h	40h
awb_cwx1_l	D6h	D6h
awb_cwx2_h	01h	01h
awb_cwx2_l	ABh	ABh
awb_control_1	95h	95h
minexp_l	0Ch	0Ch

	vsync =0b	vsync =1b
Registers	master mode off	master mode on
midexp_h	85h	85h
midexp_m	40h	40h
maxexp_t	01h	01h
maxexp_h	85h	85h
maxexp_m	40h	40h
max_yt1	A0h	A0h
min_yt1	80h	80h
awb_p1Ax	29h	29h
awb_p1Ay	39h	39h
awb_p2Ax	36h	36h
awb_p2Ay	19h	19h
awb_osAx	09h	09h
awb_osAy	10h	10h
awb_slopeA	A0h	A0h
awb_p1Bx	36h	36h
awb_p1By	21h	21h
awb_p2Bx	69h	69h
awb_p2By	14h	14h
awb_osBx	0Ch	0Ch
awb_osBy	04h	04h

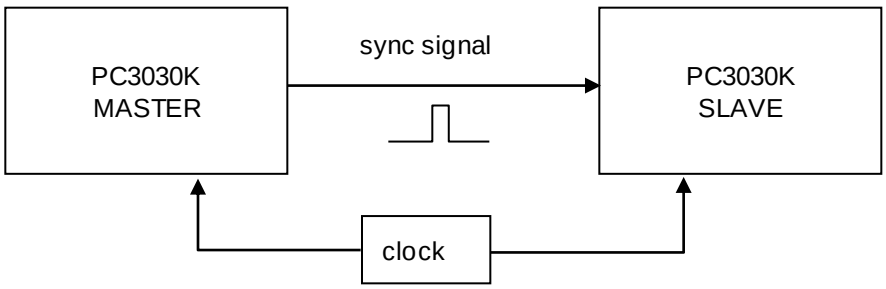
[Table 9] Internal ROM Registers Setting (continue)

	vsync =0b	vsync =1b
Registers	master mode off	master mode on
awb_slopeB	10h	10h
awb_maxc	FAh	FAh
awb_minc	08h	08h
awb_weight_c	05h	05h
awb_weight_p	0Bh	0Bh
rg_ratio_a	7Ah	7Ah
bg_ratio_a	78h	78h
ratio_axis_a	2Ah	2Ah
ratio_axis_b	50h	50h
ratio_axis_c	57h	57h
lens_gainr_a	02h	02h
axis_a	2Ah	2Ah
axis_b	50h	50h
axis_c	57h	57h
user_cs	20h	20h
dark_blf0	5Fh	5Fh
dark_blf1	3Fh	3Fh
dark_blf2	3Fh	3Fh
dark_nf0	40h	40h
dark_nf1	40h	40h
dark_nf2	40h	40h
dark_nf	01h	01h
dark_intp0	00h	00h
dark_intp1	08h	08h
dark_intp2	18h	18h
dark_intp	00h	00h
dark_hr_th0	04h	04h
dark_hr_th1	08h	08h

	vsync = 0b	vsync =1b
Registers	master mode off	master mode on
dark_hr_th2	18h	18h
dark_hr_th	04h	04h
dark_ccr1	04h	04h
dark_ccr2	08h	08h
dark_ec_pth1	04h	04h
dark_ec_pth2	04h	04h
dark_ec_mth1	04h	04h
dark_ec_mth2	04h	04h
dark_ec_pmax0	80h	80h
dark_ec_pmax1	80h	80h
dark_ec_pmax2	80h	80h
dark_ec_pmax	80h	80h
dark_ec_mmax0	80h	80h
dark_ec_mmax1	80h	80h
dark_ec_mmax2	80h	80h
dark_ec_mmax	80h	80h
resol_gain	08h	08h
enc_control	44h	44h

[Table 9] Internal ROM Registers Setting

▶ Genlock(master/slave) Operation



[Fig. 18] System Configuration for Genlock

Registers	Values	Descriptions
pad_control5(3)	'1b'	Enable GENO pad
bayer_control_01(5)	'1b'	External Sync ON
bayer_control_01(4)	'1b'	External Sync Master
rcount_genlock_h/l, ccount_genlock_h/l	same as slave's	Synchronizing time control between master and slave

[Table 10] Registers Setting for Genlock Master

Registers	Values	Descriptions
pad_control5(0)	'1b'	Enable GENI pad
bayer_control_01(5)	'1b'	External Sync ON
bayer_control_01(4)	'0b'	External Sync Slave
rcount_genlock_h/l, ccount_genlock_h/l	same as master's	Synchronizing time control between master and slave

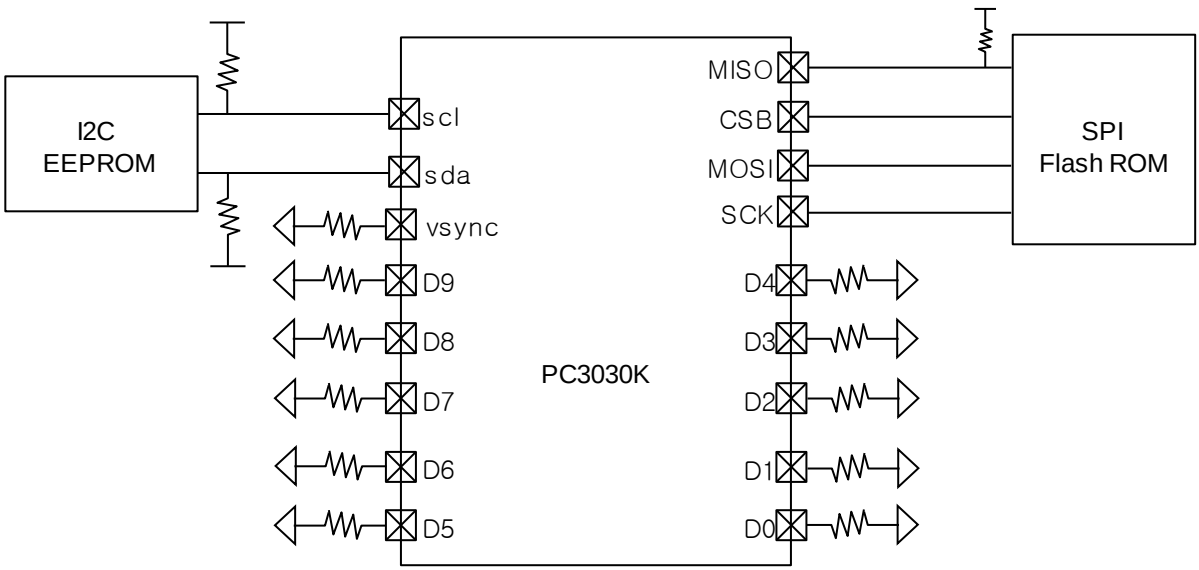
[Table 11] Registers Setting for Genlock Slave

Genlock is a function to synchronize digital output data of two or more PC3030Ks. One of the PC3030K must be a master and others are slaves. The master generates genlock signal by the *rcount_genlock_h/l* and *ccount_genlock_h/l*. Then slaves receive the genlock signal from the master and set their counters with the *rcount_genlock_h/l* and *ccount_genlock_h/l*.

Caution : When user want to use one SCL/SDA line with several PC3030Ks, user must connect CADDR1 and CADDR0 pads to pull-up or pull-down.

▶ Registers Initializing

PC3030K supports user tuning registers can be set by I2C EEPROM or SPI Flash ROM initially. [Fig. 19] shows how to connect PC3030K with external ROM(I2C EEPROM/SPI Flash ROM). After reset, PC3030K reads initialization table stored in external ROM. [Fig. 20] shows Initialization routine.



[Fig. 19] Example of Connection with External ROM

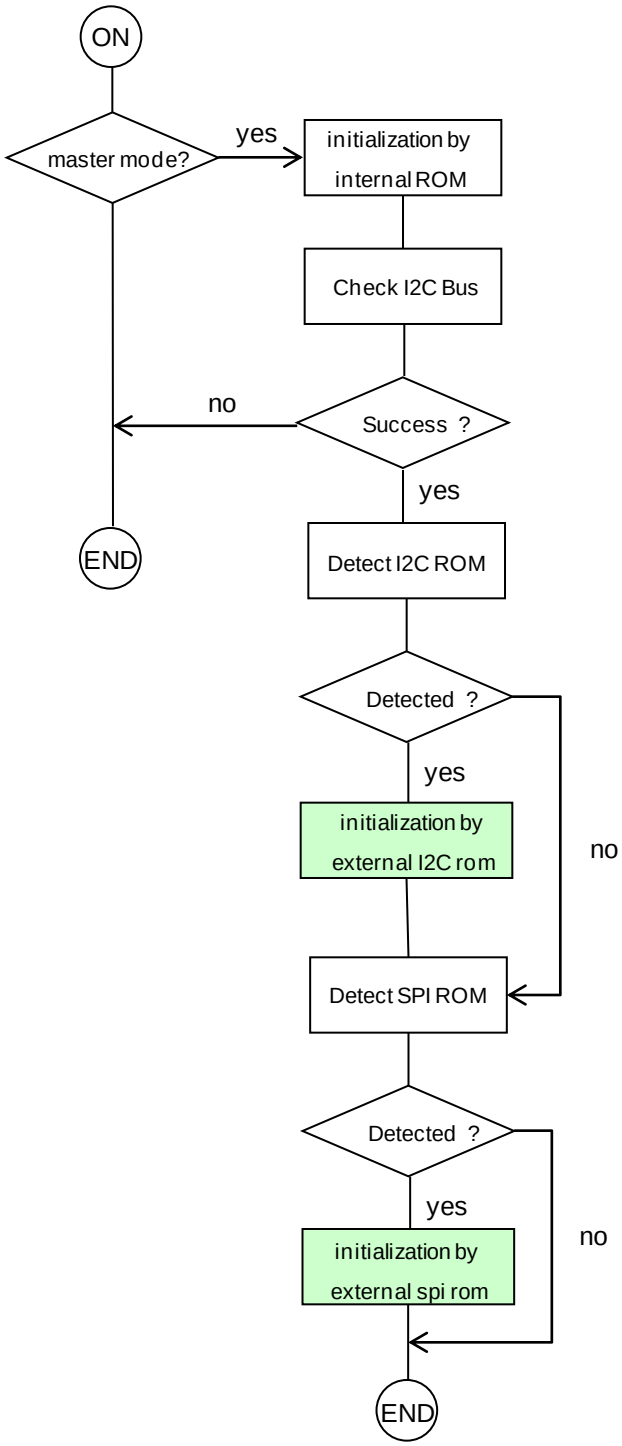
Initialization process is as below.

Case1 : Connect with I2C EEPROM & disconnect with SPI Flash ROM :
PC3030K is initialized by I2C EEPROM. SPI Flash ROM process is skipped.

Case2 : Connect with SPI Flash ROM & disconnect with I2C EEPROM :
PC3030K is initialized by SPI Flash ROM. I2C EEPROM process is skipped.

Case3 : Connect with I2C EEPROM & connect with SPI ROM :
PC3030K registers are overwritten by SPI Flash ROM.

* Caution : It covers up to 2K bytes I2C EEPROM. If the I2C EEPROM size is more than 2K bytes then register setting does not operate.



[Fig. 20] Initialization Routine

▶ Access Time of External I2C Master

Because I2C master was designed as a single master and shares SDA/SCL with I2C slave, external I2C master must access to PC3030K after initialization routine as [Fig. 20]. Initialization time depends on the number of registers to be written by external I2C rom. If the number of setting register is 1024d (max.), it will take initialization time about 140ms to be finished after reset. After that, an external I2C master should access to PC3030K.

Access time as below.

Case1 : master enable and with external I2C rom : variable (depend on register numbers, max. 140ms)

Case2 : master enable and without external I2C rom : after about 6ms(I2C rom detection time)

Case3 : master disable: always possible

▶ ROM Data Structure for Initialization (I2C/SPI ROM)

Address	Contents
0	ABh (Constant) (1)
1	CDh (Constant) (2)
2	reserved (3)
3	reserved (4)
4	reserved (5)
5	reserved (6)
6~7	Common Segment Start
8~9	Common Segment Stop
10~11	TV_mode Segment Start
12~13	TV_mode Segment Stop
14~15	Mirror Segment Start
16~17	Mirror Segment Stop
18~19	Flicker Segment Start
20~21	Flicker Segment Stop
22~23	Indoor Segment Start
24~25	Indoor Segment Stop
26~27	BLC Segment Start
28~29	BLC Segment Stop

Address	Contents
…	…
Common Start	Common Segment
Common Stop	
TVmode Start	NTSC
TVmode Stop	PAL
Mirror Start	Mirror=00
	Mirror=01
	Mirror=10
Mirror Stop	Mirror=11
Flicker Start	Flicker=00
	Flicker=01
	Flicker=10
Flicker Stop	Flicker=11
Indoor Start	Indoor
Indoor Stop	Outdoor
BLC Start	BLC on
BLC Stop	BLC off

[Fig. 21] ROM Data Structure

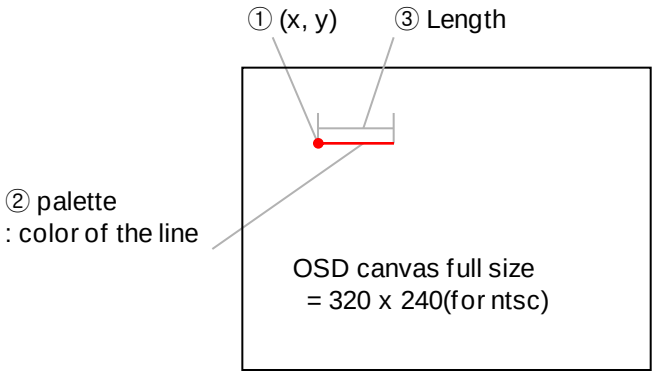
Addresses from 0 to 29d are reserved for Segment Descriptor block. I2C EEPROM and SPI Flash ROM data structure for initialization are same.

(1) ~ (2) : ABCDh in address 0-1 are required to detect external ROM.
(3) ~ (5) : These data are not used, but it should be filled with some data. (caution)

If some Segment Start address is greater than Segment Stop address, initialization by the segment will be skipped. (User should be set start address < stop address)

▶ OSD Data Structure

OSD data consists of commands on positions and lines.



[Fig.22] OSD Data Structure

One line needs 3 components:
position(x, y), palette, length.

1. Position : (x,y) on OSD canvas
➔(2x,2y) on displayed image

2. Palette: represents Y/Cb/Cr information for line.

3. Length: 1 length on OSD canvas
➔ 2 pixels on displayed image

Commands of OSD

1. set_abs_y() : "1 0 0 0 y8 y7 y6 y5 y4 y3 y2 y1 y0 0 0 0" : y = y<8:0>
2. set_rel_y() : "1 1 0 0 dy3 dy2 dy1 dy0" : y = y + dy<3:0> + 1
3. set_abs_x() : "1 1 1 0 x8 x7 x6 x5 x4 x3 x2 x1 x0 0 0 0" : x = x<8:0>
4. drw_sline() : "0 p2 p1 p0 l3 l2 l1 l0 : palette = "0 p2 p1 p0", length = l<3:0> + 1
5. drw_lline() : "1 1 1 1 p2 p1 p0 l8 l7 l6 l5 l4 l3 l2 l1 l0 : palette = "0 p2 p1 p0", length = l<8:0> + 1

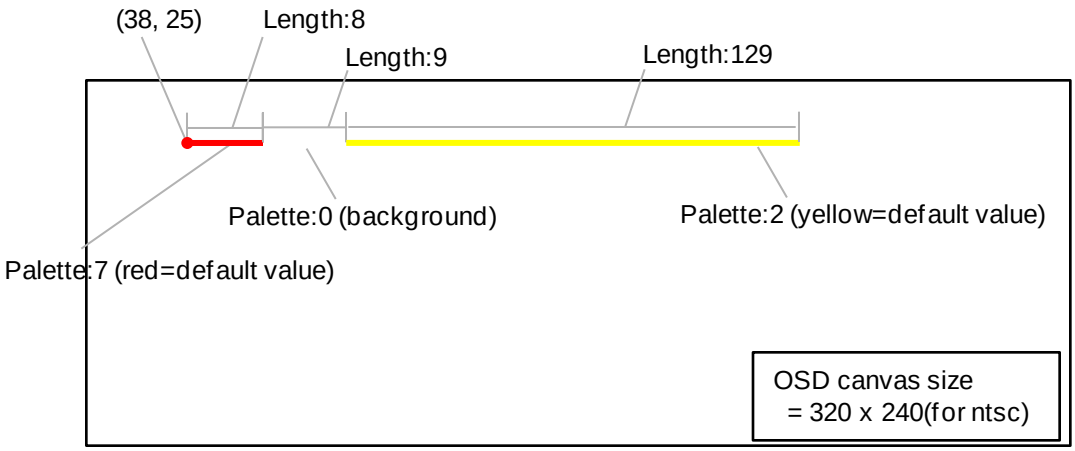
OSD data should be stored in SPI Flash ROM. If user want to change displayed OSD images, user should change *spi_saddr/spi_paddr/spi_addr_update.* For more information, please see the register part.

* Caution : 1. OSD length should be greater than 1.
2. X position should be greater than 0.

[Fig, 23] shows the example of drawing OSD line.

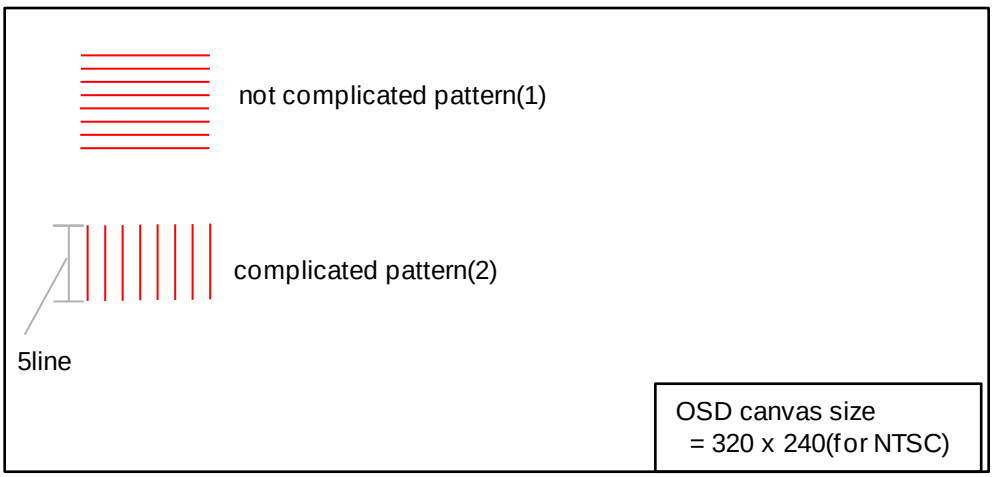
```
SPI ROM OSD data Example

0000h  :  10000000  →  y = 25d
0001h  :  11001000
0002h  :  11100001  →  x = 38d
0003h  :  00110000
0004h  :  01100111  →  draw a line with palette=110, length=8d
0005h  :  00001000  →  skip length9 (palette=000, length=9d)
                       palette 0 represents background of image(sensor data).
0006h  :  11110100  →  draw a line with palette=010, length=129d
0007h  :  10000000
```



[Fig.23] Example of Drawing OSD Line

There are some criteria related displaying OSD data by using SPI interface, because of its speed limitation. The criteria is shown at the case of (2) on [Fig, 24]. The amount of OSD data of (2) is around 20 times larger than case (1). For example, If SPI speed is 13.5Mhz*(spi_baud_rate* = 01h) , the number of limitation while displaying vertical lines such as (2) is about 35.

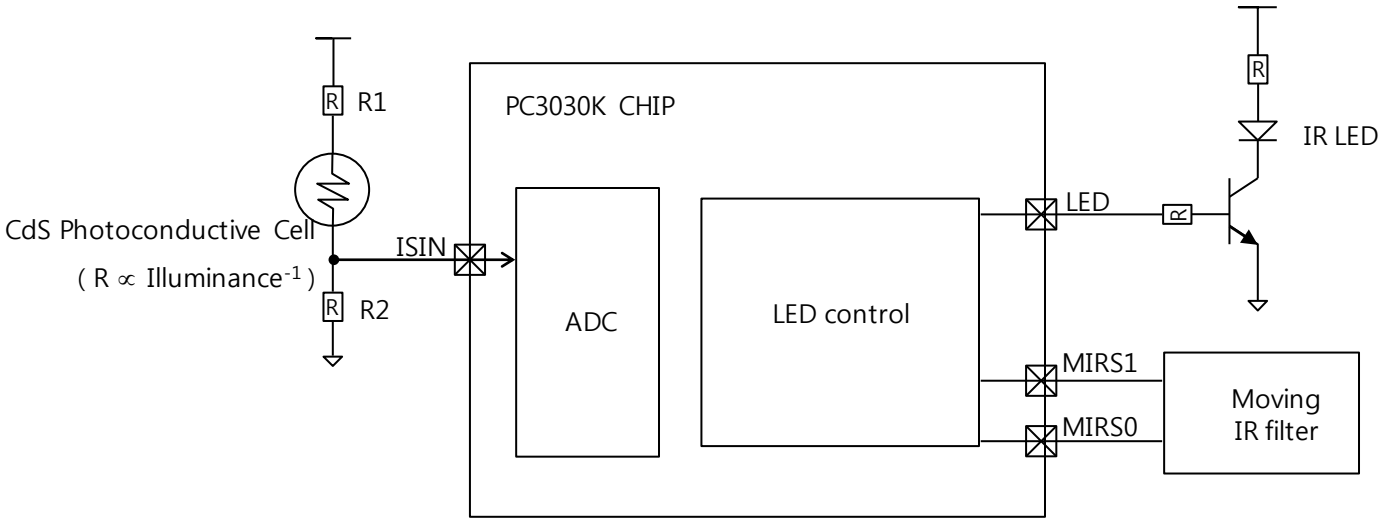


[Fig. 24] Example of Complicated OSD Pattern

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ IR LED & Moving IR filter

The human eyes can only see visible light between 380~770[nm] wavelength. The image sensors can detect wider wavelength than people. Therefore, the sensors can detect the infra-red light but people can not. As a result, when the sensors detect infra-red light, different colors from the real images come out. To prevent this phenomena, camera use the IR-cut filter.



[Fig. 25] IR LED & Moving IR Filter Structure

IR_LED can be controlled by PC3030K which uses analog data from CdS as shown in [Fig. 25]. PC3030K uses IR-cut filter in normal state to prevent above phenomena, but in the dark state, because IR-LED is ON to increase brightness, IR-cut filter should not be used. IR-LED and IR filter can be controlled automatically by PC3030K without changing registers. This means that additional MICOM (MCU) does not need for the IR-LED and IR filter control. As a result, LED and IR filter can be controlled in exact time.

▶ 2-wire Serial Interface Description

The registers of PC3030K are written and read through the 2-wire Serial Interface. The PC3030K has 2-wire Serial Interface slave. The PC3030K is controlled by the Register Access Clock (SCL), which is driven by the 2-wire Serial Interface master. Data is transferred into and out of the PC3030K through the Register Access Data (SDA) line. The SCL and SDA lines are pulled up to VDD by a 2kΩ off-chip resistor. Either the slave or master device can pull the lines down. The 2-wire Serial Interface protocol determines which device is allowed to pull the two lines down at any given time.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a 2-wire Serial Interface device consists of 7-bit of address and 1-bit of direction. A '0' in the LSB of the address indicates write mode, and a '1' indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The SCL pulse is provided by the master. The data must be stable during the HIGH period of the SCL. SDA can be only changed when the SCL is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

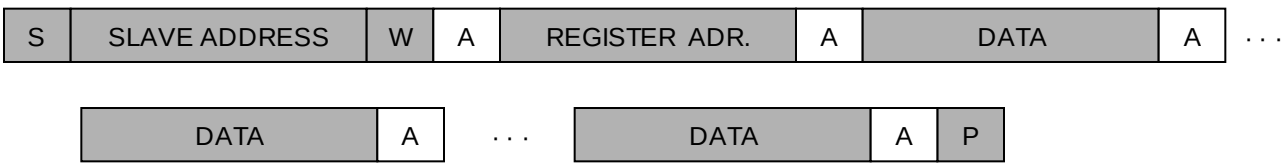
Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a write and a '1' indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master. If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The PC3030K uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit. A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

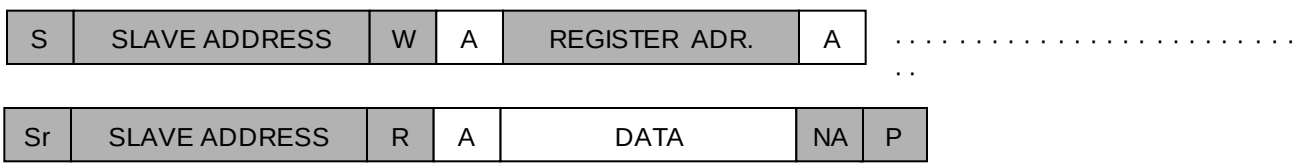
▶ 2-wire Serial Interface Functional Description

Single Write Mode operation

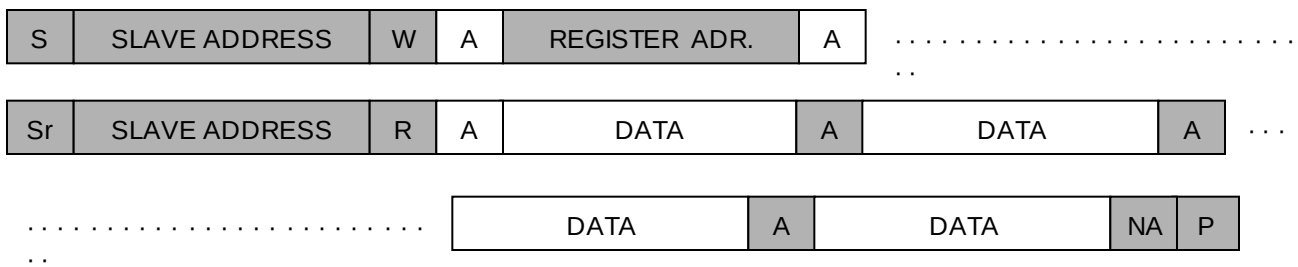
Multiple Write Mode (Register address is increased automatically)[1] operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically)[1] operation



From master to slave From slave to master

S: Start condition. Sr : Repeated Start (Start without preceding stop.)

SLAVE ADDRESS: It can be extended 60h to 67h by CADDR0 and CADDR1 pad

write address	60h	62h	64h	66h(default)
read address	61h	63h	65h	67h(default)

R/W: Read/Write selection. High = read / LOW = write.

A: Acknowledge bit. NA : No Acknowledge. DATA: 8-bit data. P: Stop condition.

Note 1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

▶ Register Tables (Detailed) : Group A

Register names are written in *slanted* characters. To differentiate between decimal, binary, and hexa numbers, (d, b, and h) are appended. The sensor should be reset by RSTB pin set low, after power is up, for at least 16 master clock periods. This will initialize all of the registers to their default values. Default values of 'U' are wire-strapping registers.

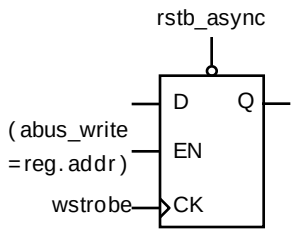
There are two register type.

1. Available Read Only (indicator is RO).
2. Available Read and Write (indicator is RW).

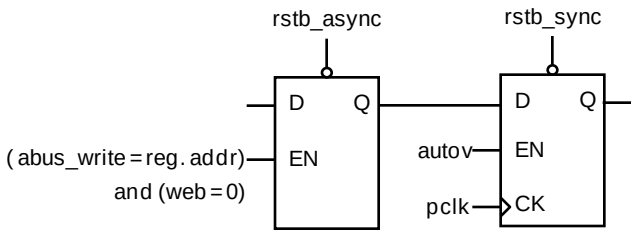
In addition, RW type register can be grouped by stage. There are 3 register stage.

1. 1 stage register (indicator is [5, 0]).
2. 2 stage register which is updated at auto vsync falling edge (indicator is [6, autov]).
3. 2 stage register which is updated at ae vsync falling edge (indicator is [6, aev]).
4. 2 stage register which is updated at ae vsync falling edge (indicator is [7, aev]) → this is 2 flip-flop structure.

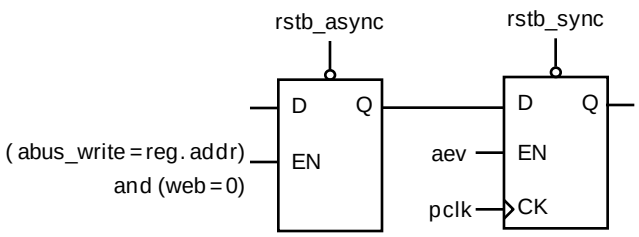
Below figure shows block diagram by register stage.



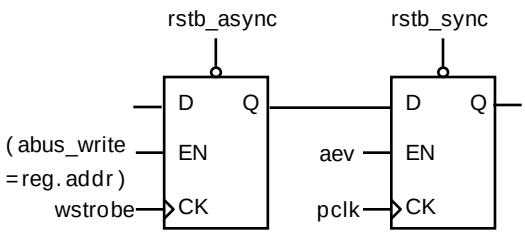
1. [1 stage register]



2. [2 stage register @ autov]



3. [2 stage register @ aev]



4. [2 stage register @ aev]

Where, abus_write means user input address by 2-wire serial interface. wstrobe and web is generated by SSCL pin. pclk means pixel clock for core. aev means ae vsync falling edge. autov means auto vsync falling edge. For more information of ae vsync and auto vsync, please refer to Reg. B-ACh~B1h.

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group A

GROUP A									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
0	00	DeviceID_H	48	30	00110000	RO	0	0	Device ID
1	01	DeviceID_L	48	30	00110000	RO	0	0	
2	02	RevNumber	0	00	00000000	RO	0	0	Revision number
3	03	bank	0	00	00000000	RW	5	0	Register group selector
4	04	chip_mode	u	u	uuuuuuuu	RW	7	aev	Chip mode selection(NTSC, PAL, VGA)
5	05	mirror	u	u	uuuuuuuu	RW	7	aev	Mirror
6	06	framewidth_h	u	u	uuuuuuuu	RW	7	aev	Framewidth
7	07	framewidth_l	u	u	uuuuuuuu	RW	7	aev	
8	08	fd_fheight_a_h	2	02	00000010	RW	6	aev	Frameheight
9	09	fd_fheight_a_l	u	u	uuuuuuuu	RW	7	aev	
10	0A	fd_fheight_b_h	2	02	00000010	RW	6	aev	
11	0B	fd_fheight_b_l	u	u	uuuuuuuu	RW	7	aev	
12	0C	windowx1_h	0	00	00000000	RW	6	aev	Window
13	0D	windowx1_l	1	01	00000001	RW	6	aev	
14	0E	windowy1_h	0	00	00000000	RW	6	aev	
15	0F	windowy1_l	1	01	00000001	RW	6	aev	
16	10	windowx2_h	2	02	00000010	RW	6	aev	
17	11	windowx2_l	128	80	10000000	RW	6	aev	
18	12	windowy2_h	u	u	uuuuuuuu	RW	7	aev	
19	13	windowy2_l	u	u	uuuuuuuu	RW	7	aev	
20	14	vsyncstartrow_f0_h	0	00	00000000	RW	6	aev	Vsync generation
21	15	vsyncstartrow_f0_l	23	17	00010111	RW	6	aev	
22	16	vsyncstoprow_f0_h	1	01	00000001	RW	6	aev	
23	17	vsyncstoprow_f0_l	u	u	uuuuuuuu	RW	7	aev	
24	18	vsyncstartrow_f1_h	1	01	00000001	RW	6	aev	
25	19	vsyncstartrow_f1_l	u	u	uuuuuuuu	RW	7	aev	
26	1A	vsyncstoprow_f1_h	2	02	00000010	RW	6	aev	
27	1B	vsyncstoprow_f1_l	u	u	uuuuuuuu	RW	7	aev	
28	1C	vsynccolumn_h	0	00	00000000	RW	5	0	
29	1D	vsynccolumn_l	2	02	00000010	RW	5	0	
30	1E	Reseved							
31	1F								
32	20	Reserved	8	08	00001000	RW	5	0	Need to stay fixed value
33	21	Reserved	0	00	00000000	RW	5	0	
34	22	Reserved	0	00	00000000	RW	5	0	
35	23	Reserved	80	50	01010000	RW	5	0	
36	24	Softreset	0	00	00000000	RW	5	0	Soft reset
37	25	Clkdiv	7	07	00000111	RW	6	aev	Colck divider
38	26	Reserved	0	00	00000000	RW	5	0	Need to stay fixed value
39	27	pad_control1	102	66	01100110	RW	5	0	Pad control
40	28	pad_control2	0	00	00000000	RW	5	0	
41	29	pad_control3	0	00	00000000	RW	5	0	
42	2A	pad_control4	0	00	00000000	RW	5	0	
43	2B	pad_control5	192	C0	11000000	RW	5	0	
44	2C	pad_control6	0	00	00000000	RW	5	0	
45	2D	strap_control	255	FF	11111111	RW	5	0	Strap control

(Group A – continued)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group A

GROUP A									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
46	2E	pixelbias	10	0A	00001010	RW	5	0	Pixel bias
47	2F	compbias	19	13	00010011	RW	5	0	Comparator bias
48	30	Reserved	47	2F	00101111	RW	5	0	Need to follow default or recommend value
49	31	Reserved	108	6C	01101100	RW	5	0	
50	32	Reserved	228	E4	11100100	RW	5	0	
51	33	Reserved	66	42	01000010	RW	5	0	
52	34	Reserved	64	40	01000000	RW	5	0	
53	35	Reserved	36	24	00100100	RW	5	0	
54 ~55	36 ~37	Reserved							
56	38	Reserved	240	F0	11110000	RW	5	0	Need to follow default or recommend value
57	39	Reserved	2	02	00000010	RW	5	0	
58	3A	Reserved	2	02	00000010	RW	5	0	
59	3B	Reserved	53	35	00110101	RW	5	0	
60	3C	Reserved	32	20	00100000	RW	5	0	
61	3D	Reserved	4	04	00000100	RW	5	0	
62	3E	Reserved	240	F0	11110000	RW	5	0	
63	3F	genlock_width	16	10	00010000	RW	5	0	Genlock pulse width
64	40	Reserved	0	00	00000000	RW	5	0	Need to follow default or recommend value
65	41	Reserved	12	0C	00001100	RW	5	0	
66	42	Reserved	12	0C	00001100	RW	5	0	
67	43	Reserved							
68	44	Reserved	4	04	00000100	RW	5	0	Need to follow default or recommend value
69	45	Reserved	10	0A	00001010	RW	5	0	
70	46	Reserved	64	40	01000000	RW	5	0	
71	47	Reserved	1	01	00000001	RW	5	0	
72	48	Reserved	129	81	10000001	RW	5	0	
73	49	bayer_control_01	5	05	00000101	RW	5	0	Don't need any changing except recommend value
74	4A	Reserved	254	FE	11111110	RW	5	0	
75	4B	Reserved	131	83	10000011	RW	5	0	
76	4C	Reserved	192	C0	11000000	RW	5	0	
77	4D	Reserved	112	70	01110000	RW	5	0	
78	4E	Reserved	0	00	00000000	RW	5	0	
79	4F	Reserved	17	11	00010001	RW	5	0	
80 ~83	50 ~53	Reserved							
84	54	Reserved	255	FF	11111111	RW	5	0	Don't need any changing except recommend value
85	55	Reserved	0	00	00000000	RW	5	0	
86	56	Reserved	0	00	00000000	RW	5	0	
87	57	Reserved	0	00	00000000	RW	5	0	
88	58	Reserved	0	00	00000000	RW	5	0	
89	59	Reserved	1	01	00000001	RW	5	0	
90	5A	Reserved	255	FF	11111111	RW	5	0	
91	5B	Reserved	7	07	00000111	RW	5	0	
92	5C	Reserved	255	FF	11111111	RW	5	0	

(Group A – continued)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
256	00	DeviceID_H	48	30	00110000	RO	0	0	Device ID
257	01	DeviceID_L	48	30	00110000	RO	0	0	
258	02	RevNumber	0	00	00000000	RO	0	0	Revision number
259	03	bank	2	02	00000010	RW	5	0	Register group selector
260	04	Reserved	247	F7	11110111	RW	6	aev	Must not change except recommend value
261	05	Reserved	255	FF	11111111	RW	6	aev	
262	06	isp_func_2	0	00	00000000	RW	6	aev	Isp function control
263	07	Reserved	161	A1	10100001	RW	6	aev	Must not change except recommend value
264	08	isp_func_4	0	00	00000000	RW	6	aev	Isp function control
265	09	isp_func_5	0	00	00000000	RW	6	aev	Isp function control
266	0A	tp_control_0	0	00	00000000	RW	5	0	Test pattern control
267	0B	Reserved							
268	0C	lens_red_e	81	51	01010001	RW	5	0	Lens shading compensation scale control
269	0D	lens_red_w	81	51	01010001	RW	5	0	
270	0E	lens_red_n	81	51	01010001	RW	5	0	
271	0F	lens_red_s	81	51	01010001	RW	5	0	
272	10	lens_g1_e	81	51	01010001	RW	5	0	
273	11	lens_g1_w	81	51	01010001	RW	5	0	
274	12	lens_g1_n	81	51	01010001	RW	5	0	
275	13	lens_g1_s	81	51	01010001	RW	5	0	
276	14	lens_g2_e	81	51	01010001	RW	5	0	
277	15	lens_g2_w	81	51	01010001	RW	5	0	
278	16	lens_g2_n	81	51	01010001	RW	5	0	
279	17	lens_g2_s	81	51	01010001	RW	5	0	
280	18	lens_blu_e	81	51	01010001	RW	5	0	
281	19	lens_blu_w	81	51	01010001	RW	5	0	
282	1A	lens_blu_n	81	51	01010001	RW	5	0	
283	1B	lens_blu_s	81	51	01010001	RW	5	0	
284	1C	lens_gainr	0	00	00000000	RW	6	aev	Lens shading compensation R gain
285	1D	lens_gaing1	0	00	00000000	RW	6	aev	Lens shading compensation G1 gain
286	1E	lens_gaing2	0	00	00000000	RW	6	aev	Lens shading compensation G2 gain
287	1F	lens_gainb	0	00	00000000	RW	6	aev	Lens shading compensation B gain
288	20	lens_rx	0	00	00000000	RW	5	0	Lens shading compensation center control
289	21	lens_ry	0	00	00000000	RW	5	0	
290	22	lens_g1x	0	00	00000000	RW	5	0	
291	23	lens_g1y	0	00	00000000	RW	5	0	
292	24	lens_g2x	0	00	00000000	RW	5	0	
293	25	lens_g2y	0	00	00000000	RW	5	0	
294	26	lens_bx	0	00	00000000	RW	5	0	
295	27	lens_by	0	00	00000000	RW	5	0	
296	28	Reserved							
297	29	format	0	00	00000000	RW	6	aev	Format control
298	2A	Reserved							
299	2B	Reserved	20	14	00010100	RW	5	0	Need to follow recommend or default setting
300	2C	Reserved	0	00	00000000	RW	5	0	
301	2D	Reserved	64	40	01000000	RW	5	0	
302	2E	Reserved	48	30	00110000	RW	5	0	

(Group B – continued)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
303	2F	edge_gain	20	14	00010100	RW	5	0	Edge gain
304	30	ec_pgain	128	80	10000000	RW	5	0	Positive max edge clamp gain
305	31	ec_mgain	128	80	10000000	RW	5	0	Negative max edge clamp gain
306	32	Reserved							
307	33	ccr_m11	51	33	00110011	RW	5	0	Color correction matrix value
308	34	ccr_m12	139	8B	10001011	RW	5	0	
309	35	ccr_m13	136	88	10001000	RW	5	0	
310	36	ccr_m21	134	86	10000110	RW	5	0	
311	37	ccr_m22	49	31	00110001	RW	5	0	
312	38	ccr_m23	138	8A	10001010	RW	5	0	
313	39	ccr_m31	131	83	10000011	RW	5	0	
314	3A	ccr_m32	143	8F	10001111	RW	5	0	
315	3B	ccr_m33	50	32	00110010	RW	5	0	
316	3C	Reserved							
317	3D	ygm1_y0	0	00	00000000	RW	5	0	Y gamma1 coefficient
318	3E	ygm1_y1	3	03	00000011	RW	5	0	
319	3F	ygm1_y2	12	0C	00001100	RW	5	0	
320	40	ygm1_y3	25	19	00011001	RW	5	0	
321	41	ygm1_y4	38	26	00100110	RW	5	0	
322	42	ygm1_y5	63	3F	00111111	RW	5	0	
323	43	ygm1_y6	82	52	01010010	RW	5	0	
324	44	ygm1_y7	110	6E	01101110	RW	5	0	
325	45	ygm1_y8	130	82	10000010	RW	5	0	
326	46	ygm1_y9	161	A1	10100001	RW	5	0	
327	47	ygm1_y10	185	B9	10111001	RW	5	0	
328	48	ygm1_y11	206	CE	11001110	RW	5	0	
329	49	ygm1_y12	224	E0	11100000	RW	5	0	
330	4A	ygm1_y13	240	F0	11110000	RW	5	0	
331	4B	ygm1_y14	255	FF	11111111	RW	5	0	
332	4C	ygm2_y0	0	00	00000000	RW	5	0	Y gamma2 coefficient
333	4D	ygm2_y1	11	0B	00001011	RW	5	0	
334	4E	ygm2_y2	23	17	00010111	RW	5	0	
335	4F	ygm2_y3	34	22	00100010	RW	5	0	
336	50	ygm2_y4	46	2E	00101110	RW	5	0	
337	51	ygm2_y5	64	40	01000000	RW	5	0	
338	52	ygm2_y6	80	50	01010000	RW	5	0	
339	53	ygm2_y7	110	6E	01101110	RW	5	0	
340	54	ygm2_y8	136	88	10001000	RW	5	0	
341	55	ygm2_y9	174	AE	10101110	RW	5	0	
342	56	ygm2_y10	202	CA	11001010	RW	5	0	
343	57	ygm2_y11	220	DC	11011100	RW	5	0	
344	58	ygm2_y12	236	EC	11101100	RW	5	0	
345	59	ygm2_y13	246	F6	11110110	RW	5	0	
346	5A	ygm2_y14	255	FF	11111111	RW	5	0	

(Group B – continued)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
347	5B	cgm1_y0	0	00	00000000	RW	5	0	RGB gamma1 coefficient
348	5C	cgm1_y1	11	0B	00001011	RW	5	0	
349	5D	cgm1_y2	23	17	00010111	RW	5	0	
350	5E	cgm1_y3	34	22	00100010	RW	5	0	
351	5F	cgm1_y4	46	2E	00101110	RW	5	0	
352	60	cgm1_y5	64	40	01000000	RW	5	0	
353	61	cgm1_y6	80	50	01010000	RW	5	0	
354	62	cgm1_y7	110	6E	01101110	RW	5	0	
355	63	cgm1_y8	136	88	10001000	RW	5	0	
356	64	cgm1_y9	174	AE	10101110	RW	5	0	
357	65	cgm1_y10	202	CA	11001010	RW	5	0	
358	66	cgm1_y11	220	DC	11011100	RW	5	0	
359	67	cgm1_y12	236	EC	11101100	RW	5	0	
360	68	cgm1_y13	246	F6	11110110	RW	5	0	
361	69	cgm1_y14	255	FF	11111111	RW	5	0	
362	6A	cgm2_y0	0	00	00000000	RW	5	0	RGB gamma2 coefficient
363	6B	cgm2_y1	11	0B	00001011	RW	5	0	
364	6C	cgm2_y2	23	17	00010111	RW	5	0	
365	6D	cgm2_y3	34	22	00100010	RW	5	0	
366	6E	cgm2_y4	46	2E	00101110	RW	5	0	
367	6F	cgm2_y5	64	40	01000000	RW	5	0	
368	70	cgm2_y6	80	50	01010000	RW	5	0	
369	71	cgm2_y7	110	6E	01101110	RW	5	0	
370	72	cgm2_y8	136	88	10001000	RW	5	0	
371	73	cgm2_y9	174	AE	10101110	RW	5	0	
372	74	cgm2_y10	202	CA	11001010	RW	5	0	
373	75	cgm2_y11	220	DC	11011100	RW	5	0	
374	76	cgm2_y12	236	EC	11101100	RW	5	0	
375	77	cgm2_y13	246	F6	11110110	RW	5	0	
376	78	cgm2_y14	255	FF	11111111	RW	5	0	
377	79	Reserved							
378	7A	sketch_offset	140	8C	10001100	RW	6	aev	Sketch offset
379	7B	scale_x	32	20	00100000	RW	6	aev	Horizontal scale factor
380	7C	scale_y	x	x	uuuuuuuu	RW	7	aev	Vertical scale factor
381	7D	scale_th_h	0	00	00000000	RW	6	aev	Scale buffer TH
382	7E	scale_th_l	10	0A	00001010	RW	6	aev	
383	7F	bw_th	128	80	10000000	RW	5	0	Black&white TH
384	80	cs11	37	25	00100101	RW	6	aev	Color saturation matrix value
385	81	cs12	0	00	00000000	RW	6	aev	
386	82	cs21	0	00	00000000	RW	6	aev	
387	83	cs22	37	25	00100101	RW	6	aev	
388 ~ 391	84 ~ 87	Reserved							

(Group B – continued)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
392	88	cb_offset	128	80	10000000	RW	6	aev	Cb offset
393	89	cr_offset	128	80	10000000	RW	6	aev	Cr offset
394	8A	c_max	127	7F	01111111	RW	6	aev	Cb/Cr max
395	8B	Reserved							
396	8C	auto_data_control	0	00	00000000	RW	5	0	Auto data control
397	8D	auto_off	0	00	00000000	RW	5	0	Auto off (MCU off)
398	8E	Reserved							
399	8F	y_weight	64	40	01000000	RW	6	aev	Y weight
400	90	y_max	254	FE	11111110	RW	6	aev	Y max
401	91	ycontrast_ref0	64	40	01000000	RW	5	0	Dark Y contrast fitting control
402	92	ycontrast_ref1	64	40	01000000	RW	5	0	
403	93	ycontrast_ref2	64	40	01000000	RW	5	0	
404	94	ycontrast	64	40	01000000	RW	6	aev	
405	95	ybrightness_ref0	0	00	00000000	RW	5	0	Dark Y brightness fitting control
406	96	ybrightness_ref1	0	00	00000000	RW	5	0	
407	97	ybrightness_ref2	0	00	00000000	RW	5	0	
408	98	ybrightness	0	00	00000000	RW	6	aev	
409	99	Reserved							
410	9A	sync_control_0	128	80	10000000	RW	6	aev	Sync control
411	9B	sync_control_1	0	00	00000000	RW	6	aev	
412	9C	sync_control_2	128	80	10000000	RW	6	aev	
413	9D	blankvalue	0	00	00000000	RW	5	aev	Data of black period
414	9E	Reserved	0	00	00000000	RW	5	0	Reserved register for test
415	9F	Reserved							
416	A0	prvc_wx1_h	0	00	00000000	RW	5	0	Privacy window size control
417	A1	prvc_wx1_l	1	01	00000001	RW	5	0	
418	A2	prvc_wx2_h	2	02	00000010	RW	5	0	
419	A3	prvc_wx2_l	128	80	10000000	RW	5	0	
420	A4	prvc_wy1_h	0	00	00000000	RW	5	0	
421	A5	prvc_wy1_l	1	01	00000001	RW	5	0	
422	A6	prvc_wy2_h	0	00	00000000	RW	5	0	
423	A7	prvc_wy2_l	240	F0	11110000	RW	5	0	
424	A8	prvc_y	0	00	00000000	RW	5	0	YCbCr of privacy window
425	A9	prvc_cb	128	80	10000000	RW	5	0	
426	AA	prvc_cr	128	80	10000000	RW	5	0	
427	AB	Reserved							
428	AC	Reserved	0	00	00000000	RW	5	0	Don't change these values. Changed values make sensor malfunction.
429	AD	Reserved	0	00	00000000	RW	5	0	
430	AE	Reserved	1	01	00000001	RW	5	0	
431	AF	Reserved	241	F1	11110001	RW	5	0	
432	B0	Reserved	2	02	00000010	RW	5	0	
433	B1	Reserved	59	3B	00111011	RW	5	0	
434	B2	Reserved							
435	B3	ae_fwx1_h	0	00	00000000	RW	5	0	AE full window X start position
436	B4	ae_fwx1_l	1	01	00000001	RW	5	0	
437	B5	ae_fwx2_h	2	02	00000010	RW	5	0	AE full window X stop position
438	B6	ae_fwx2_l	128	80	10000000	RW	5	0	

(Group B – continued)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
439	B7	ae_fwy1_h	0	00	00000000	RW	5	0	AE full window Y start position
440	B8	ae_fwy1_l	1	01	00000001	RW	5	0	
441	B9	ae_fwy2_h	u	u	uuuuuuuu	RW	5	0	AE full window Y stop position
442	BA	ae_fwy2_l	u	u	uuuuuuuu	RW	5	0	
443	BB	ae_cwx1_h	0	00	00000000	RW	5	0	AE center window X start position
444	BC	ae_cwx1_l	214	D6	11010110	RW	5	0	
445	BD	ae_cwx2_h	1	01	00000001	RW	5	0	AE center window X stop position
446	BE	ae_cwx2_l	171	AB	10101011	RW	5	0	
447	BF	ae_cwy1_h	0	00	00000000	RW	5	0	AE center window Y start position
448	C0	ae_cwy1_l	u	u	uuuuuuuu	RW	5	0	
449	C1	ae_cwy2_h	0	00	00000000	RW	5	0	AE center window Y stop position
450	C2	ae_cwy2_l	u	u	uuuuuuuu	RW	5	0	
451	C3	ae_xaxis_h	1	01	00000001	RW	5	0	AE window X axis
452	C4	ae_xaxis_l	65	41	01000001	RW	5	0	
453	C5	ae_yaxis_h	0	00	00000000	RW	5	0	AE window Y axis
454	C6	ae_yaxis_l	u	u	uuuuuuuu	RW	5	0	
455	C7	awb_fwx1_h	0	00	00000000	RW	5	0	AWB full window X start position
456	C8	awb_fwx1_l	1	01	00000001	RW	5	0	
457	C9	awb_fwx2_h	2	02	00000010	RW	5	0	AWB full window X stop position
458	CA	awb_fwx2_l	128	80	10000000	RW	5	0	
459	CB	awb_fwy1_h	0	00	00000000	RW	5	0	AWB full window Y start position
460	CC	awb_fwy1_l	1	01	00000001	RW	5	0	
461	CD	awb_fwy2_h	u	u	uuuuuuuu	RW	5	0	AWB full window Y stop position
462	CE	awb_fwy2_l	u	u	uuuuuuuu	RW	5	0	
463	CF	awb_cwx1_h	0	00	00000000	RW	5	0	AWB center window X start position
464	D0	awb_cwx1_l	214	D6	11010110	RW	5	0	
465	D1	awb_cwx2_h	1	01	00000001	RW	5	0	AWB center window X stop position
466	D2	awb_cwx2_l	171	AB	10101011	RW	5	0	
467	D3	awb_cwy1_h	0	00	00000000	RW	5	0	AWB center window Y start position
468	D4	awb_cwy1_l	u	u	uuuuuuuu	RW	5	0	
469	D5	awb_cwy2_h	0	00	00000000	RW	5	0	AWB center window Y stop position
470	D6	awb_cwy2_l	u	u	uuuuuuuu	RW	5	0	
471	D7	Reserved							
472	D8	af_cwx1_h	0	00	00000000	RW	5	0	AF center window X start position
473	D9	af_cwx1_l	214	D6	11010110	RW	5	0	
474	DA	af_cwx2_h	1	01	00000001	RW	5	0	AF center window X stop position
475	DB	af_cwx2_l	171	AB	10101011	RW	5	0	
476	DC	af_cwy1_h	0	00	00000000	RW	5	0	AF center window Y start position
477	DD	af_cwy1_l	u	u	uuuuuuuu	RW	5	0	
478	DE	af_cwy2_h	0	00	00000000	RW	5	0	AF center window Y stop position
479	DF	af_cwy2_l	u	u	uuuuuuuu	RW	5	0	
480	E0	af_cweight	8	08	00001000	RW	5	0	AF weight center
481	E1	af_edge_th	0	00	00000000	RW	5	0	AF edge TH
482	E2	Reserved							
483	E3	md_yth1	64	40	01000000	RW	5	0	Y threshold1 for motion detection
484	E4	md_yth2	64	40	01000000	RW	5	0	Y threshold2 for motion detection
485	E5	md_yth3	64	40	01000000	RW	5	0	Y threshold3 for motion detection

(Group B – continued)

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
486	E6	md_yth4	64	40	01000000	RW	5	0	Y threshold4 for motion detection
487	E7	md_diff1	64	40	01000000	RW	5	0	Difference1 for motion detection
488	E8	md_diff2	64	40	01000000	RW	5	0	Difference2 for motion detection
489	E9	md_diff3	64	40	01000000	RW	5	0	Difference3 for motion detection
490	EA	md_diff4	64	40	01000000	RW	5	0	Difference4 for motion detection
491	EB	md_interval	8	08	00001000	RW	5	0	Intervals of frames used for motion detection
492	EC	md_alarm_y	0	00	00000000	RW	5	0	YCbCr for Motion detection alarm
493	ED	md_alarm_cb	128	80	10000000	RW	5	0	
494	EE	md_alarm_cr	128	80	10000000	RW	5	0	
495	EF	md_alarmnumb	4	04	00000100	RW	5	0	Number of Motion detection alarm
496	F0	md_alarm_xlw	4	04	00000100	RW	5	0	X width of motion detection alarm
497	F1	md_alarm_ylw	4	04	00000100	RW	5	0	Y width of motion detection alarm
498	F2	md_alarmdur_h	0	00	00000000	RW	5	0	Period of motion detection alarm
499	F3	md_alarmdur_l	60	3C	00111100	RW	5	0	
500	F4	md_sleepdur_h	2	02	00000010	RW	5	0	Motion detection sleep
501	F5	md_sleepdur_l	58	3A	00111010	RW	5	0	
502	F6	md_section7	0	00	00000000	RW	5	0	Image section 7 for motion detection
503	F7	md_section6	0	00	00000000	RW	5	0	Image section 6 for motion detection
504	F8	md_section5	0	00	00000000	RW	5	0	Image section 5 for motion detection
505	F9	md_section4	0	00	00000000	RW	5	0	Image section 4 for motion detection
506	FA	md_section3	0	00	00000000	RW	5	0	Image section 3 for motion detection
507	FB	md_section2	0	00	00000000	RW	5	0	Image section 2 for motion detection
508	FC	md_section1	0	00	00000000	RW	5	0	Image section 1 for motion detection
509	FD	md_section0	0	00	00000000	RW	5	0	Image section 0 for motion detection
510 ~511	FE ~FF	Reserved							

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
512	00	DeviceID_H	48	30	00110000	RO	0	0	Device ID
513	01	DeviceID_L	48	30	00110000	RO	0	0	
514	02	RevNumber	0	00	00000000	RO	0	0	Revision number
515	03	bank	2	02	00000010	0	5	0	Register group selector
516	04	Reserved	152	98	10011000	RW	6	autov	Reserved for internal automatic control
517	05	Reserved	101	65	01100101	RW	6	autov	
518	06	Reserved	128	80	10000000	RW	6	autov	
519	07	Reserved	128	80	10000000	RW	6	autov	
520	08	Reserved	0	00	00000000	RW	6	autov	
521	09	Reserved	1	01	00000001	RW	6	autov	
522	0A	Reserved	149	95	10010101	RW	6	autov	
523	0B	Reserved	119	77	01110111	RW	6	autov	
524	0C	Reserved	36	24	00100100	RW	6	autov	
525	0D	Reserved	128	80	10000000	RW	6	autov	
526	0E	Reserved	238	EE	11101110	RW	5	0	
527	0F	Reserved							
528	10	expfrmh_h	2	02	00000010	RW	5	0	AE reference
529	11	expfrmh_l	u	u	uuuuuuuu	RW	5	0	
530	12	midfrmheight_h	2	02	00000010	RW	5	0	
531	13	midfrmheight_l	u	u	uuuuuuuu	RW	5	0	
532	14	maxfrmheight_h	2	02	00000010	RW	5	0	
533	15	maxfrmheight_l	u	u	uuuuuuuu	RW	5	0	
534	16	minexp_h	0	00	00000000	RW	5	0	
535	17	minexp_m	0	00	00000000	RW	5	0	
536	18	minexp_l	12	0C	00001100	RW	5	0	
537	19	midexp_t	1	01	00000001	RW	5	0	
538	1A	midexp_h	133	85	10000101	RW	5	0	
539	1B	midexp_m	64	40	01000000	RW	5	0	
540	1C	maxexp_t	1	01	00000001	RW	5	0	
541	1D	maxexp_h	133	85	10000101	RW	5	0	
542	1E	maxexp_m	64	40	01000000	RW	5	0	
543	1F	Reserved							
544	20	ext_inttime_h	0	00	00000000	RW	6	autov	Manual integration time @ external AE mode
545	21	ext_inttime_m	128	80	10000000	RW	6	autov	
546	22	ext_inttime_l	0	00	00000000	RW	6	autov	
547	23	ext_glbg_h	1	01	00000001	RW	6	autov	Manual analog gain @ external AE mode
548	24	ext_glbg_l	0	00	00000000	RW	6	autov	
549	25	exposure_t	0	00	00000000	RW	6	autov	Exposure
550	26	exposure_h	1	01	00000001	RW	6	autov	
551	27	exposure_m	64	40	01000000	RW	6	autov	
552	28	exposure_l	0	00	00000000	RW	6	autov	
553	29	Reserved							
554	2A	ae_ysat	68	44	01000100	RW	6	autov	Saturation decision TH
555	2B	Reserved							
556	2C	sratio_weight	8	08	00001000	RW	5	0	Saturation ratio weight
557	2D	sratio	0	00	00000000	RW	5	0	Saturation ratio

(Group C – continued)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
558	2E	ae_weight1	8	08	00001000	RW	5	0	AE weight peripheral
559	2F	ae_weight2	8	08	00001000	RW	5	0	
560	30	ae_weight3	8	08	00001000	RW	5	0	
561	31	ae_weight4	8	08	00001000	RW	5	0	
562	32	ae_weightc	8	08	00001000	RW	5	0	AE weight center
563	33	Reserved	16	10	00010000	RW	5	0	Need to follow default or recommend value
564	34	Reserved	64	40	01000000	RW	5	0	
565	35	Reserved	128	80	10000000	RW	5	0	
566	36	Reserved	255	FF	11111111	RW	5	0	
567	37	ymean_h	0	00	00000000	RW	5	0	Y mean
568	38	ymean_l	128	80	10000000	RW	5	0	
569	39	max_yt1	160	A0	10100000	RW	6	autov	Dynamic Y target control
570	3A	max_yt2	128	80	10000000	RW	6	autov	
571	3B	min_yt1	128	80	10000000	RW	6	autov	
572	3C	min_yt2	80	50	01010000	RW	6	autov	
573	3D	gg_ref0	36	24	00100100	RW	6	autov	
574	3E	gg_ref1	75	4B	01001011	RW	6	autov	
575	3F	sratio_ref0	4	04	00000100	RW	6	autov	
576	40	sratio_ref1	16	10	00010000	RW	6	autov	
577	41	sratio_ref2	26	1A	00011010	RW	6	autov	
578	42	sratio_ref3	50	32	00110010	RW	6	autov	
579	43	yt_step	4	04	00000100	RW	5	0	
580	44	ytarget	112	70	01110000	RW	5	0	Y target
581	45	user_wyt	128	80	10000000	RW	6	autov	User weight Y target
582	46	ae_up_speed	8	08	00001000	RW	6	autov	AE upside speed
583	47	ae_down_speed	8	08	00001000	RW	6	autov	AE downside speed
584	48	ae_lock	16	10	00010000	RW	6	autov	AE lock range
585	49	auto_flag	0	00	00000000	RW	5	0	Auto flag
586	4A	afd_th_h	2	02	00000010	RW	5	0	Auto flicker detection TH.
587	4B	afd_th_m	7	07	00000111	RW	5	0	
588	4C	awb_full_th_t	1	01	00000001	RW	5	0	AWB full Control
589	4D	awb_full_th_h	133	85	10000101	RW	5	0	
590	4E	awb_full_th_m	64	40	01000000	RW	5	0	
591	4F	awb_full	0	00	00000000	RW	5	0	
592	50	Reserved							
593	51	awb_p1Ax	41	29	00101001	RW	5	0	AWB sampling range selection
594	52	awb_p1Ay	57	39	00111001	RW	5	0	
595	53	awb_p2Ax	54	36	00110110	RW	5	0	
596	54	awb_p2Ay	25	19	00011001	RW	5	0	
597	55	awb_osAx	9	09	00001001	RW	5	0	
598	56	awb_osAy	16	10	00010000	RW	5	0	
599	57	awb_slopeA	160	A0	10100000	RW	5	0	
600	58	awb_p1Bx	54	36	00110110	RW	5	0	
601	59	awb_p1By	33	21	00100001	RW	5	0	
602	5A	awb_p2Bx	105	69	01101001	RW	5	0	
603	5B	awb_p2By	20	14	00010100	RW	5	0	
604	5C	awb_osBx	12	0C	00001100	RW	5	0	

(Group C – continued)

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
605	5D	awb_osBy	4	04	00000100	RW	5	0	AWB sampling range selection
606	5E	awb_slopeB	16	10	00010000	RW	5	0	
607	5F	awb_maxc	250	FA	11111010	RW	5	0	
608	60	awb_minc	8	08	00001000	RW	5	0	
609	61	awb_weight_c	5	05	00000101	RW	5	0	AWB weight for center
610	62	awb_weight_p	11	0B	00001011	RW	5	0	AWB weight for peripheral
611	63	awb_wspeed	4	04	00000100	RW	5	0	AWB weight speed
612 ~613	64 ~65	Reserved							
614	66	rg_ratio_a	122	7A	01111010	RW	5	0	Target awb ratio fitting reference
615	67	bg_ratio_a	120	78	01111000	RW	5	0	
616	68	rg_ratio_b	128	80	10000000	RW	5	0	
617	69	bg_ratio_b	128	80	10000000	RW	5	0	
618	6A	rg_ratio_c	128	80	10000000	RW	5	0	
619	6B	bg_ratio_c	128	80	10000000	RW	5	0	
620	6C	ratio_axis_a	42	2A	00101010	RW	5	0	
621	6D	ratio_axis_b	80	50	01010000	RW	5	0	
622	6E	ratio_axis_c	87	57	01010111	RW	5	0	
623	6F	awb_rgratio	128	80	10000000	RW	5	0	AWB RG ratio control
624	70	awb_bgratio	128	80	10000000	RW	5	0	AWB BG ratio control
625	71	awb_lock	16	10	00010000	RW	5	0	AWB lock range
626	72	awb_speed	4	04	00000100	RW	5	0	AWB speed
627	73	awb_rgain_min1	42	2A	00101010	RW	5	0	AWB gain clamping fitting control
628	74	awb_rgain_min2	40	28	00101000	RW	5	0	
629	75	awb_rgain_max1	90	5A	01011010	RW	5	0	
630	76	awb_rgain_max2	93	5D	01011101	RW	5	0	
631	77	awb_bgain_min1	80	50	01010000	RW	5	0	
632	78	awb_bgain_min2	77	4D	01001101	RW	5	0	
633	79	awb_bgain_max1	183	B7	10110111	RW	5	0	
634	7A	awb_bgain_max2	186	BA	10111010	RW	5	0	
635	7B	awb_cmp_th1_h	1	01	00000001	RW	5	0	
636	7C	awb_cmp_th1_m	0	00	00000000	RW	5	0	
637	7D	awb_cmp_th2_h	2	02	00000010	RW	5	0	
638	7E	awb_cmp_th2_m	7	07	00000111	RW	5	0	
639	7F	cs11_a	40	28	00101000	RW	5	0	Color saturation matrix fitting reference
640	80	cs12_a	0	00	00000000	RW	5	0	
641	81	cs21_a	0	00	00000000	RW	5	0	
642	82	cs22_a	40	28	00101000	RW	5	0	
643	83	cs11_b	36	24	00100100	RW	5	0	
644	84	cs12_b	0	00	00000000	RW	5	0	
645	85	cs21_b	0	00	00000000	RW	5	0	
646	86	cs22_b	40	28	00101000	RW	5	0	
647	87	cs11_c	32	20	00100000	RW	5	0	
648	88	cs12_c	0	00	00000000	RW	5	0	
649	89	cs21_c	0	00	00000000	RW	5	0	
650	8A	cs22_c	32	20	00100000	RW	5	0	

(Group C – continued)

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
651	8B	lens_gainr_a	2	02	00000010	RW	5	0	Lens gain fitting reference
652	8C	lens_gainb_a	0	00	00000000	RW	5	0	
653	8D	lens_gainr_b	2	02	00000010	RW	5	0	
654	8E	lens_gainb_b	0	00	00000000	RW	5	0	
655	8F	lens_gainr_c	2	02	00000010	RW	5	0	
656	90	lens_gainb_c	0	00	00000000	RW	5	0	
657	91	axis_a	42	2A	00101010	RW	5	0	CS matrix / lens gain fitting reference
658	92	axis_b	80	50	01010000	RW	5	0	
659	93	axis_c	87	57	01010111	RW	5	0	
660	94	user_cs	32	20	00100000	RW	5	0	User CS gain
661 ~ 669	95 ~ 9D	Reserved							
670	9E	dark_xref1_g0	12	0C	00001100	RW	5	0	Dark filter x-axis reference
671	9F	dark_xref2_g0	32	20	00100000	RW	5	0	
672	A0	dark_xref3_g0	64	40	01000000	RW	5	0	
673	A1	Reserved	12	0C	00001100	RW	5	0	Reserved for xref option.
674	A2	Reserved	24	18	00011000	RW	5	0	
675	A3	Reserved	32	20	00100000	RW	5	0	
676	A4	totalgain	2	02	00000010	RW	6	autov	Total gain
677	A5	Reserved							
678	A6	dark_lens0	0	00	00000000	RW	5	0	Dark lens fitting control
679	A7	dark_lens1	0	00	00000000	RW	5	0	
680	A8	dark_lens2	0	00	00000000	RW	5	0	
681	A9	dark_lens	0	00	00000000	RW	6	aev	
682	AA	Reserved	0	00	00000000	RW	5	0	Reserved for extra filtering
683	AB	Reserved	16	10	00010000	RW	5	0	
684	AC	Reserved	32	20	00100000	RW	5	0	
685	AD	Reserved	0	00	00000000	RW	6	aev	
686	AE	Reserved	0	00	00000000	RW	5	0	Reserved for extra filtering
687	AF	Reserved	12	0C	00001100	RW	5	0	
688	B0	Reserved	28	1C	00011100	RW	5	0	
689	B1	Reserved	0	00	00000000	RW	6	aev	
690	B2	dark_blf0	95	5F	01011111	RW	5	0	Dark bilateral filter fitting control
691	B3	dark_blf1	63	3F	00111111	RW	5	0	
692	B4	dark_blf2	63	3F	00111111	RW	5	0	
693	B5	dark_blf	127	7F	01111111	RW	6	aev	
694	B6	dark_nf0	64	40	01000000	RW	5	0	Dark noise floor fitting control
695	B7	dark_nf1	64	40	01000000	RW	5	0	
696	B8	dark_nf2	64	40	01000000	RW	5	0	
697	B9	dark_nf	1	01	00000001	RW	6	aev	

(Group C – continued)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
698	BA	Reserved	0	00	00000000	RW	5	0	Reserved for dark filter control
699	BB	Reserved	8	08	00001000	RW	5	0	
700	BC	Reserved	24	18	00011000	RW	5	0	
701	BD	Reserved	0	00	00000000	RW	6	aev	
702	BE	Reserved	16	10	00010000	RW	5	0	Reserved for dark filter control
703	BF	Reserved	16	10	00010000	RW	5	0	
704	C0	Reserved	16	10	00010000	RW	5	0	
705	C1	Reserved	16	10	00010000	RW	6	aev	
706	C2	Reserved	4	04	00000100	RW	5	0	Reserved for dark filter control
707	C3	Reserved	8	08	00001000	RW	5	0	
708	C4	Reserved	24	18	00011000	RW	5	0	
709	C5	Reserved	4	04	00000100	RW	6	aev	
710	C6	Reserved							
711	C7	y_cont_th_ref0	255	FF	11111111	RW	5	0	Dark y contrast th fitting control
712	C8	y_cont_th_ref1	255	FF	11111111	RW	5	0	
713	C9	y_cont_th_ref2	255	FF	11111111	RW	5	0	
714	CA	y_cont_th	255	FF	11111111	RW	6	aev	
715	CB	y_cont_slope_ref0	80	50	01010000	RW	5	0	Dark y contrast slope fitting control
716	CC	y_cont_slope_ref1	80	50	01010000	RW	5	0	
717	CD	y_cont_slope_ref2	80	50	01010000	RW	5	0	
718	CE	y_cont_slope	80	50	01010000	RW	6	aev	
719 ~ 721	CF ~ D1	Reserved							
722	D2	dark_y_gm0	0	00	00000000	RW	5	0	Dark Y gamma fitting control
723	D3	dark_y_gm1	16	10	00010000	RW	5	0	
724	D4	dark_y_gm2	63	3F	00111111	RW	5	0	
725	D5	dark_y_gm	0	00	00000000	RW	6	aev	
726	D6	dark_rgb_gm0	0	00	00000000	RW	5	0	Dark RGB gamma fitting control
727	D7	dark_rgb_gm1	0	00	00000000	RW	5	0	
728	D8	dark_rgb_gm2	0	00	00000000	RW	5	0	
729	D9	dark_rgb_gm	0	00	00000000	RW	6	aev	
730	DA	dark_ccr0	0	00	00000000	RW	5	0	Dark color correction fitting control
731	DB	dark_ccr1	4	04	00000100	RW	5	0	
732	DC	dark_ccr2	8	08	00001000	RW	5	0	
733	DD	dark_ccr	0	00	00000000	RW	6	aev	
734	DE	Reserved							
735	DF	inttime_h	1	01	00000001	RW	6	aev	Integration time (line)
736	E0	inttime_m	64	40	01000000	RW	6	aev	
737	E1	inttime_l	0	00	00000000	RW	6	aev	Integration time (column)
738	E2	globalgain	0	00	00000000	RW	6	aev	Analog gain
739	E3	digitalgain	64	40	01000000	RW	6	aev	Digital gain
740	E4	Reserved							
741	E5	Reserved	0	00	00000000	RW	5	0	Need to follow default or recommend value
742	E6	Reserved	0	00	00000000	RW	5	0	
743	E7	Reserved	6	06	00000110	RW	5	0	
744	E8	Reserved	10	0A	00001010	RW	5	0	

(Group C – continued)

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
745	E9	Reserved	13	0D	00001101	RW	5	0	Need to follow default or recommend value
746	EA	Reserved	15	0F	00001111	RW	5	0	
747	EB	Reserved							
748	EC	wb_rgain	93	5D	01011101	RW	6	aev	White balance R gain
749	ED	wb_ggain	64	40	01000000	RW	6	aev	White balance G gain
750	EE	wb_bgain	94	5E	01011110	RW	6	aev	White balance B gain
751	EF	rgain_no_normal_h	93	5D	01011101	RW	5	0	White balance R gain is not normalized
752	F0	rgain_no_normal_l	0	00	00000000	RW	5	0	(Monitoring)
753	F1	bgain_no_normal_h	94	5E	01011110	RW	5	0	White balance B gain is not normalized
754	F2	bgain_no_normal_l	0	00	00000000	RW	5	0	(Monitoring)
755	F3	inv_rgain	44	2C	00101100	RW	6	aev	Inverse white balance R gain
756	F4	inv_ggain	64	40	01000000	RW	6	aev	Inverse white balance G gain
757	F5	inv_bgain	43	2B	00101011	RW	6	aev	Inverse white balance B gain
758	F6	wb_gratio	128	80	10000000	RW	5	0	Gr/Gb ratio of white balance gain
759	F7	Reserved							
760	F8	Reserved	12	0C	00001100	RW	5	0	Must not change any value except recommend value
761	F9	Reserved	42	2A	00101010	RW	5	0	
762	FA	Reserved	0	00	00000000	RW	5	0	
763	FB	Reserved	6	06	00000110	RW	5	0	
764	FC	Reserved	0	00	00000000	RW	5	0	
765 ~ 767	FD ~ FF	Reserved							

▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		Dec	hex	bin				
768	00	DeviceID_H	48	30	00110000	RO	0	0	Device ID
769	01	DeviceID_L	48	30	00110000	RO	0	0	
770	02	RevNumber	0	00	00000000	RO	0	0	Revision number
771	03	Bank	3	03	00000011	RW	5	0	Register group selector
772	04	Reserved	0	00	00000000	RO	0	0	Reserved for test
773	05	Reserved	0	00	00000000	RO	0	0	
774	06	Reserved	0	00	00000000	RO	0	0	
775	07	Reserved	0	00	00000000	RO	0	0	
776	08	Reserved	0	00	00000000	RO	0	0	
777	09	Reserved	0	00	00000000	RO	0	0	
778	0A	Reserved							
779	0B	real_led_data	0	00	00000000	RO	0	0	Current LED data
780	0C	sif_state	0	00	00000000	RO	0	0	I2c master state monitor
781	0D	fd_state	0	00	00000000	RO	0	0	Current Flicker state
782	0E	fd_period_h	0	00	00000000	RO	0	0	Current Flicker period
783	0F	fd_period_m	0	00	00000000	RO	0	0	
784	10	fd_period_l	0	00	00000000	RO	0	0	
785	11	fd_fheight_h	0	00	00000000	RO	0	0	Current frameheight
786	12	fd_fheight_l	0	00	00000000	RO	0	0	
787	13	Reserved							
788	14	Reserved	0	00	00000000	RO	0	0	Reserved for test
789	15	Reserved	0	00	00000000	RO	0	0	
790	16	Reserved	0	00	00000000	RO	0	0	
791	17	Reserved	0	00	00000000	RO	0	0	
792	18	Reserved	0	00	00000000	RO	0	0	
793	19	Reserved	0	00	00000000	RO	0	0	
794	1A	Reserved	0	00	00000000	RO	0	0	
795	1B	Reserved	0	00	00000000	RO	0	0	
796	1C	Reserved	0	00	00000000	RO	0	0	
797	1D	Reserved	0	00	00000000	RO	0	0	
798	1E	Reserved	0	00	00000000	RO	0	0	
799	1F	Reserved	0	00	00000000	RO	0	0	
800	20	Reserved	0	00	00000000	RO	0	0	
801	21	Reserved	0	00	00000000	RO	0	0	
802	22	Reserved	0	00	00000000	RO	0	0	
803	23	Reserved	0	00	00000000	RO	0	0	
804	24	Reserved	0	00	00000000	RO	0	0	
805	25	Reserved	0	00	00000000	RO	0	0	
806	26	Reserved	0	00	00000000	RO	0	0	
807	27	Reserved	0	00	00000000	RO	0	0	
808	28	Reserved	0	00	00000000	RO	0	0	
809	29	sum_sample1_byte3	0	00	00000000	RO	0	0	Summation of Y in AE peripheral 1 window
810	2A	sum_sample1_byte2	0	00	00000000	RO	0	0	
811	2B	sum_sample1_byte1	0	00	00000000	RO	0	0	
812	2C	sum_sample1_byte0	0	00	00000000	RO	0	0	

(Group D – continued)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
813	2D	sum_sample2_byte3	0	00	00000000	RO	0	0	Summation of Y in AE peripheral 2 window
814	2E	sum_sample2_byte2	0	00	00000000	RO	0	0	
815	2F	sum_sample2_byte1	0	00	00000000	RO	0	0	
816	30	sum_sample2_byte0	0	00	00000000	RO	0	0	
817	31	sum_sample3_byte3	0	00	00000000	RO	0	0	Summation of Y in AE peripheral 3 window
818	32	sum_sample3_byte2	0	00	00000000	RO	0	0	
819	33	sum_sample3_byte1	0	00	00000000	RO	0	0	
820	34	sum_sample3_byte0	0	00	00000000	RO	0	0	
821	35	sum_sample4_byte3	0	00	00000000	RO	0	0	Summation of Y in AE peripheral 4 window
822	36	sum_sample4_byte2	0	00	00000000	RO	0	0	
823	37	sum_sample4_byte1	0	00	00000000	RO	0	0	
824	38	sum_sample4_byte0	0	00	00000000	RO	0	0	
825	39	sum_samplec_byte3	0	00	00000000	RO	0	0	Summation of Y in AE center window
826	3A	sum_samplec_byte2	0	00	00000000	RO	0	0	
827	3B	sum_samplec_byte1	0	00	00000000	RO	0	0	
828	3C	sum_samplec_byte0	0	00	00000000	RO	0	0	
829	3D	Reserved	0	00	00000000	RO	0	0	Reserved for test
830	3E	Reserved							
831	3F	Reserved	0	00	00000000	RO	0	0	AWB flag
832	40	Reserved	0	00	00000000	RO	0	0	Reserved for AWB status.
833	41	Reserved	0	00	00000000	RO	0	0	
834	42	Reserved	0	00	00000000	RO	0	0	
835	43	Reserved	0	00	00000000	RO	0	0	
836	44	Reserved	0	00	00000000	RO	0	0	
837	45	Reserved	0	00	00000000	RO	0	0	
838	46	Reserved	0	00	00000000	RO	0	0	Reserved for test
839	47	Reserved	0	00	00000000	RO	0	0	Reserved for test
840	48	monitor_proximity	0	00	00000000	RO	0	0	Current maximum value of edge
841	49	Reserved							
842	4A	Reserved	0	00	00000000	RO	0	0	Reserved for test
843	4B	Reserved	0	00	00000000	RO	0	0	
844	4C	Reserved	0	00	00000000	RO	0	0	
845	4D	Reserved	0	00	00000000	RO	0	0	
846	4E	Reserved	0	00	00000000	RO	0	0	
847	4F	Reserved	0	00	00000000	RO	0	0	
848	50	Reserved	0	00	00000000	RO	0	0	
849	51	Reserved	0	00	00000000	RO	0	0	
850	52	Reserved	0	00	00000000	RO	0	0	
851	53	Reserved	0	00	00000000	RO	0	0	
852	54	Reserved	0	00	00000000	RO	0	0	
853	55	Reserved							

(Group D – continued)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
854	56	Reserved	0	00	00000000	RO	0	0	Reserved for motion detection
855	57	Reserved	0	00	00000000	RO	0	0	
856	58	Reserved	0	00	00000000	RO	0	0	
857	59	Reserved	0	00	00000000	RO	0	0	
858	5A	Reserved	0	00	00000000	RO	0	0	
859	5B	Reserved	0	00	00000000	RO	0	0	
860	5C	Reserved	0	00	00000000	RO	0	0	
861	5D	Reserved	0	00	00000000	RO	0	0	
862	5E	Reserved	0	00	00000000	RO	0	0	Reserved for auto focus
863	5F	Reserved	0	00	00000000	RO	0	0	
864	60	Reserved	0	00	00000000	RO	0	0	
865	61	Reserved	0	00	00000000	RO	0	0	
866	62	Reserved							
867	63	sync_blankEAV_f0	182	B6	10110110	RW	5	0	Blank EAV for field0 of CCIR656 data or blank EAV for frame data
868	64	sync_blankSAV_f0	171	AB	10101011	RW	5	0	Blank SAV for field0 of CCIR656 data or blank SAV for frame data
869	65	sync_activeEAV_f0	157	9D	10011101	RW	5	0	Active EAV for field0 of CCIR656 data or active EAV for frame data
870	66	sync_activeSAV_f0	128	80	10000000	RW	5	0	Active SAV for field0 of CCIR656 data or active SAV for frame data
871	67	sync_blankEAV_f1	241	F1	11110001	RW	5	0	blank EAV for field1 of CCIR656 data
872	68	sync_blankSAV_f1	236	EC	11101100	RW	5	0	blank SAV for field1 of CCIR656 data
873	69	sync_activeEAV_f1	218	DA	11011010	RW	5	0	active EAV for field1 of CCIR656 data
874	6A	sync_activeSAV_f1	199	C7	11000111	RW	5	0	active SAV for field1 of CCIR656 data
875	6B	sync_CCIR_FF	255	FF	11111111	RW	5	0	CCIR data format
876	6C	sync_CCIR_00	0	00	00000000	RW	5	0	
877	6D	sync_CCIR_80	128	80	10000000	RW	5	0	
878	6E	sync_CCIR_10	16	10	00010000	RW	5	0	
879	6F	ccir656enc_ctrl1	144	90	10010000	RW	5	0	Ccir656 control for encoder
880	70	xscale_th_h	2	02	00000010	RW	5	0	Xscale horizontal scaling TH for encoder
881	71	xscale_th_l	128	80	10000000	RW	5	0	
882	72	Reserved							
883	73	flicker_control1	u	u	uuuuuuuu	RW	5	0	Flicker control
884	74	auto_fd	0	00	00000000	RW	5	0	Auto flicker detection enable monitoring
885	75	fd_a_step_h	u	u	uuuuuuuu	RW	5	0	Flicker detection step for A state
886	76	fd_a_step_l	u	u	uuuuuuuu	RW	5	0	
887	77	fd_b_step_h	3	03	00000011	RW	5	0	Flicker detection step for B state
888	78	fd_b_step_l	u	u	uuuuuuuu	RW	5	0	
889	79	fd_winheight	64	40	01000000	RW	5	0	Flicker detection window height
890	7A	fd_a_delay	0	00	00000000	RW	5	0	Flicker detection delay for A state
891	7B	fd_b_delay	0	00	00000000	RW	5	0	Flicker detection delay for A state
892	7C	fd_th	16	10	00010000	RW	5	0	Flicker detection TH.
893	7D	fd_period_a_h	u	u	uuuuuuuu	RW	5	0	Flicker period for A state
894	7E	fd_period_a_m	u	u	uuuuuuuu	RW	5	0	
895	7F	fd_period_a_l	u	u	uuuuuuuu	RW	5	0	
896	80	fd_period_b_h	1	01	00000001	RW	5	0	Flicker period for B state
897	81	fd_period_b_m	u	u	uuuuuuuu	RW	5	0	
898	82	fd_period_b_l	u	u	uuuuuuuu	RW	5	0	
899	83	fd_period_c_h	u	u	uuuuuuuu	RW	5	0	Flicker period for 1/20 second

(Group D – continued)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
900	84	fd_period_c_m	u	u	uuuuuuuu	RW	5	0	Flicker period for 1/20 second
901	85	fd_minfr	4	04	00000100	RW	5	0	Flicker TH. for 1/20 second
902	86	led_control1	0	00	00000000	RW	5	0	Led control
903	87	led_control2	0	00	00000000	RW	5	0	
904	88	led_lvth1	0	00	00000000	RW	5	0	Led control level th.1
905	89	led_lvth2	0	00	00000000	RW	5	0	Led control level th.2
906	8A	led_frame	128	80	10000000	RW	5	0	led frame control
907	8B	mirs_pw	100	64	01100100	RW	5	0	Mirs pulse width
908	8C	Reserved							
909	8D	periedge_gain	0	00	00000000	RW	5	0	Peripheral edge gain
910	8E	periedge_x	0	00	00000000	RW	5	0	Peripheral edge center control
911	8F	periedge_y	0	00	00000000	RW	5	0	
912	90	periedge_scalex	81	51	01010001	RW	5	0	Peripheral edge scale control
913	91	periedge_scaley	81	51	01010001	RW	5	0	
914	92	spi_addr_update	0	00	00000000	RW	5	0	Spi address update control
915	93	Reserved							
916	94	y_min	0	00	00000000	RW	5	0	Control register for Output Y min
917	95	Reserved							
918	96	dark_ec_pth0	4	04	00000100	RW	5	0	Dark edge clamp plus threshold filter control
919	97	dark_ec_pth1	4	04	00000100	RW	5	0	
920	98	dark_ec_pth2	4	04	00000100	RW	5	0	
921	99	dark_ec_pth	4	04	00000100	RW	6	aev	
922	9A	dark_ec_mth0	4	04	00000100	RW	5	0	Dark edge clamp minus threshold filter control
923	9B	dark_ec_mth1	4	04	00000100	RW	5	0	
924	9C	dark_ec_mth2	4	04	00000100	RW	5	0	
925	9D	dark_ec_mth	4	04	00000100	RW	6	aev	
926	9E	dark_ec_pmax0	128	80	10000000	RW	5	0	Dark edge clamp plus max filter control
927	9F	dark_ec_pmax1	128	80	10000000	RW	5	0	
928	A0	dark_ec_pmax2	128	80	10000000	RW	5	0	
929	A1	dark_ec_pmax	128	80	10000000	RW	6	aev	
930	A2	dark_ec_mmax0	128	80	10000000	RW	5	0	Dark edge clamp minus max filter control
931	A3	dark_ec_mmax1	128	80	10000000	RW	5	0	
932	A4	dark_ec_mmax2	128	80	10000000	RW	5	0	
933	A5	dark_ec_mmax	128	80	10000000	RW	6	aev	
934	A6	spi_baud_rate	13	0D	00001101	RW	5	0	Spi baud rate
935	A7	osd_opac	16	10	00010000	RW	5	0	OSD transparency control
936	A8	spi_osd_control	u	u	uuuuuuuu	RW	5	0	[1]: OSD boundary, [0]: OSD enable
937	A9	spi_saddr_h	0	00	00000000	RW	5	0	OSD rom data read start address (SPI Flash ROM)
938	AA	spi_saddr_m	0	00	00000000	RW	5	0	
939	AB	spi_saddr_l	0	00	00000000	RW	5	0	
940	AC	spi_paddr_h	0	00	00000000	RW	5	0	OSD rom data read stop address (SPI Flash ROM)
941	AD	spi_paddr_m	0	00	00000000	RW	5	0	
942	AE	spi_paddr_l	0	00	00000000	RW	5	0	
943	AF	palette_1_y	144	90	10010000	RW	5	0	Palette 1 Color
944	B0	palette_1_cb	53	35	00110101	RW	5	0	
945	B1	palette_1_cr	34	22	00100010	RW	5	0	
946	B2	palette_2_y	210	D2	11010010	RW	5	0	Palette 2 Color
947	B3	palette_2_cb	16	10	00010000	RW	5	0	
948	B4	palette_2_cr	146	92	10010010	RW	5	0	

(Group D – continued)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
949	B5	palette_3_y	81	51	01010001	RW	5	0	Palette 3 Color
950	B6	palette_3_cb	90	5A	01011010	RW	5	0	
951	B7	palette_3_cr	240	F0	11110000	RW	5	0	
952	B8	palette_4_y	235	EB	11101011	RW	5	0	Palette 4 Color
953	B9	palette_4_cb	128	80	10000000	RW	5	0	
954	BA	palette_4_cr	128	80	10000000	RW	5	0	
955	BB	palette_5_y	106	6A	01101010	RW	5	0	Palette 5 Color
956	BC	palette_5_cb	202	CA	11001010	RW	5	0	
957	BD	palette_5_cr	221	DD	11011101	RW	5	0	
958	BE	palette_6_y	169	A9	10101001	RW	5	0	Palette 6 Color
959	BF	palette_6_cb	165	A5	10100101	RW	5	0	
960	C0	palette_6_cr	16	10	00010000	RW	5	0	
961	C1	palette_7_y	41	29	00101001	RW	5	0	Palette 7 Color
962	C2	palette_7_cb	240	F0	11110000	RW	5	0	
963	C3	palette_7_cr	109	6D	01101101	RW	5	0	
964	C4	palette_8_y	16	10	00010000	RW	5	0	Palette 8 Color (boundary color)
965	C5	palette_8_cb	128	80	10000000	RW	5	0	
966	C6	palette_8_cr	128	80	10000000	RW	5	0	
967	C7	resol_gain	8	08	00001000	RW	5	0	Resolution enhance gain
968	C8	enc_fcnt_genlock	1	01	00000001	RW	5	0	Gen_lock control for encoder block
969	C9	enc_rcnt_genlock_h	0	00	00000000	RW	5	0	
970	CA	enc_rcnt_genlock_l	1	01	00000001	RW	5	0	
971	CB	enc_ccnt_genlock_h	0	00	00000000	RW	5	0	
972	CC	enc_ccnt_genlock_l	3	03	00000011	RW	5	0	
973	CD	enc_control	68	44	01000100	RW	5	0	Encoder control
974	CE	enc_scfreq	u	u	uuuuuuuu	RW	5	0	Subcarrier frequency selection for which TV mode
975	CF	enc_sync	16	10	00010000	RW	5	0	Encoder sync level
976	D0	enc_blankH	0	00	00000000	RW	5	0	Encoder blank level
977	D1	enc_blankL	u	u	uuuuuuuu	RW	5	0	
978	D2	enc_pedestal	u	u	uuuuuuuu	RW	5	0	Encoder pedestal
979	D3	enc_burst	u	u	uuuuuuuu	RW	5	0	Burst amplitude
980	D4	enc_Ygain	u	u	uuuuuuuu	RW	5	0	Y convergence gain from YCbCr to YUV
981	D5	enc_Ugain	u	u	uuuuuuuu	RW	5	0	U convergence gain from YCbCr to YUV
982	D6	enc_Vgain	u	u	uuuuuuuu	RW	5	0	V convergence gain from YCbCr to YUV
983	D7	enc_Yrange_H	3	03	00000011	RW	5	0	max. luminance
984	D8	enc_Yrange_L	32	20	00100000	RW	5	0	
985	D9	enc_Crange_H	1	01	00000001	RW	5	0	Maximum amplitudes of chrominance
986	DA	enc_Crange_L	u	u	uuuuuuuu	RW	5	0	
987	DB	enc_chroma_max_H	3	03	00000011	RW	5	0	Maximum chrominance of composite output
988	DC	enc_chroma_max_L	u	u	uuuuuuuu	RW	5	0	
989	DD	enc_chroma_min_H	0	00	00000000	RW	5	0	Minimum chrominance of composite output
990	DE	enc_chroma_min_L	u	u	uuuuuuuu	RW	5	0	
991	DF	enc_lpyc0	4	04	00000100	RW	5	0	Luminance low-pass filter coefficient
992	E0	enc_lpyc1	19	13	00010011	RW	5	0	
993	E1	enc_lpyc2	19	13	00010011	RW	5	0	
994	E2	enc_lpyc3	146	92	10010010	RW	5	0	
995	E3	enc_lpyc4	228	E4	11100100	RW	5	0	
996	E4	enc_lpys	3	03	00000011	RW	5	0	Signs of luminance low-pass filter coefficients

(Group D – continued)

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▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
997	E5	enc_lpcc0	1	01	00000001	RW	5	0	Chrominance low-pass filter coefficient
998	E6	enc_lpcc1	3	03	00000011	RW	5	0	
999	E7	enc_lpcc2	4	04	00000100	RW	5	0	
1000	E8	enc_lpcc3	3	03	00000011	RW	5	0	
1001	E9	enc_lpcc4	0	00	00000000	RW	5	0	
1002	EA	enc_lpcc5	6	06	00000110	RW	5	0	
1003	EB	enc_lpcc6	15	0F	00001111	RW	5	0	
1004	EC	enc_lpcc7	22	16	00010110	RW	5	0	
1005	ED	enc_lpcc8	22	16	00010110	RW	5	0	
1006	EE	enc_lpcc9	11	0B	00001011	RW	5	0	
1007	EF	enc_lpcc10	15	0F	00001111	RW	5	0	
1008	F0	enc_lpcc11	53	35	00110101	RW	5	0	
1009	F1	enc_lpcc12	99	63	01100011	RW	5	0	
1010	F2	enc_lpcc13	143	8F	10001111	RW	5	0	
1011	F3	enc_lpcc14	174	AE	10101110	RW	5	0	
1012	F4	enc_lpcc15	186	BA	10111010	RW	5	0	
1013	F5	enc_lpcsH	3	03	00000011	RW	5	0	Signs of chrominance
1014	F6	enc_lpcsL	240	F0	11110000	RW	5	0	Low-pass filter coefficients
1015	F7	enc_y_preclamp	0	00	00000000	RW	5	0	Pre-clampping Y into LPF
1016	F8	enc_SCH_offset_T	0	00	00000000	RW	5	0	SCH(subcarrier to horizontal) phase offset
1017	F9	enc_SCH_offset_H	0	00	00000000	RW	5	0	
1018	FA	enc_SCH_offset_M	0	00	00000000	RW	5	0	
1019	FB	enc_SCH_offset_L	0	00	00000000	RW	5	0	
1020	FC	DAC_tp_period	0	00	00000000	RW	5	0	DAC test pattern period
1021	FD	burst_toffset	0	00	00000000	RW	5	0	Burst time +/- offset
1022	FE	dac_clk_control	0	00	00000000	RW	5	0	DAC clock control
1023	FF	resol_th	0	00	00000000	RW	5	0	Resolution enhance threshold

▶ Register Tables – Group E

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1024	00	DeviceID_H	48	30	00110000	RO	0	0	device ID
1025	01	DeviceID_L	48	30	00110000	RO	0	0	
1026	02	RevNumber	0	00	00000000	RO	0	0	revision number
1027	03	bank	4	04	00000100	RW	5	0	Register group selector
1028	04	pg_control	9	09	00001001	RW	6	autov	PG(embedded parking guide line) control
1029	05	pg_yt	127	7F	01111111	RW	6	autov	
1030	06	pg_y1	60	3C	00111100	RW	6	autov	
1031	07	pg_y2	2	02	00000010	RW	6	autov	
1032	08	pg_y3	11	0B	00001011	RW	6	autov	
1033	09	pg_y4	25	19	00011001	RW	6	autov	
1034	0A	pg_y5	44	2C	00101100	RW	6	autov	
1035	0B	pg_y6	66	42	01000010	RW	6	autov	
1036	0C	pg_y7	69	45	01000101	RW	6	autov	
1037	0D	pg_y8	95	5F	01011111	RW	6	autov	
1038	0E	pg_y9	124	7C	01111100	RW	6	autov	
1039	0E	pg_y10	129	81	10000001	RW	6	autov	
1040	10	pg_a	114	72	01110010	RW	6	autov	
1041	11	pg_b	62	3E	00111110	RW	6	autov	
1042	12	pg_c	135	87	10000111	RW	6	autov	
1043	13	pg_d	7	07	00000111	RW	6	autov	
1044	14	pg_e	10	0A	00001010	RW	6	autov	
1045	15	pg_f	21	15	00010101	RW	6	autov	
1046	16	pg_line1	161	A1	10100001	RW	6	autov	
1047	17	pg_line2	38	26	00100110	RW	6	autov	
1048	18	pg_line3	43	2B	00101011	RW	6	autov	
1049	19	pg_line4	79	4F	01001111	RW	6	autov	
1050	1A	pg_line5	82	52	01010010	RW	6	autov	
1051	1B	pg_line6	194	C2	11000010	RW	6	autov	
1052	1C	pg_line7	85	55	01010101	RW	6	autov	
1053	1D	pg_line8	120	78	01111000	RW	6	autov	
1054	1E	pg_line9	228	E4	11100100	RW	6	autov	
1055	1F	pg_line10	126	7E	01111110	RW	6	autov	
1056	20	pg_center_h	1	01	00000001	RW	6	autov	
1057	21	pg_center_l	62	3E	00111110	RW	6	autov	
1058 ~ 1068	22 ~ 2C	Reserved							
1069	2D	md_ymsel	0	00	00000000	RW	5	0	Select region of monitoring ymean in motion block
1070	2E	md_ymean	0	00	00000000	RO		0	Monitoring ymean in motion block
1071	2F	md_fcnt	0	00	00000000	RO			Monitoring frame counter in motion block
1072 ~ 1074	30 ~ 32	Reserved							
1075	33	ledlight_h	0	00	00000000	RW	6	aev	IR led control
1076	34	ledlight_m	0	00	00000000	RW	6	aev	
1077	35	ledlight_l	0	00	00000000	RW	6	aev	

(Group E – continued)

▶ Register Tables – Group E

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1078	36	led_on	0	00	00000000	RW	6	aev	IR led control
1079	37	ledcnt	0	00	00000000	RW	5	0	
1080	38	min_ledlight_h	0	00	00000000	RW	5	0	
1081	39	min_ledlight_m	1	01	00000001	RW	5	0	
1082	3A	max_ledlight_h	3	03	00000011	RW	5	0	
1083	3B	max_ledlight_m	255	FF	11111111	RW	5	0	
1084	3C	led_speed	8	08	00001000	RW	5	0	
1085	3D	led_exposure_t	0	00	00000000	RW	5	0	
1086	3E	led_exposure_h	194	C2	11000010	RW	5	0	
1087	3F	led_exposure_m	160	A0	10100000	RW	5	0	
1088	40	led_exposure_l	0	00	00000000	RW	5	0	
1089	41	led_pp_th	7	07	00000111	RW	5	0	
1090	42	led_pw_h	0	00	00000000	RW	6	aev	
1091	43	led_pw_l	0	00	00000000	RW	6	aev	
1092	44	led_pp_h	3	03	00000011	RW	6	aev	
1093	45	led_pp_l	255	FF	11111111	RW	6	aev	
1094	46	led_mtr	0	00	01001011	RW	6	aev	
1095 ~ 1279	47 ~ FF	Reserved							

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▷ **Chip_mode, Mirror & PAD control**

address bank	address hex	register name	bit#	Bit name	default (h)		Description
A	04	chip_mode	7	x	UU	0	Reserved
			6	x		0	Reserved
			5	x		0	Reserved
			4	x		0	Reserved
			3	x		0	Reserved
			2	x		0	Reserved
			1	chip_mode		U	Chip mode selection 00b - NTSC/ (M)PAL ,01b - PAL , else – VGA
			0			U	*The default value of this register is changed by wire-strapping. After changed wire-strapping, the register can be set with other values through SCL and SDA.
A	05	Mirror	7	x	UU	0	Reserved
			6	x		0	Reserved
			5	x		0	Reserved
			4	x		0	Reserved
			3	x		0	Reserved
			2	x		0	Reserved
			1	vm		U	Vertical mirror ON/OFF
			0	hm		U	Horizontal mirror ON/OFF
A	25	Clock divider	7	x	07	0	Reserved
			6	x		0	Reserved
			5	x		0	Reserved
			4	x		0	Reserved
			3	x		0	Reserved
			2	clkdiv		1	00h = mclk , 01h = mclk x 2/3 02h = mclk x 1/2, 03h= mclk x 1/3 04h = mclk x 1/4, 05h= mclk x 1/8 , else =mclk
			1			1	
			0			1	
A	27	Pad control 1	7	Register stdby	66	0	0 : normal mode, 1: stdby mode,
			6	x		1	Reserved
			5	pad stdby_level		1	Stdby data output pad level selector
			4			0	1xb : hiz, 01b : high, 00b : low
			3	clkoff		0	0b : not kill ,1b : clock Kill
			2	osc_pad_en		1	Osc(x1) pad enable
			1	osc_pad_drv		1	Osc(x1) pad drivability
			0			0	
A	28	Pad control 2	7	pad_drv	00	0	Data & Vsync pad drivability control register
			6			0	
			5	pclk_drv		0	Pclk drivability control
			4			0	
			3	pclk_delay		0	Pclk delay control
			2			0	
			1			0	
			0	x		0	Reserved

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▷ **PAD & Strap controls**

Address bank	Address hex	register name	bit#	Bit name	default (h)		Description
A	29	Pad control 3	7	vsync_pad_en	00	0	0b : disable ,1b : enable
			6	hsync_drv		0	Hsync drivability control
			5			0	
			4	hsync_pad_en		0	0b : disable ,1b : enable
			3	data_pad_en		0	0b : disable ,1b : enable
			2	motion_pad_en		0	0b : disable, 1b : enable
			1	d0 pad select		0	0b : DO0, 1b : motion detection
			0	x		0	Reserved
A	2A	Pad control 4	7	ledctrl_en	00	0	0b : disable ,1b : enable
			6	ledctrl_pad_drv		0	LED pad drivability control
			5			0	
			4	x		0	Reserved
			3	x		0	Reserved
			2			0	
			1			0	
			0			0	
A	2B	Pad control 5	7	spi_pad_en	C0	1	0b : disable ,1b : enable
			6	spi_pad_ie		1	0b : disable ,1b : enable
			5	spi_pad_drv		0	SPI output pad drivability control
			4			0	
			3	geno_pad_en		0	0b : disable ,1b : enable
			2	geno_pad_drv		0	Genlock output pad drivability control
			1			0	
			0	geni_en		0	0b : disable ,1b : enable
A	2C	Pad control 6	7	mirsctrl_en	00	0	MIRS output pad
			6	mirsctrl_pad_drv		0	MIRS output pad drivability control
			5			0	
			4	x		0	Reserved
			3	x		0	
			2	x		0	
			1	x		0	
			0	x		0	
A	2D	Strap_control	7	x	FF	1	Reserved
			6	IIC Strap master		1	1b:control when reset='0' ,0b : control in real-time
			5	OSD		1	1b:control when reset='0' ,0b : control in real-time
			4	Strap in/out door		1	1b:control when reset='0' ,0b : control in real-time
			3	Strap BLC		1	1b:control when reset='0' ,0b : control in real-time
			2	Strap flicker		1	1b:control when reset='0' ,0b : control in real-time
			1	Strap TV mode		1	1b:control when reset='0' ,0b : control in real-time
			0	Strap Mirror		1	1b:control when reset='0' ,0b : control in real-time

▷ **Bayer control**

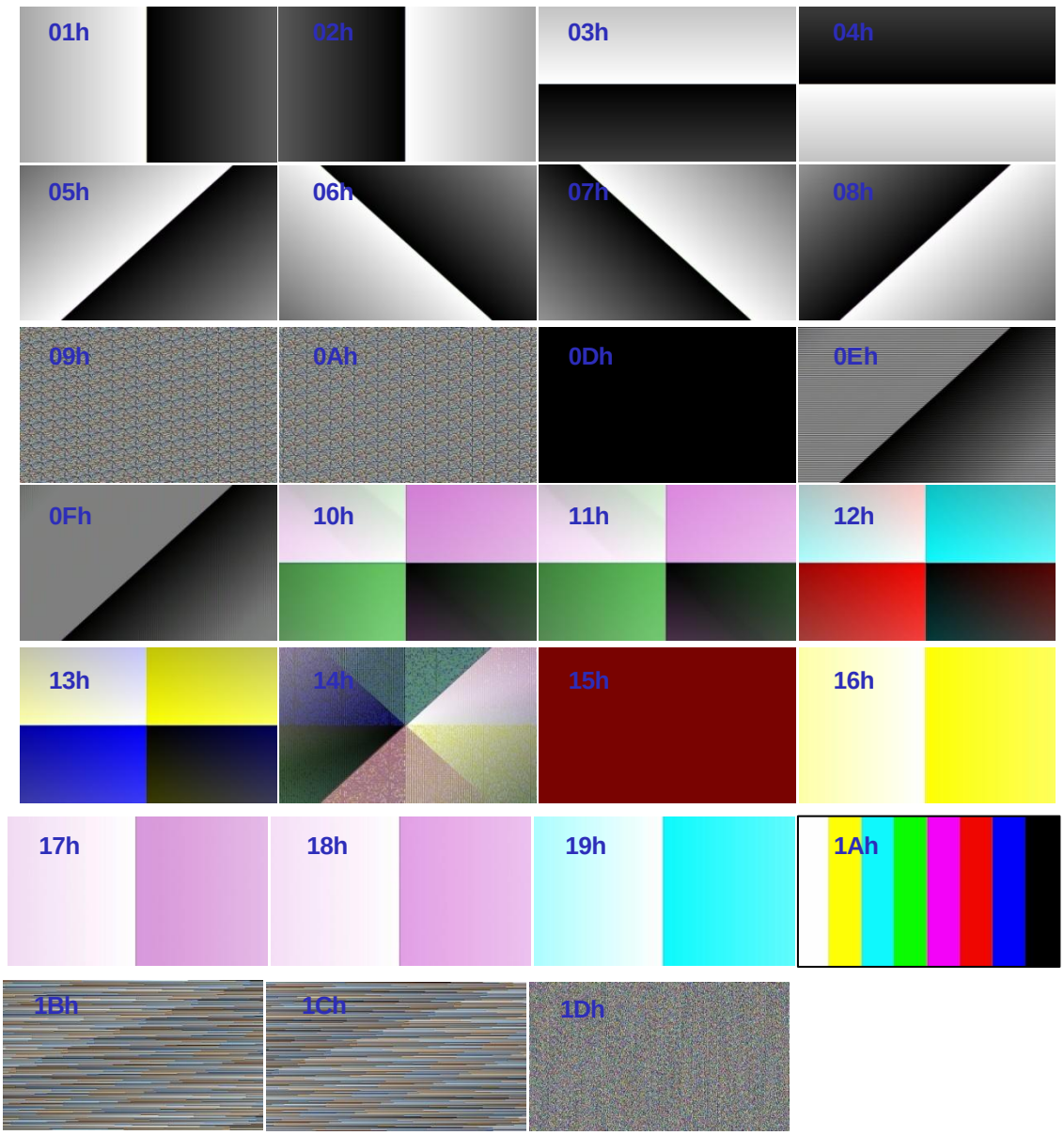
Address bank	Address hex	register name	bit#	Bit name	default (h)		Description
A	49	Bayer control 01	7	x	05	0	Reserved
			6	frmvar_en		0	Variable Frame rate mode, 0: disable, 1: enable
			5	genlock_en		0	External Frame Sync EN, 0: disable, 1: enable
			4	genlock_master		0	0b : slave , 1b : master
			3	x		0	Reserved
			2			1	
			1	x		0	Reserved
			0			1	

▷ **ISP Function control**

Address bank	Address hex	register name	bit#	Bit name	default (h)		Description
B	6	ISP Function control 2	7	reverse	00	0	Image reverse, 0b : disable, 1b : enable
			6	emboss_en		0	Embossing effect , 0b : disable, 1b: enable
			5	emboss_mode		0	Embossing effect mode selection 0b : disable, 1b : enable
			4	sketch_en		0	Sketch effect ,0b : disable, 1b : enable
			3	black&white		0	Black&white , 0b : disable, 1b : enable
			2	md_sleep		0	Motion detection sleep 0b : disable, 1b : enable
			1	md_alarm		0	Motion detection alarm on screen 0b : disable, 1b : enable
			0	md_alarm_mode		0	Motion detection alarm mode selection 0b : disable, 1b : enable
B	9	ISP Function control 5	7	peri-edge_en	00	0	Peripheral edge enhance ,0b: disable, 1b : enable
			6	yrange		0	0 b: 0~255 , 1b : 16~235
			5	x		0	Reserved
			4	x		0	Reserved
			3	x		0	Reserved
			2	x		0	Reserved
			1	x		0	Reserved
			0			0	

▷ **Test Pattern Control**

Address bank	Address hex	register name	bit#	Bit name	default (h)		Description
B	0A	tp_control_0	7	X	00	0	TEST Pattern control
			6			0	
			5			0	
			4			0	
			3			0	
			2			0	
			1			0	
			0			0	



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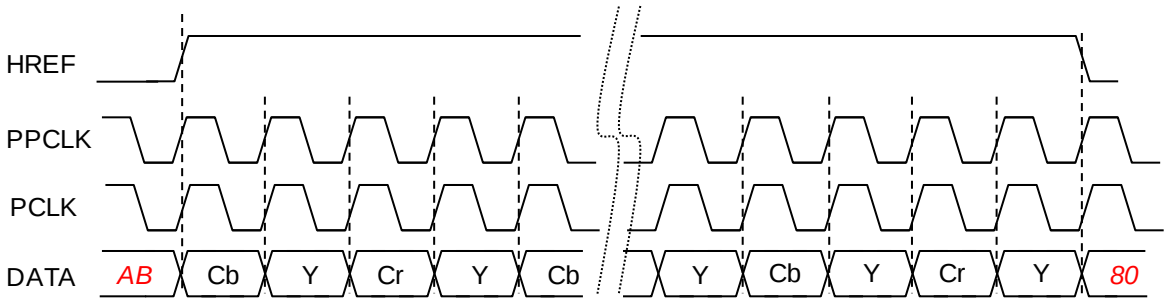
▷ Format Control

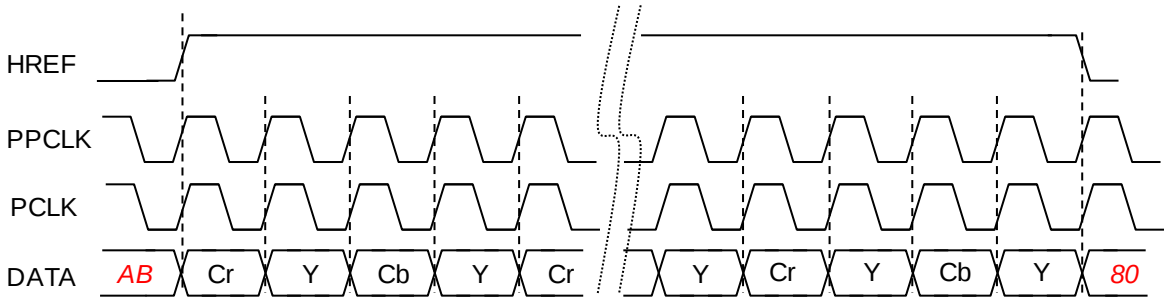
Address bank	Address hex	register name	bit#	Bit name	default (h)		Description
B	29	Format Control	7	X	00	0	00h : cbycry 01h : crycby 02h : ycbycr
			6			0	03h : ycrycb 10h : rggb 11h : gbrg
			5			0	12h : grbg 13h : bggr
			4			0	30h : rgb565 31h : rgb565 (byte swap)
			3			0	32h : bgr565 33h : bgr565 (byte swap)
			2			0	36h : rgb444 37h : rgb444 (byte swap)
			1			0	41h : dpc bayer
			0			0	44h : yyyy

▷ Output timing diagrams for format register (1/4)

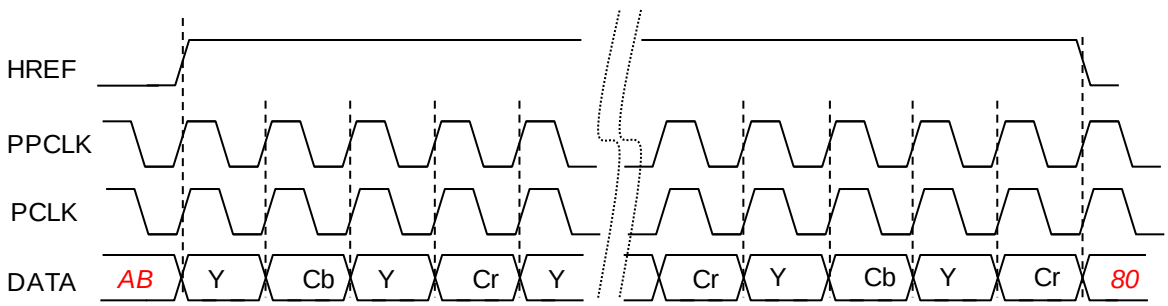
format = 00h (Cb, Y, Cr, Y …),



format = 01h (Cr, Y, Cb, Y, …),

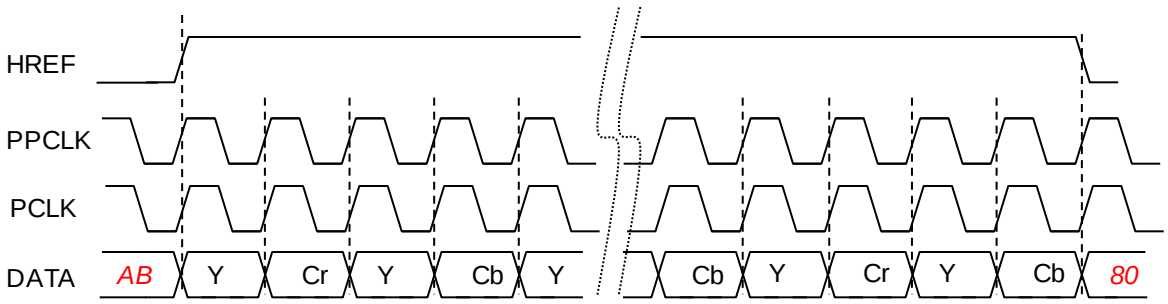


format = 02h (Y, Cb, Y, Cr, …),

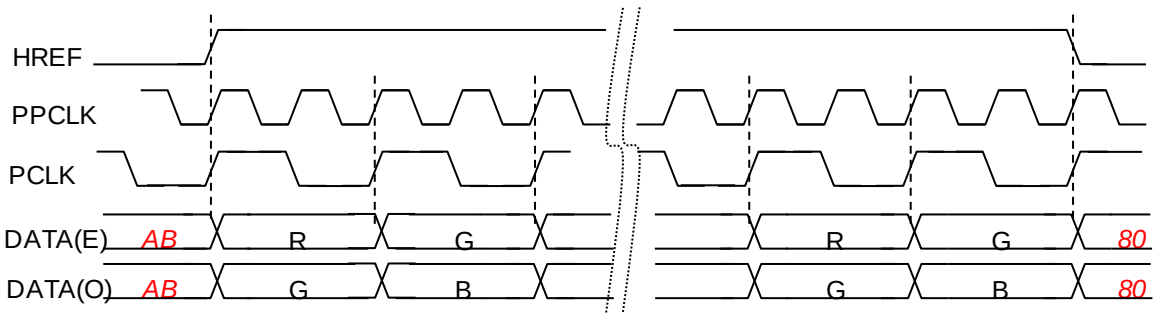


▷ Output timing diagrams for format register (2/4)

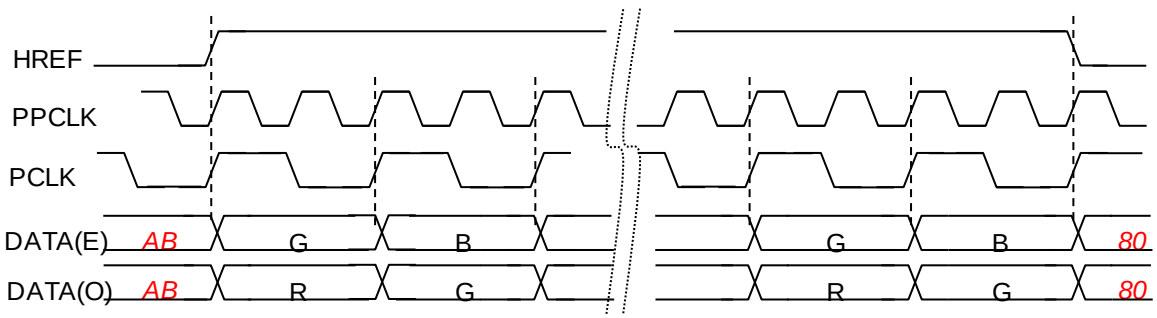
format = 03h (Y, Cr, Y, Cb, …),



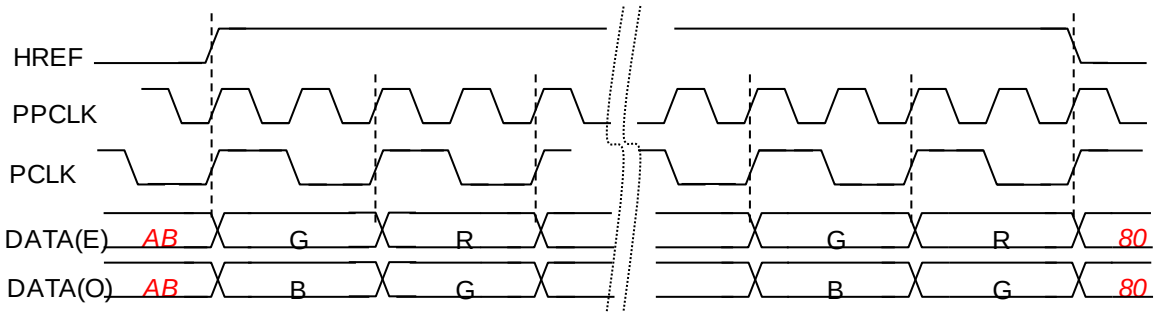
format = 10h (ISP bayer, RGRG, GBGB, …),



format = 11h (ISP bayer, GBGB, RGRG, …),

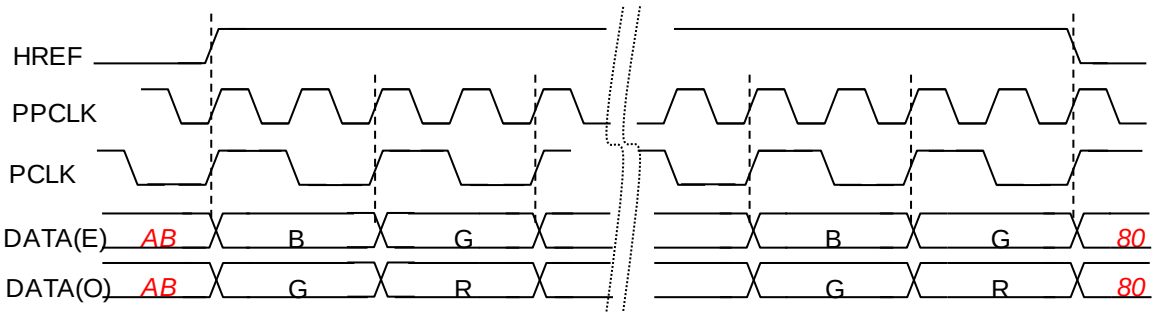


format = is 12h (ISP bayer, GRGR, BGBG, …),

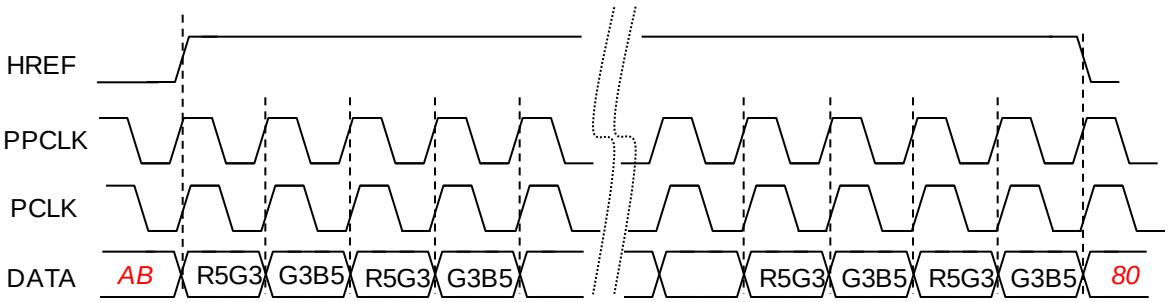


▷ Output timing diagrams for format register (3/4)

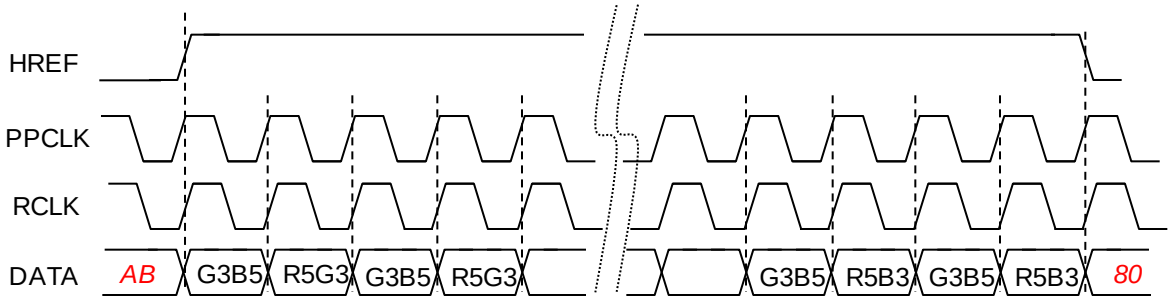
format = 13h (ISP bayer, BGBG, GRGR, …),



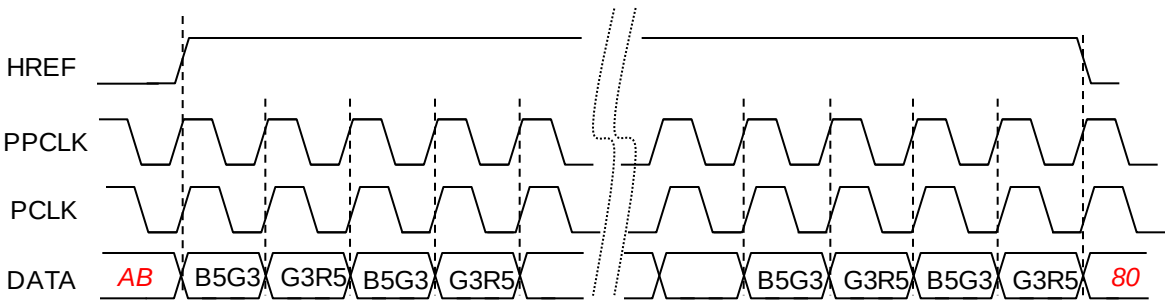
format = 30h(R5G3, G3B5, …),



format = 31h(G3B5, R5B3, …),

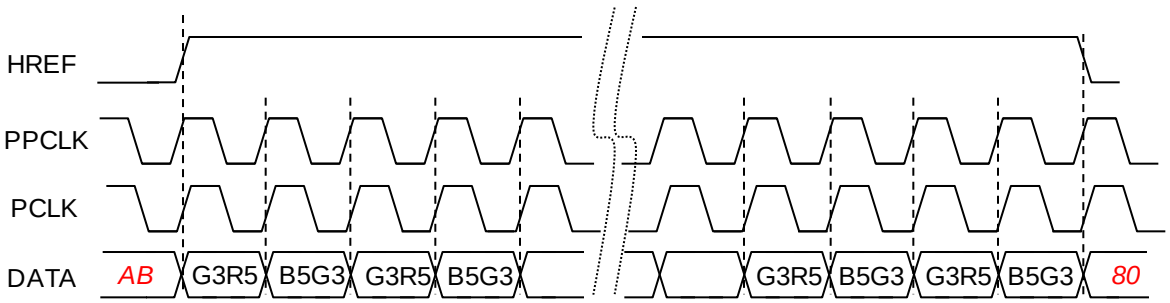


format = 32h(B5G3, G3R5, …),

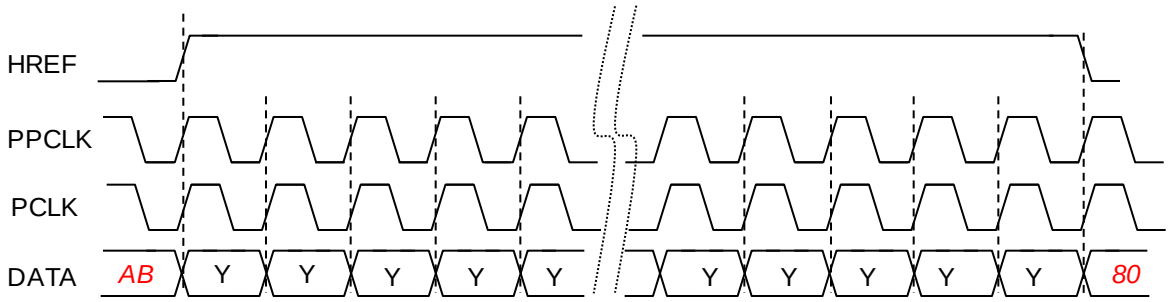


▷ Output timing diagrams for format register (4/4)

format = 33h(G3R5, B5G3, …),



format = 44h(only Y),

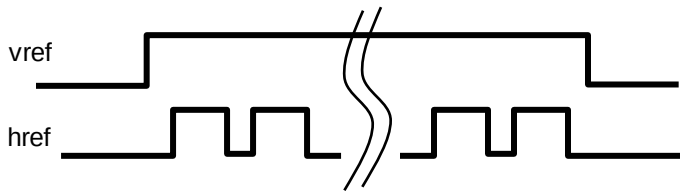


▷ **Sync control 0**

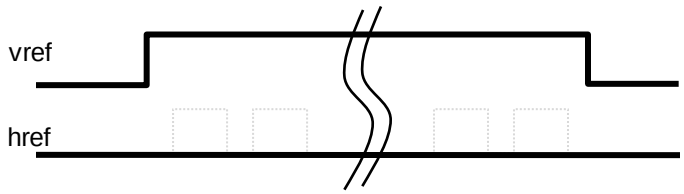
Address		register name	bit#	Bit name	default (h)		Description
bank	hex						
B	9A	Sync Control_0	7	x	80	1	Reserved
			6	sync_drop		0	0 : disable 2 : vsync drop 1 : hsync drop 3 : hsync and vsync drop
			5			0	
			4	sync_pclkrate		0	Pclk rate 0d : ppclk, 1d : ppclk * 1/2 , 2d : ppclk*1/3 3d : ppclk*1/4 ····· 31d : ppclk*/32
			3			0	
			2			0	
			1			0	
			0			0	

▷ **Sync_drop**

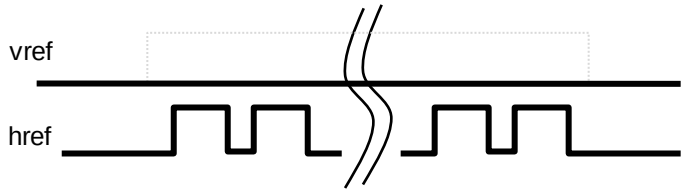
▶ case 1 : sync_drop = “00” (normal)



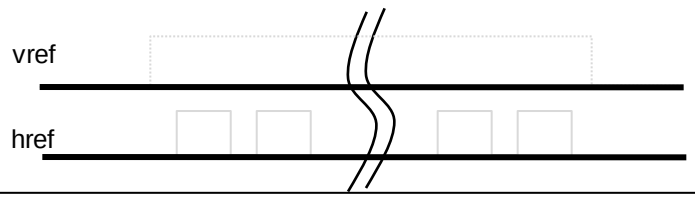
▶ case 2 : sync_drop = “01” (hsync drop)



▶ case 3 : sync_drop = “10” (vsync drop)



▶ case 4 : sync_drop = “11” (hsync & vsync drop)

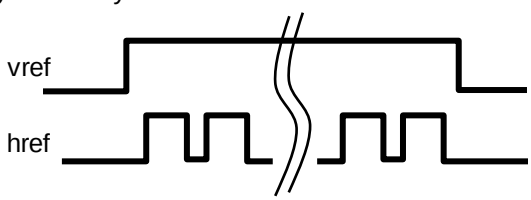


▷ Sync control 1

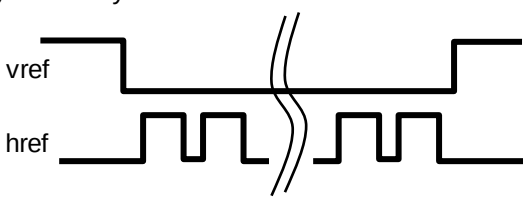
Address bank	Address hex	register name	bit#	Bit name	default (h)		Description
B	9B	Sync Control_1	7	x	00	0	Reserved
			6	sync_vsyncPolarity		0	Vsync polarity change 0: normal, 1 : reverse
			5	sync_hsyncAllLines		0	Hsync output all lines enable(black and active)
			4	sync_hsyncPolarity		0	Hsync polarity change 0: normal, 1: reverse
			3	sync_pclkwindow		0	Pclk window
			2	sync_pclkPolarity		0	Pclk polarity change 0: normal, 1: reverse
			1	bt601		0	Output data 00h/FFh output enable
			0	blkmask		0	Blank period data masking enable

▷ Sync_vsyncpolarity

▶ vsyncPolarity = '0'

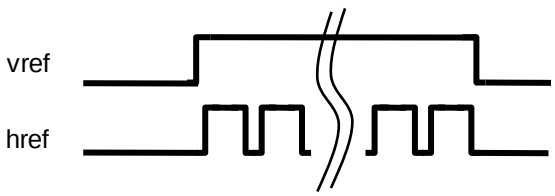


▶ vsyncPolarity = '1'

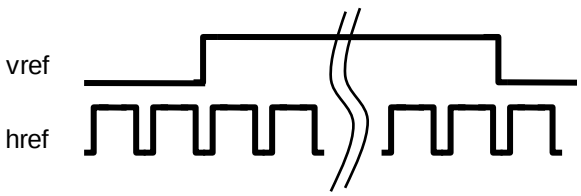


▷ Sync_hsyncAllLines

▶ hsyncAllLines = '0'

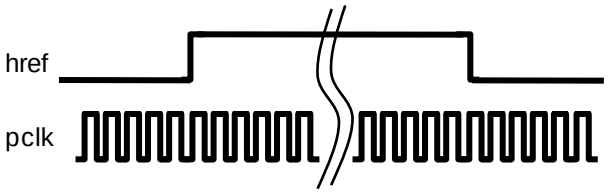


▶ hsyncAllLines = '1'

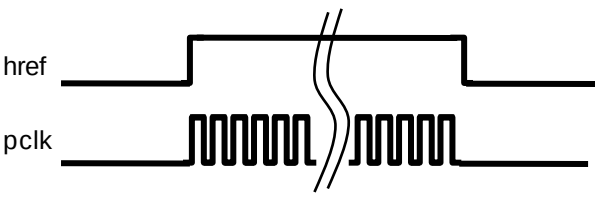


▷ Sync_pclkwindow

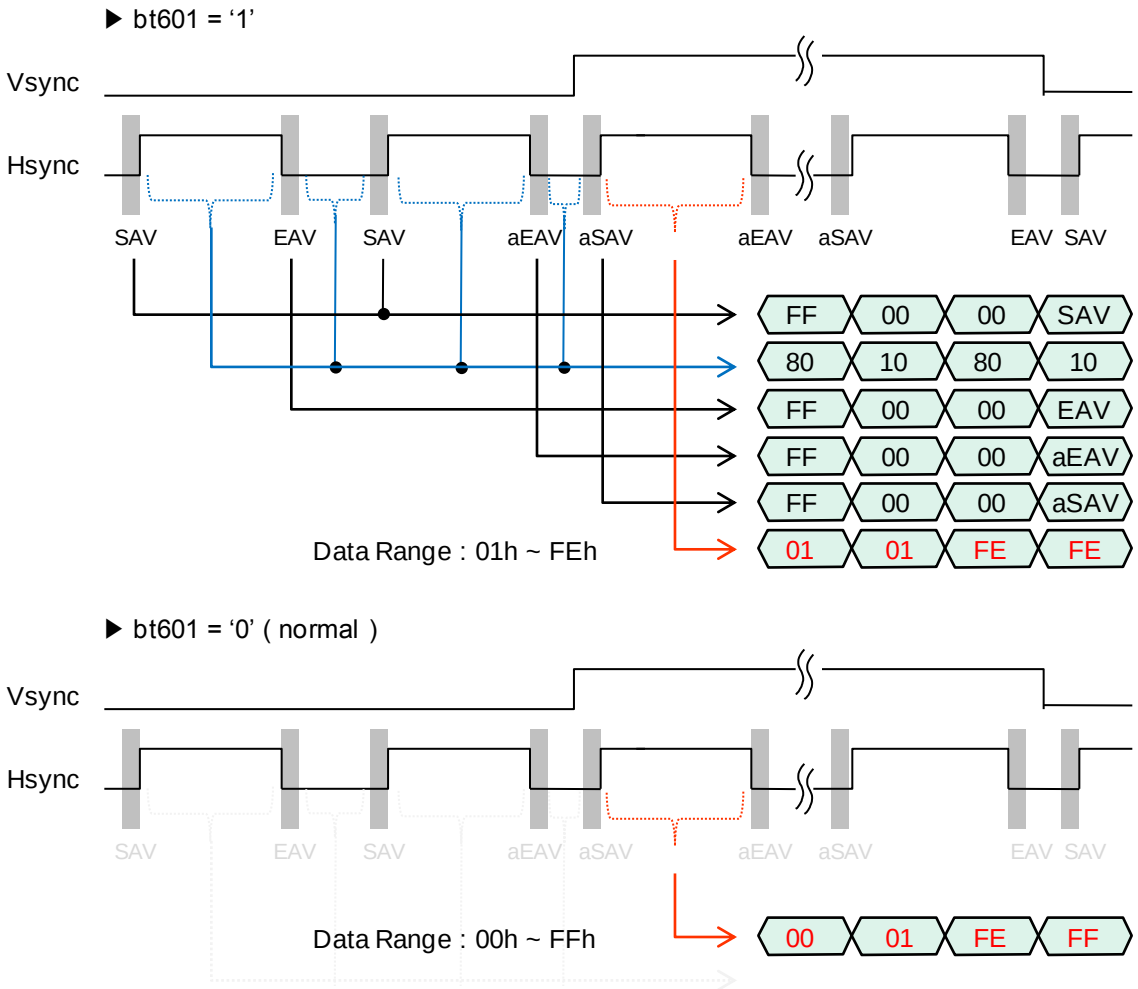
▶ pclkwindow = '0'



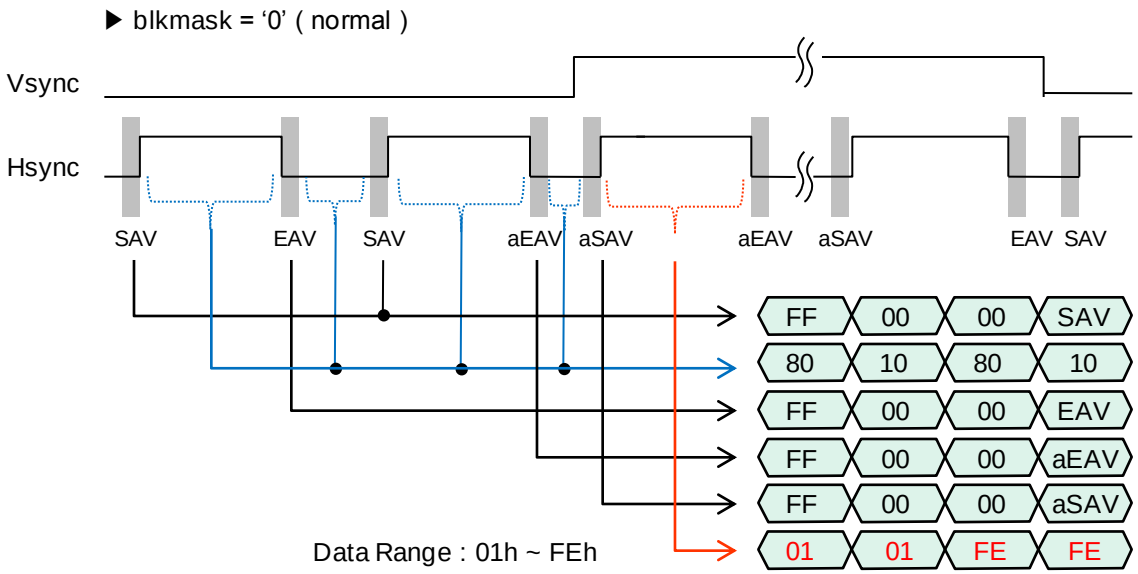
▶ pclkwindow = '1'

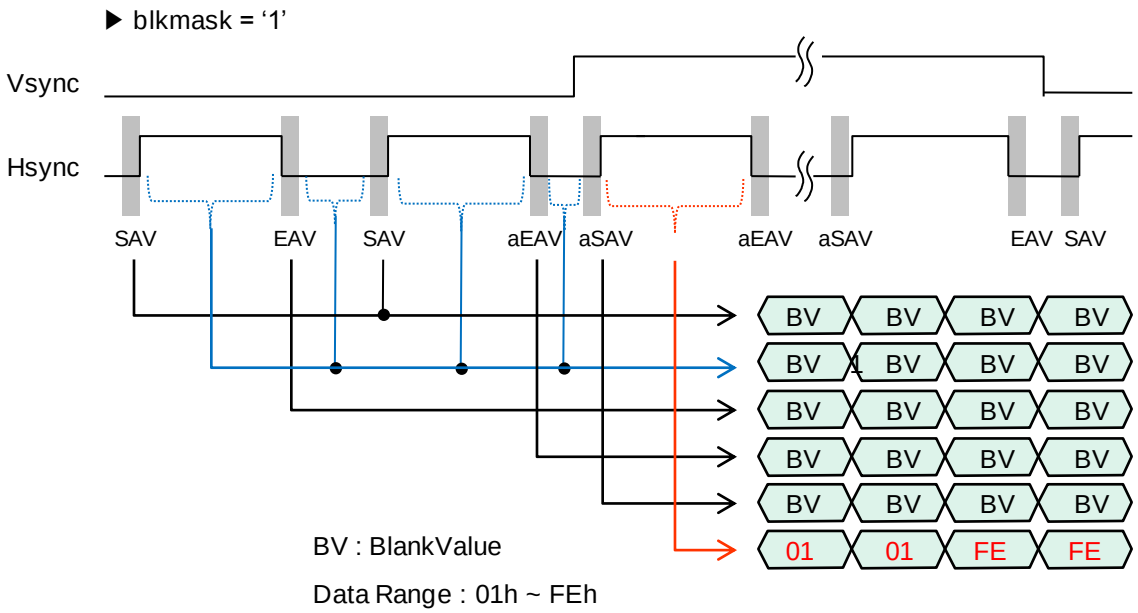


▷ bt601


▶ bt601 = '1'
Vsync
Hsync
SAV
EAV
SAV
aEAV
aSAV
aEAV
aSAV
EAV
SAV
FF 00 00 SAV
80 10 80 10
FF 00 00 EAV
FF 00 00 aEAV
FF 00 00 aSAV
01 01 FE FE
Data Range : 01h ~ FEh
▶ bt601 = '0' (normal)
Vsync
Hsync
SAV
EAV
SAV
aEAV
aSAV
aEAV
aSAV
EAV
SAV
00 01 FE FF
Data Range : 00h ~ FFh

▷ blkmask


▶ blkmask = '0' (normal)
Vsync
Hsync
SAV
EAV
SAV
aEAV
aSAV
aEAV
aSAV
EAV
SAV
FF 00 00 SAV
80 10 80 10
FF 00 00 EAV
FF 00 00 aEAV
FF 00 00 aSAV
01 01 FE FE
Data Range : 01h ~ FEh


▶ blkmask = '1'
Vsync
Hsync
SAV
EAV
SAV
aEAV
aSAV
aEAV
aSAV
EAV
SAV
BV BV BV BV
BV BV BV BV
BV BV BV BV
BV BV BV BV
BV BV BV BV
01 01 FE FE
BV : BlankValue
Data Range : 01h ~ FEh

▷ **Sync control 2**

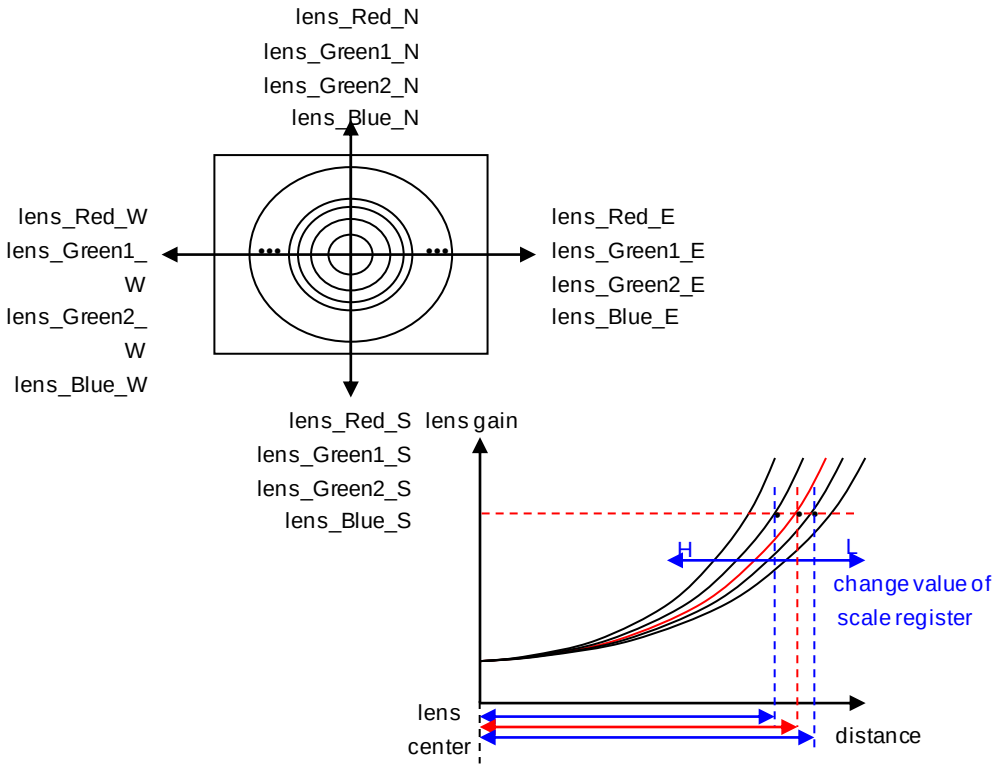
Address		register name	bit#	Bit name	default (h)		Description
bank	hex						
B	9C	Sync Control_2	7	o8bit	80	1	8bit output only mode @ yuv format
			6	x		0	Reserved
			5	mclkphase_en		0	Mclkphase enable
			4	mclkphase		0	Output pclk phase option @ opclk_sel='1'
			3			0	
			2			0	
			1			0	
			0			0	

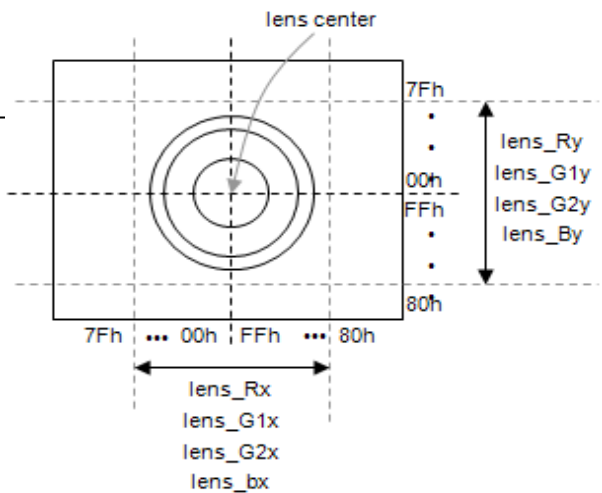
▷ **o8bit**

reg_format	o8bit	motion_pad_en	d1pad	d0pad
DPC bayer	x	0	data[1]	data[0]
others	0	0	data[1]	data[0]
	0	1	data[1]	motion
	1	0	fix(0b)	hiz
	1	1	fix(0b)	motion

▷ Lens shading compensation

Address bank	Address hex	register name	default (h)	Description
B	0C	lens_red_e	51	Lens shading compensation scale control
	0D	lens_red_w	51	
	0E	lens_red_n	51	
	0F	lens_red_s	51	
	10	lens_g1_e	51	
	11	lens_g1_w	51	
	12	lens_g1_n	51	
	13	lens_g1_s	51	
	14	lens_g2_e	51	
	15	lens_g2_w	51	
	16	lens_g2_n	51	
	17	lens_g2_s	51	
	18	lens_blu_e	51	
	19	lens_blu_w	51	
	1A	lens_blu_n	51	
	1B	lens_blu_s	51	
	1C	lens_gainr	00	Lens shading compensation
	1D	lens_gaing1	00	
	1E	lens_gaing2	00	
	1F	lens_gainb	00	
	20	lens_rx	00	Center position control
	21	lens_ry	00	
	22	lens_g1x	00	
	23	lens_g1y	00	
	24	lens_g2x	00	
	25	lens_g2y	00	
	26	lens_bx	00	
	27	lens_by	00	





▷ ***Edge enhancement control***

Address bank	Address hex	register name	default (h)	Description
B	2F	edge_gain	14	Edge gain
	30	ec_pgain	80	Positive max edge clamp gain
	31	ec_mgain	80	Negative max edge clamp gain

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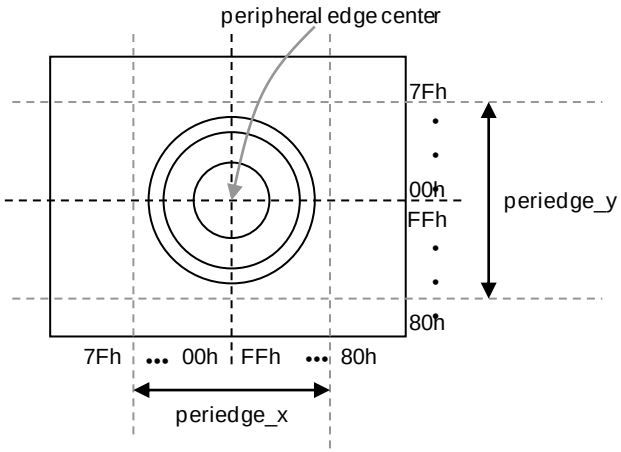
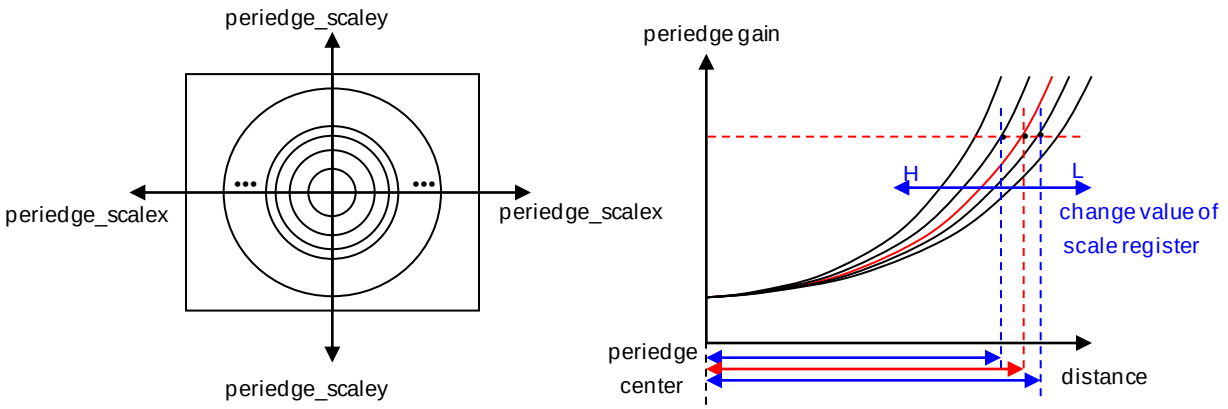
▷ Peripheral edge enhancement

Address bank	Address hex	register name	default (h)	Description
D	8D	periedge_gain	00	Peripheral edge gain ▷When we use a wide-angle lens , you know that peripheral edge become blurred. By using the periedge_gain, peripheral edges are enhanced.
	8E	periedge_x	00	Peripheral edge center control
	8F	periedge_y	00	
	90	periedge_scalex	51	Peripheral edge scale control
	91	periedge_scaley	51	

▷ peripheral edge center control



▷ peripheral edge scale

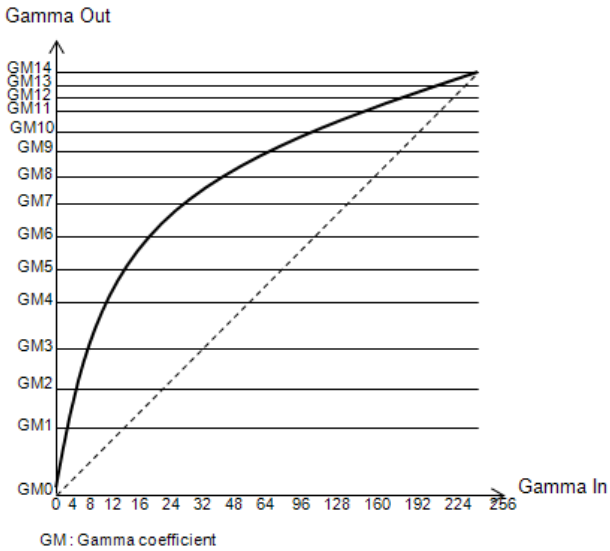
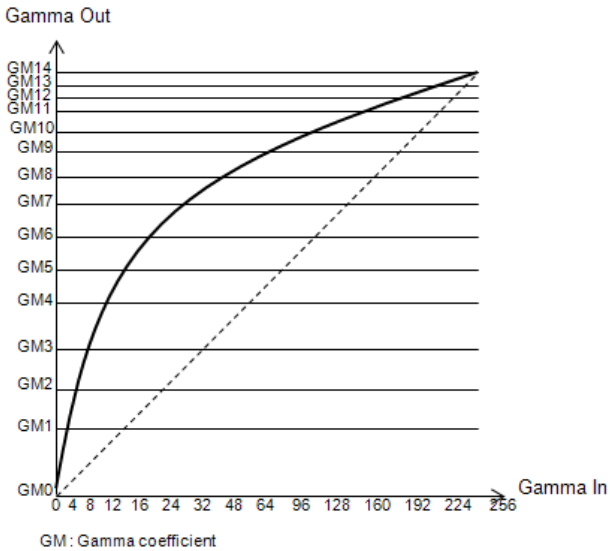


▷ **Color correction matrix**

Address		register	default	Description
bank	hex	name	(h)	
B	33	ccr_m11	33	Color correction matrix value
	34	ccr_m12	8B	
	35	ccr_m13	88	
	36	ccr_m21	86	
	37	ccr_m22	31	
	38	ccr_m23	8A	
	39	ccr_m31	83	
	3A	ccr_m32	8F	
	3B	ccr_m33	32	

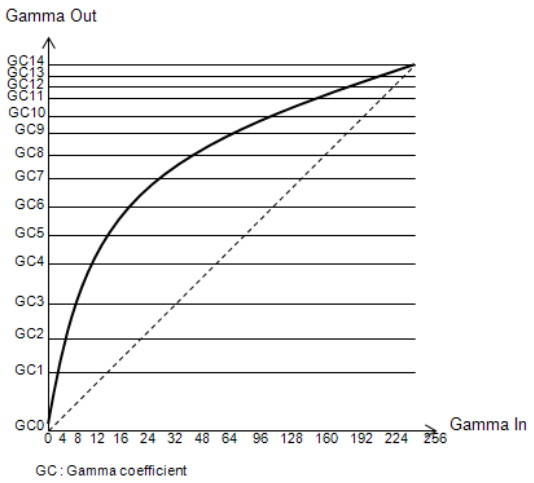
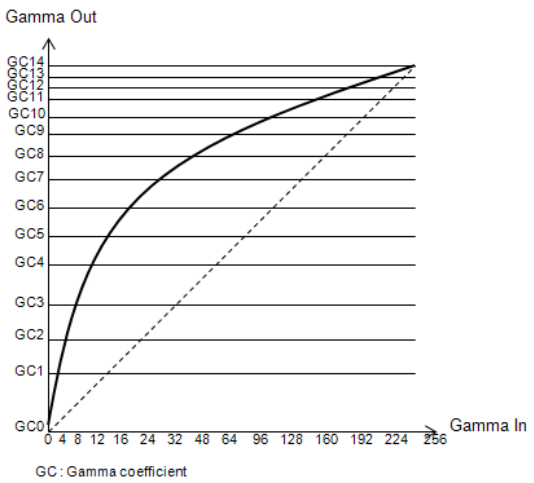
$$\begin{pmatrix} R' \\ G' \\ B' \end{pmatrix} = \begin{pmatrix} ccr\_m11 & ccr\_m12 & ccr\_m13 \\ ccr\_m21 & ccr\_m22 & ccr\_m23 \\ ccr\_m31 & ccr\_m32 & ccr\_m33 \end{pmatrix} \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

▷ ***Y signal Gamma correction***

Address		register name	default (h)	Description
bank	hex			
B	3D	ygm1_y0	00	Y gamma1 coefficient 
	3E	ygm1_y1	03	
	3F	ygm1_y2	0C	
	40	ygm1_y3	19	
	41	ygm1_y4	26	
	42	ygm1_y5	3F	
	43	ygm1_y6	52	
	44	ygm1_y7	6E	
	45	ygm1_y8	82	
	46	ygm1_y9	A1	
	47	ygm1_y10	B9	
	48	ygm1_y11	CE	
	49	ygm1_y12	E0	
	4A	ygm1_y13	F0	
	4B	ygm1_y14	FF	
	4C	ygm2_y0	00	Y gamma2 coefficient 
	4D	ygm2_y1	0B	
	4E	ygm2_y2	17	
	4F	ygm2_y3	22	
	50	ygm2_y4	2E	
	51	ygm2_y5	40	
	52	ygm2_y6	50	
	53	ygm2_y7	6E	
	54	ygm2_y8	88	
	55	ygm2_y9	AE	
	56	ygm2_y10	CA	
	57	ygm2_y11	DC	
	58	ygm2_y12	EC	
	59	ygm2_y13	F6	
	5A	ygm2_y14	FF	

→Difference of Y Gamma1 and Y Gamma2 was selected by exposure. When exposure's value is increased , RGB Output data is affected by the Y Gamma2.

▷ ***Gamma correction for RGB***

Address		register name	default (h)	Description
bank	hex			
B	5B	cgm1_y0	00	RGB gamma1 coefficient 
	5C	cgm1_y1	0B	
	5D	cgm1_y2	17	
	5E	cgm1_y3	22	
	5F	cgm1_y4	2E	
	60	cgm1_y5	40	
	61	cgm1_y6	50	
	62	cgm1_y7	6E	
	63	cgm1_y8	88	
	64	cgm1_y9	AE	
	65	cgm1_y10	CA	
	66	cgm1_y11	DC	
	67	cgm1_y12	EC	
	68	cgm1_y13	F6	
	69	cgm1_y14	FF	
	6A	cgm2_y0	00	RGB gamma2 coefficient 
	6B	cgm2_y1	0B	
	6C	cgm2_y2	17	
	6D	cgm2_y3	22	
	6E	cgm2_y4	2E	
	6F	cgm2_y5	40	
	70	cgm2_y6	50	
	71	cgm2_y7	6E	
	72	cgm2_y8	88	
	73	cgm2_y9	AE	
	74	cgm2_y10	CA	
	75	cgm2_y11	DC	
	76	cgm2_y12	EC	
	77	cgm2_y13	F6	
	78	cgm2_y14	FF	

→Difference of RGB Gamma1 and RGB Gamma2 was selected by exposure. When exposure's value is increased , RGB Output data is affected by the RGB Gamma2.

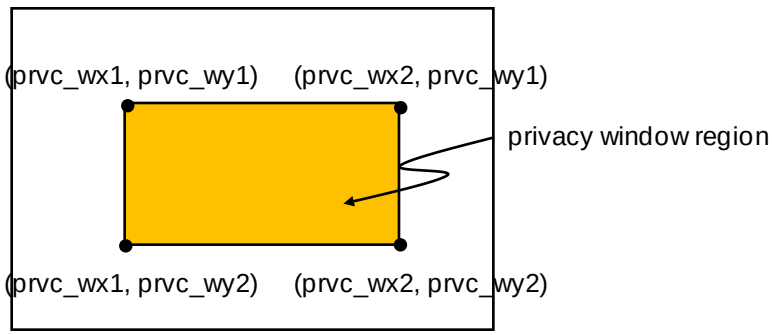
▷ Special Effect control

Address bank	Address hex	register name	default (h)	Description
B	7A	sketch_offset	8C	Sketch offset Sketch offset is applied to chrominance signal which is controlled fro m 0 to 255.
	7B	scale_x	20	Horizontal scale factor, 20h = x1
	7C	scale_y	UU	Vertical scale factor, 20h = x1
	7D	scale_th_h	00	Scale buffer TH : Scale buffer size control register.
	7E	scale_th_l	0A	
	7F	bw_th	80	Black & White output threshold control register. (Special Effect)

▷ ***Color saturation control***

Address bank	Address hex	register name	default (h)	Description
B	80	cs11	25	Color Saturation matrix control register $\begin{bmatrix} Cb' \\ Cr' \end{bmatrix} = \begin{bmatrix} Cs11 & Cs12 \\ Cs21 & Cs22 \end{bmatrix} \begin{bmatrix} Cb \\ Cr \end{bmatrix}$
	81	cs12	00	
	82	cs21	00	
	83	cs22	25	Cb/Cr → CS matrix → Cb'/Cr'
	88	cb_offset	80	Cb color offset control ▶ Cb` = Cb ± reg_cb_offset
	89	cr_offset	80	Cr color offset control ▶ Cr` = Cr ± reg_cr_offset
	8A	c_max	7F	Max. color clamping control register.

▷ ***Privacy window control***

Address		register name	default (h)	Description
bank	hex			
B	A0	prvc_wx1_h	00	Privacy window size control 
	A1	prvc_wx1_l	01	
	A2	prvc_wx2_h	02	
	A3	prvc_wx2_l	80	
	A4	prvc_wy1_h	00	
	A5	prvc_wy1_l	01	
	A6	prvc_wy2_h	00	
	A7	prvc_wy2_l	F0	
	A8	prvc_y	00	* YCbCr of privacy window. User can control the color & Y values of the defined privacy window by controlling these registers .
	A9	prvc_cb	80	
	AA	prvc_cr	80	

▷ **Auto Control**

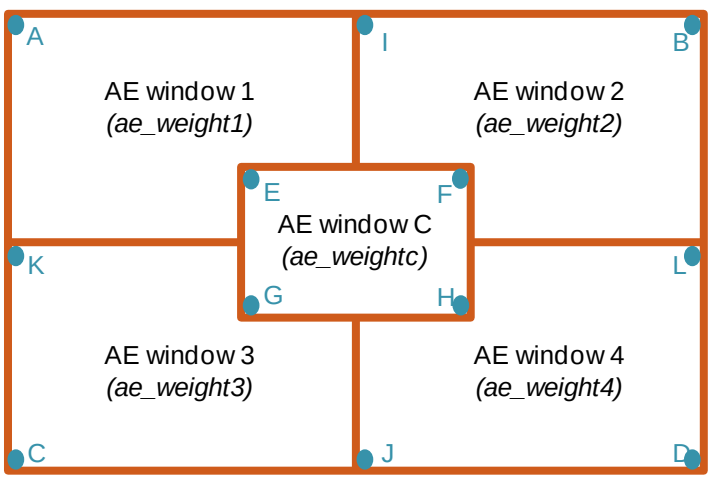
Address bank	Address hex	register name	bit#	Bit name	default (h)		Description
C	4	auto_control_1	7	x	98	1	Reserved
			6	x		0	Reserved
			5	x		0	Reserved
			4	x		1	Reserved
			3	x		1	Reserved
			2	AWB Mode		0	White blance mode selection 0b : auto mode, 1b : manual mode
			1	Exposure Mode		0	Exposure mode selection 00b : auto mode 01b : manual mode (exposure write) 10b : manual mode (ext_inttime, ext_glbgain write) 11b : manual mode (inttime, globalgain write)
			0			0	
C	5	auto_control_2	7	x	65	0	Reserved
			6	LG/CS fitting		1	Lens gain, color saturation fitting 0b : disable 1b : LG & CS fitting enable
			5	min/max YT fitting		1	Minimum & maximum Y target fitting 0b : disable 1b : dynamic minimum/maximum clamping of Y target function enable
			4	x		0	Reserved
			3	x		0	Reserved
			2	x		1	Reserved
			1	x		0	Reserved
			0	x		1	Reserved
C	6	auto_control_3	7	rg/bg ratio fitting	80	1	RG ratio, BG ratio fitting 0b : disable 1b : enable
			6	x		0	Reserved
			5	x		0	Reserved
			4	x		0	Reserved
			3	x		0	Reserved
			2	adcoffst fitting		0	Adcoffset fitting 0b : disable 1b : enable
			1	x		0	Reserved
			0	x		0	Reserved
C	7	auto_control_4	7	dark filter fitting	80	1	Dark filter fitting enable 0b : disable 1b : enable
			6	x		0	Reserved
			5	x		0	Reserved
			4	x		0	Reserved
			3	x		0	Reserved
			2	x		0	Reserved
			1	x		0	Reserved
			0	x		0	Reserved

▷ **Auto Control**

Address bank	Address hex	register name	bit#	Bit name	default (h)		Description
C	8	auto_control_5	7	ec_pth_gsel	00	0	Ec_pth dark filter group selection 0b : group0 1b : group1
			6	ec_mth_gsel		0	Ec_mth dark filter group selection 0b : group0 1b : group1
			5	x		0	Reserved
			4	x		0	Reserved
			3	x		0	Reserved
			2	x		0	Reserved
			1	x		0	Reserved
			0	x		0	Reserved
C	9	auto_control_6	7	ycontrast_gsel	01	0	Ycontrast dark filter group selection 0b : group0 1b : group1
			6	ybrightness_gsel		0	Ybrightness dark filter group selection 0b : group0 1b : group1
			5	x		0	Reserved
			4	x		0	Reserved
			3	*ec_pmax_gsel*		0	Ec_pmax dark filter group selection 0b : group0 1b : group1
			2	*ec_mmax_gsel*		0	Ec_mmax dark filter group selection 0b : group0 1b : group1
			1	x		0	Reserved
			0	x		1	Reserved

▷ Auto Exposure control (1) – AE Window

Address bank	Address hex	register name	default (h)	Description
B	B3	ae_fwx1_h	00	AE full window X start position
	B4	ae_fwx1_l	01	
	B5	ae_fwx2_h	02	AE full window X stop position
	B6	ae_fwx2_l	80	
	B7	ae_fwy1_h	00	AE full window Y start position
	B8	ae_fwy1_l	01	
	B9	ae_fwy2_h	UU	AE full window Y stop position
	BA	ae_fwy2_l	UU	
	BB	ae_cwx1_h	00	AE center window X start position
	BC	ae_cwx1_l	D6	
	BD	ae_cwx2_h	01	AE center window X stop position
	BE	ae_cwx2_l	AB	
	BF	ae_cwy1_h	00	AE center window Y start position
	C0	ae_cwy1_l	UU	
	C1	ae_cwy2_h	00	AE center window Y stop position
	C2	ae_cwy2_l	UU	
	C3	ae_xaxis_h	01	AE window X axis
	C4	ae_xaxis_l	41	
	C5	ae_yaxis_h	00	AE window Y axis
	C6	ae_yaxis_l	UU	



A : *(ae_fwx1, ae_fwy1)*
B : *(ae_fwx2, ae_fwy1)*
C : *(ae_fwx1, ae_fwy2)*
D : *(ae_fwx2, ae_fwy2)*
E : *(ae_cwx1, ae_cwy1)*
F : *(ae_cwx2, ae_cwy1)*
G : *(ae_cwx1, ae_cwy2)*
H : *(ae_cwx2, ae_cwy2)*
I : *(ae_xaxis, ae_fwy1)*
J : *(ae_xaxis, ae_fwy2)*
K : *(ae_fwx1, ae_yaxis)*
L : *(ae_fwx2, ae_yaxis)*

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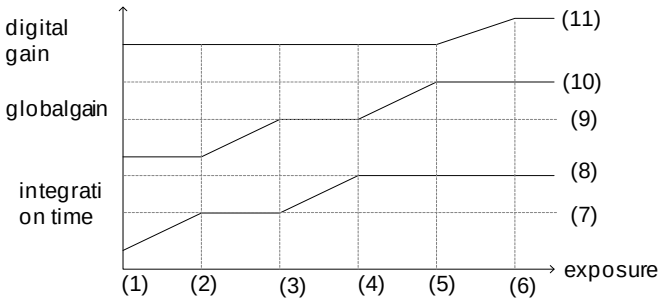
▷ Auto Exposure control (2) - AE Reference

Address bank	Address hex	register name	default (h)	Description
C	10	expfrmh_h	02	** AE Reference ****
	11	expfrmh_l	U	When auto_control_1[1:0] is 00b or 01b, integration time, globalgain and **digitalgain** are calculated by AE reference registers .
	12	midfrmheight_h	02	
	13	midfrmheight_l	U	
	14	maxfrmheight_h	02	
	15	maxfrmheight_l	U	
	16	minexp_h	00	
	17	minexp_m	00	
	18	minexp_l	0C	
	19	midexp_t	01	
	1A	midexp_h	85	
	1B	midexp_m	40	
	1C	maxexp_t	01	
	1D	maxexp_h	85	
	1E	maxexp_m	40	



(1) minimum exposure
(2) frame height for exposure
(3) mid frame height for exposure
(4) max frame height for exposure
(5) mid exposure
(6) max exposure
(7) mid integration time = (2)
(8) max integration time = (4)/(9)
(9) mid globalgain = (3)/(2)
(10) max globalgain =(5)/(8)
(11) max digital gain = (6)/{ (10)*(8) }

▷ Auto Exposure control (3) - in case of External AE

Address bank	Address hex	register name	default (h)	Description
C	20	ext_inttime_h	00	Manual integration time @ external AE mode
	21	ext_inttime_m	80	: When auto_control_1[1:0] is 10b, user can control integration time by writing external integration time registers.
	22	ext_inttime_l	00	Ext_inttime_h & ext_inttime_m : external line integration time. Ext_inttime_l : external column integration time.
	23	ext_glbg_h	01	Manual analog gain @ external AE mode
	24	ext_glbg_l	00	: :When auto_control_1[1:0] is 10b, user can control global gain by these registers.

▷ Auto Exposure control (4) - Manual Exposure

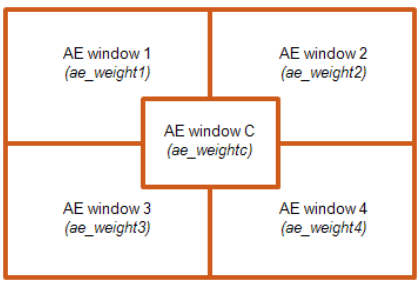
Address bank	Address hex	register name	default (h)	Description
C	25	exposure_t	00	**Exposure control by manual.
	26	exposure_h	00	:When auto_control_1[1:0] is 00b, exposure registers are calculated by auto exposure block. Exposure registers are used in calculating integration time, global gain and digital gain.
	27	exposure_m	40	
	28	exposure_l	00	When auto_control_1[1:0] is 01b, user can write exposure registers. Set auto_control_1[1:0] to 01b, before writing exposure registers.

▷ **Auto Exposure control (5) - Saturation ratio control register**

Address bank	Address hex	register name	default (h)	Description
C	2A	ae_ysat	44	Saturation decision TH for Y data
	2C	sratio_weight	08	Saturation ratio weight factor
	2D	sratio	00	Saturation ratio value for monitoring. $SR\_c/p = \frac{(\#\text{ of saturation pixel in AE window})\_c/p}{(\#\text{ of pixel in AE window})\_c/p}$ $sratio = \frac{(SR\_c \times sratio\_weight) + (SR\_p \times (16 - sratio\_weight))}{16}$

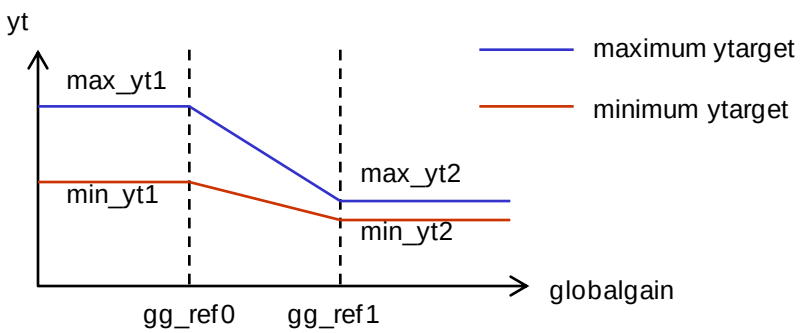
▷ **Auto Exposure control (6) - AE weight for back light compensation.**

Address bank	Address hex	register name	default (h)	Description
C	2E	ae_weight1	08	AE weight peripheral
	2F	ae_weight2	08	
	30	ae_weight3	08	
	31	ae_weight4	08	
	32	ae_weightc	08	AE weight center



▷ **Auto Exposure control (7) - Min/Max Y target reference**

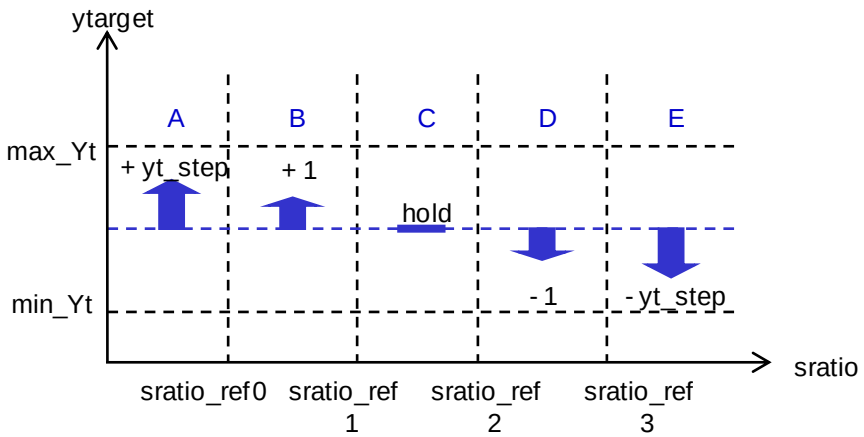
Address bank	Address hex	register name	default (h)	Description
C	39	max_yt1	A0	▷ min/max_yt1/2
	3A	max_yt2	80	User can program dynamic y_target with these registers. Dynamic y_target means that y_target can be changed to match current brightness automatically.
	3B	min_yt1	80	
	3C	min_yt2	50	
	3D	gg_ref0	24	
	3E	gg_ref1	4B	



When auto_control_2[5] is 1b, min./max. y_target is given like graph.

When auto_control_2[5] is 0b, min./max. y_target is given like min_yt1 / max_yt1.

▷ **Auto Exposure control (8) - Y target reference & Y target**

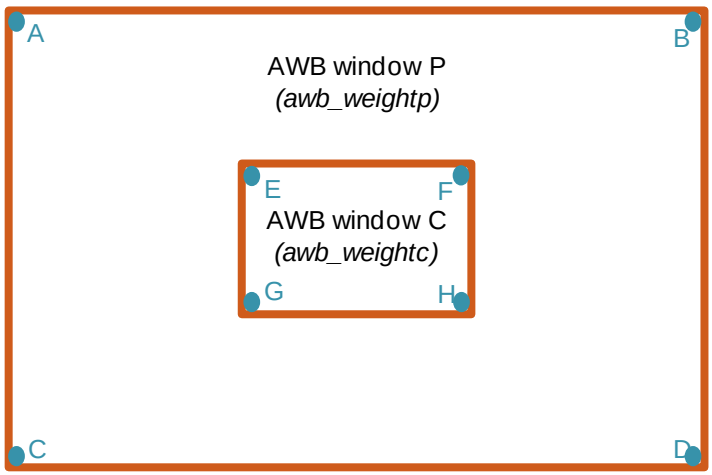
Address bank	Address hex	register name	default (h)	Description
C	3F	sratio_ref0	04	Ytarget control reference ▷ sratio_ref0/1/2/3 Saturation ratio reference fitting registers for y_target control.
	40	sratio_ref1	10	
	41	sratio_ref2	1A	
	42	sratio_ref3	32	
	43	yt_step	04	▷ yt_step Y target step control register. 
	44	ytarget	70	Y target
	45	user_wyt	80	User weight Y target : Final Ytarget is given as Ytarget = (ytarget x user_wyt) / 128d

▷ **Auto Exposure control (9) - AE Speed & AE lock range**

Address bank	Address hex	register name	default (h)	Description
C	46	ae_up_speed	08	AE speed -ae_up_speed : AE up speed control . -ae_down_speed : AE down speed control . : yt ≥ ym : AE_speed = ae_up_speed yt < ym : AE_speed = ae_down_speed
	47	ae_down_speed	08	
	48	ae_lock	10	AE lock range :(lock ratio = | Ymean - Ytarget | / Ytarget)
	49	auto_flag	00	Auto flag :Current AE state indicator. If auto_flag[0] = '0b' , then AE state is "not hold" If auto_flag[0] = '1b' , then AE state is "hold"

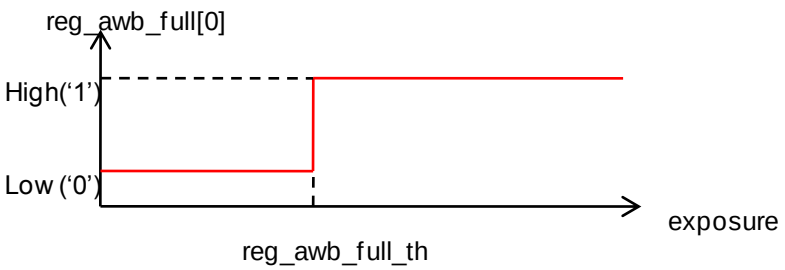
▷ ***Auto White balance control (1) – AWB window***

Address bank	Address hex	register name	default (h)	Description
B	C7	awb_fwx1_h	00	AWB full window X start position
	C8	awb_fwx1_l	01	
	C9	awb_fwx2_h	02	AWB full window X stop position
	CA	awb_fwx2_l	80	
	CB	awb_fwy1_h	00	AWB full window Y start position
	CC	awb_fwy1_l	01	
	CD	awb_fwy2_h	UU	AWB full window Y stop position
	CE	awb_fwy2_l	UU	
	CF	awb_cwx1_h	00	AWB center window X start position
	D0	awb_cwx1_l	D6	
	D1	awb_cwx2_h	01	AWB center window X stop position
	D2	awb_cwx2_l	AB	
	D3	awb_cwy1_h	00	AWB center window Y start position
	D4	awb_cwy1_l	UU	
	D5	awb_cwy2_h	00	AWB center window Y stop position
	D6	awb_cwy2_l	UU	

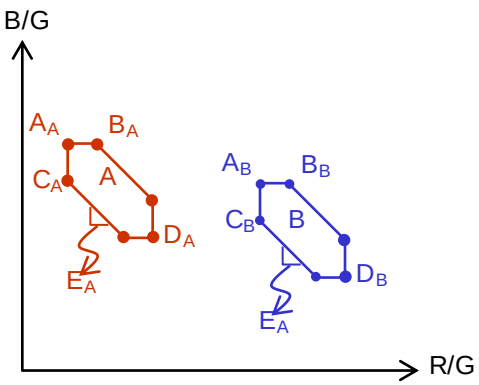


A : *(awb_fwx1, awb_fwy1)*
B : *(awb_fwx2, awb_fwy1)*
C : *(awb_fwx1, awb_fwy2)*
D : *(awb_fwx2, awb_fwy2)*
E : *(awb_cwx1, awb_cwy1)*
F : *(awb_cwx2, awb_cwy1)*
G : *(awb_cwx1, awb_cwy2)*
H : *(awb_cwx2, awb_cwy2)*

▷ Auto White balance control (2) – AWB sampling range threshold

Address bank	Address hex	register name	default (h)	Description
C	4C	awb_full_th_t	01	AWB sampling range threshold. When exposure is bigger than awb_full_th, awb_full is set to 01h automatically and all data of AWB window (both center & peripheral) is used for AWB function although user defines the sampling regions (Reg. C-51h~60h). 
	4D	awb_full_th_h	85	
	4E	awb_full_th_m	40	
	4F	awb_full	00	

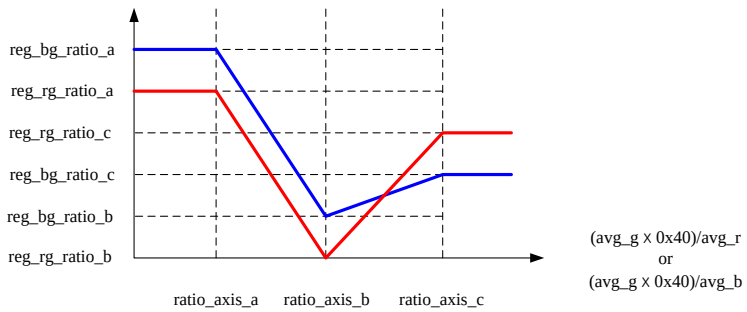
▷ Auto White balance control (3) – AWB sampling control

Address bank	Address hex	register name	default (h)	Description
C	51	awb_p1Ax	29	AWB sampling range selection. :These registers are used for more correct AWB operation.  A_A : (awb_p1Ax, awb_p1Ay) B_A : (awb_p1Ax+awb_osAx, awb_p1Ay) C_A : (awb_p1Ax, awb_p1Ay-awb_osAy) D_A : (awb_p2Ax, awb_p2Ay) E_A : awb_slopeA A_B : (awb_p1Bx, awb_p1By) B_B : (awb_p1Bx+awb_osBx, awb_p1By) C_B : (awb_p1Bx, awb_p1By-awb_osBy) D_B : (awb_p2Bx, awb_p2By) E_B : awb_slopeB If data are not included in region A or region B, then all of data are bad samples and not used AWB operations. In addition, if one of R, G, B is bigger than awb_maxc or lower than awb_minc, then data is bad sample and not used AWB operation.
	52	awb_p1Ay	39	
	53	awb_p2Ax	36	
	54	awb_p2Ay	19	
	55	awb_osAx	09	
	56	awb_osAy	10	
	57	awb_slopeA	A0	
	58	awb_p1Bx	36	
	59	awb_p1By	21	
	5A	awb_p2Bx	69	
	5B	awb_p2By	14	
	5C	awb_osBx	0C	
	5D	awb_osBy	04	
	5E	awb_slopeB	10	
	5F	awb_maxc	FA	
	60	awb_minc	08	

▷ Auto White balance control (4) – AWB weight & AWB weight Speed

Address bank	Address hex	register name	default (h)	Description	
C	61	awb_weight_c	05	AWB weight for center	※caution) awb_weight_c & awb_weight_p should be, awb_weight_c + awb_weight_p = 64d ※R/G/B mean_c/p = [(Sum. of R/G/B data in AWB window)_c/p]/ [(# of pixel in AWB window)_c/p] ※Weighted_R/G/B mean= [(R/G/Bmean_c x ae_weight_c) + (R/G/Bmean_p x ae_weight_p)]/[awb_weight_c + awb_weight_p]
	62	awb_weight_p	0B	AWB weight for peripheral	
	63	awb_wspeed	04	AWB weight speed, Please refer to *awb_control3[6] register*	

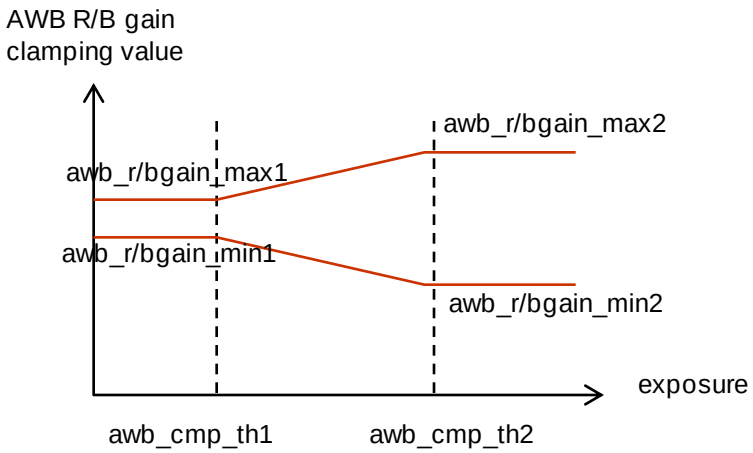
▷ Auto White balance control (5) – Target AWB color ratio.

Address bank	Address hex	register name	default (h)	Description
C	66	rg_ratio_a	7A	Target AWB ratio fitting reference : These registers are used for deciding AWB target. It's possible to enable or disable these registers by controlling auto_control_3[7].  : User can change the value of X-axis by using auto_cotnrol_3[6]. 1b': avg_gx0x40/avg_r, '0b': avg_gx0x40/avg_b *Caution) ratio_axis_a < ratio_axis_b < ratio_axis_c*
	67	bg_ratio_a	78	
	68	rg_ratio_b	80	
	69	bg_ratio_b	80	
	6A	rg_ratio_c	80	
	6B	bg_ratio_c	80	
	6C	ratio_axis_a	2A	
	6D	ratio_axis_b	50	
	6E	ratio_axis_c	57	
	6F	awb_rgratio	80	AWB RG ratio control
	70	awb_bgratio	80	AWB BG ratio control

▷ Auto White balance control (6) – AWB lock range & AWB Speed

Address bank	Address hex	register name	default (h)	Description
C	71	awb_lock	10	AWB lock range
	72	awb_speed	04	AWB speed

▷ ***Auto White balance control (7) – AWB Gain Control***

Address bank	Address hex	register name	default (h)	Description
C	73	awb_rgain_min1	2A	AWB gain clamping fitting control in an Exposure : User can control the minimum or maximum values of AWB in a light intensity by controlling awb_cmp_th1~2 and awb_rgain_min/max1~2.  00h < awb_r/bgain_min1 < awb_r/bgain_max1 < FFh 00h < awb_r/bgain_min2 < awb_r/bgain_max2 < FFh minexp < awb_cmp_th1 < awb_cmp_th2 < maxexp
	74	awb_rgain_min2	28	
	75	awb_rgain_max1	5A	
	76	awb_rgain_max2	5D	
	77	awb_bgain_min1	50	
	78	awb_bgain_min2	4D	
	79	awb_bgain_max1	B7	
	7A	awb_bgain_max2	BA	
	7B	awb_cmp_th1_h	01	
	7C	awb_cmp_th1_m	00	
	7D	awb_cmp_th2_h	02	
	7E	awb_cmp_th2_m	07	

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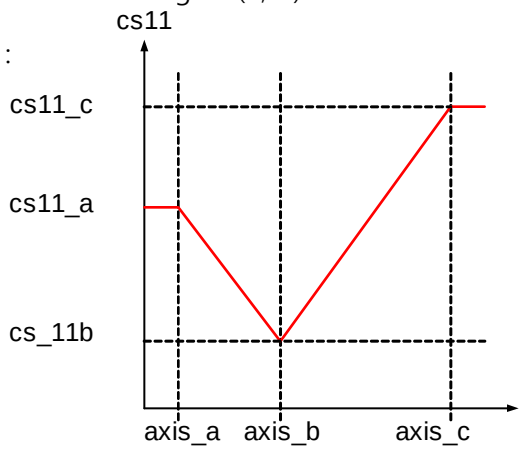
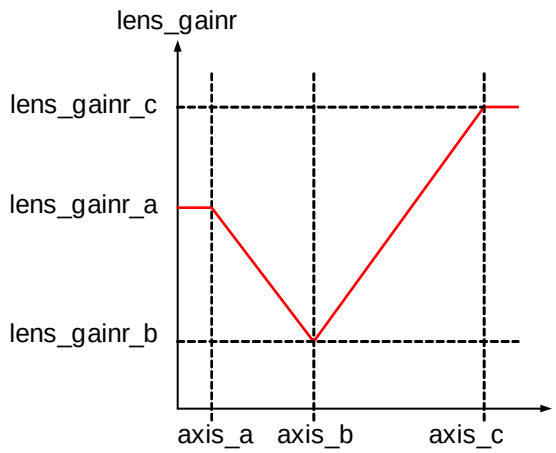
▷ ***Auto White balance control (8) – Lens gain & CS matrix fitting reference***

Address bank	Address hex	register name	default (h)	Description
C	7F	cs11_a	28	Color saturation matrix & Lens Gain fitting reference. :PC3030K provides lens gain (R, B) and CS matrix fitting function which are controlled by user setting. When auto_control_2[6] is '1b', lens gain (R, B) and CS matrix fitting function is enabled. Below diagram shows that how to calculate lens gain (R, B) and CS matrix.
	80	cs12_a	00	
	81	cs21_a	00	
	82	cs22_a	28	
	83	cs11_b	24	
	84	cs12_b	00	
	85	cs21_b	00	
	86	cs22_b	28	
	87	cs11_c	20	
	88	cs12_c	00	
	89	cs21_c	00	
	8A	cs22_c	20	
	8B	lens_gainr_a	02	
	8C	lens_gainb_a	00	
	8D	lens_gainr_b	02	
	8E	lens_gainb_b	00	
	8F	lens_gainr_c	02	
	90	lens_gainb_c	00	
	91	axis_a	2A	
	92	axis_b	50	CS matrix / lens gain fitting reference
	93	axis_c	57	
	94	user_cs	20	User CS gain



* calculation method of cs12, cs21 and cs22 are same as calculation method of cs11.

* bit define of cs11_a/b/c
  [7] : sign
  [6:5] : magnitude of integer
  [4:0] : magnitude of fraction



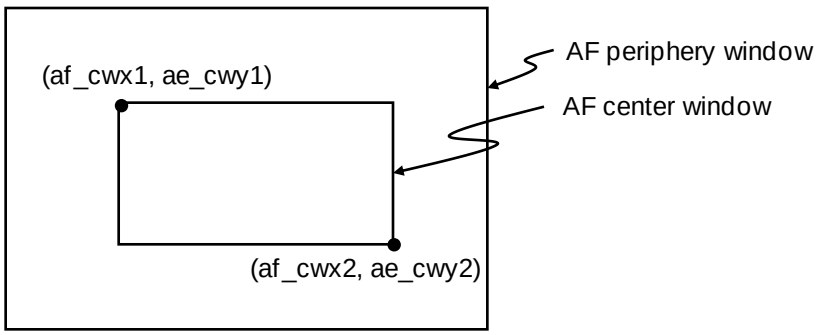
• calculation method of lens_gainb is same as calculation method of lens_gainr.

* bit define of lens_gainr_a/b/c
  [7:5] : magnitude of integer
  [4:0] : magnitude of fraction

▷ **Auto Focus control**

Address bank	Address hex	register name	default (h)	Description
B	D8	af_cwx1_h	00	AF center window X start position
	D9	af_cwx1_l	D6	
	DA	af_cwx2_h	01	AF center window X stop position
	DB	af_cwx2_l	AB	
	DC	af_cwy1_h	00	AF center window Y start position
	DD	af_cwy1_l	U	
	DE	af_cwy2_h	00	AF center window Y stop position
	DF	af_cwy2_l	U	
	E0	af_cweight	08	Control the weight of AF center.
	E1	af_edge_th	00	Control the threshold of AF edge.

▷ **af_cwx1/x2/y1/y2**



▶ AF window can't control AF periphery window.

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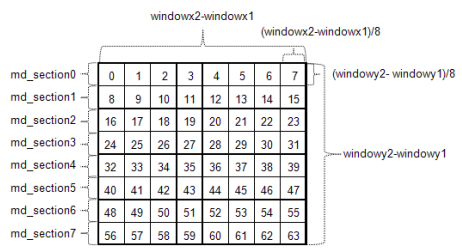
▷ Motion detection (1)

Address bank	Address hex	register name	default (h)	Description	
B	E3	md_yth1	40	Y threshold1 for motion detection	It 's possible to detect the motion using the threshold of Y (luminance) average difference between current and previous frames at the same section.
	E4	md_yth2	40	Y threshold2 for motion detection	
	E5	md_yth3	40	Y threshold3 for motion detection	
	E6	md_yth4	40	Y threshold4 for motion detection	
	E7	md_diff1	40	Difference1 for motion detection	Difference between entire current and previous frame's brightness means.
	E8	md_diff2	40	Difference2 for motion detection	
	E9	md_diff3	40	Difference3 for motion detection	
	EA	md_diff4	40	Difference4 for motion detection	
	EB	md_interval	08	Intervals of frames used for motion detection *md_yth1 md_diff1* | *md_yth2 md_diff2* *md_yth3 md_diff3* | *md_yth4 md_diff4* PC3030K can detect the motion with 4 blocks and it's possible to control the threshold for each block.	

▷ Motion detection (2)

Address bank	Address hex	register name	default (h)	Description
B	EC	md_alarm_y	00	YCbCr for Motion detection alarm. : when the motion is detected , user can control the color & Y value.
	ED	md_alarm_cb	80	
	EE	md_alarm_cr	80	
	EF	md_alarmnumb	04	Number of Motion detection alarm
	F0	md_alarm_xlw	04	X width of motion detection alarm
	F1	md_alarm_ylw	04	Y width of motion detection alarm
	F2	md_alarmdur_h	00	Motion detection alarm speed control.
	F3	md_alarmdur_l	3C	
	F4	md_sleepdur_h	02	Motion detection sleep In case the motion is not detected, user can turn DAC off in this defined time.
	F5	md_sleepdur_l	3A	
	F6	md_section7	00	Image section 7 for motion detection
	F7	md_section6	00	Image section 6 for motion detection
	F8	md_section5	00	Image section 5 for motion detection
	F9	md_section4	00	Image section 4 for motion detection
	FA	md_section3	00	Image section 3 for motion detection
	FB	md_section2	00	Image section 2 for motion detection
	FC	md_section1	00	Image section 1 for motion detection
	FD	md_section0	00	Image section 0 for motion detection

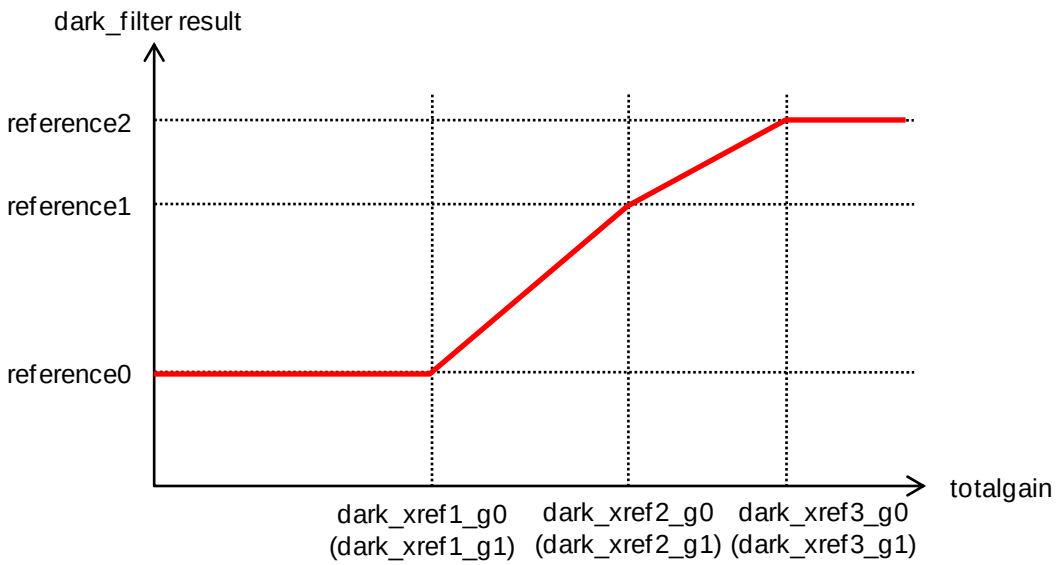


▷ ***Motion detection (3) – Monitoring registers***

<table>
<tr><th colspan="2">Address</th><th>register name</th><th>default (h)</th><th>Description</th></tr>
<tr><th>bank</th><th>hex</th><th></th><th></th><th></th></tr>
<tr><td rowspan="3">E</td><td>2D</td><td>md_ymsel</td><td>00</td><td>Area selection for monitoring Y mean,
<table><tr><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td></tr><tr><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td></tr><tr><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td></tr><tr><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td></tr><tr><td>32</td><td>33</td><td>34</td><td>35</td><td>36</td><td>37</td><td>38</td><td>39</td></tr><tr><td>40</td><td>41</td><td>42</td><td>43</td><td>44</td><td>45</td><td>46</td><td>47</td></tr><tr><td>48</td><td>49</td><td>50</td><td>51</td><td>52</td><td>53</td><td>54</td><td>55</td></tr><tr><td>56</td><td>57</td><td>58</td><td>59</td><td>60</td><td>61</td><td>62</td><td>63</td></tr></table></td></tr>
<tr><td>2E</td><td>md_ymean</td><td>00</td><td>Motion ymean monitoring register</td></tr>
<tr><td>2F</td><td>md_fcnt</td><td>00</td><td>Motion frame counter monitoring register</td></tr>
</table>

▷ ***Dark filter (1) -- Dark filter horizontal axis control register & total gain***

Address bank	Address hex	register name	default (h)	Description
C	9E	dark_xref1_g0	0C	Dark filter x-axis reference
	9F	dark_xref2_g0	20	
	A0	dark_xref3_g0	40	
	A1	dark_xref1_g1	0C	
	A2	dark_xref2_g1	18	
	A3	dark_xref3_g1	20	



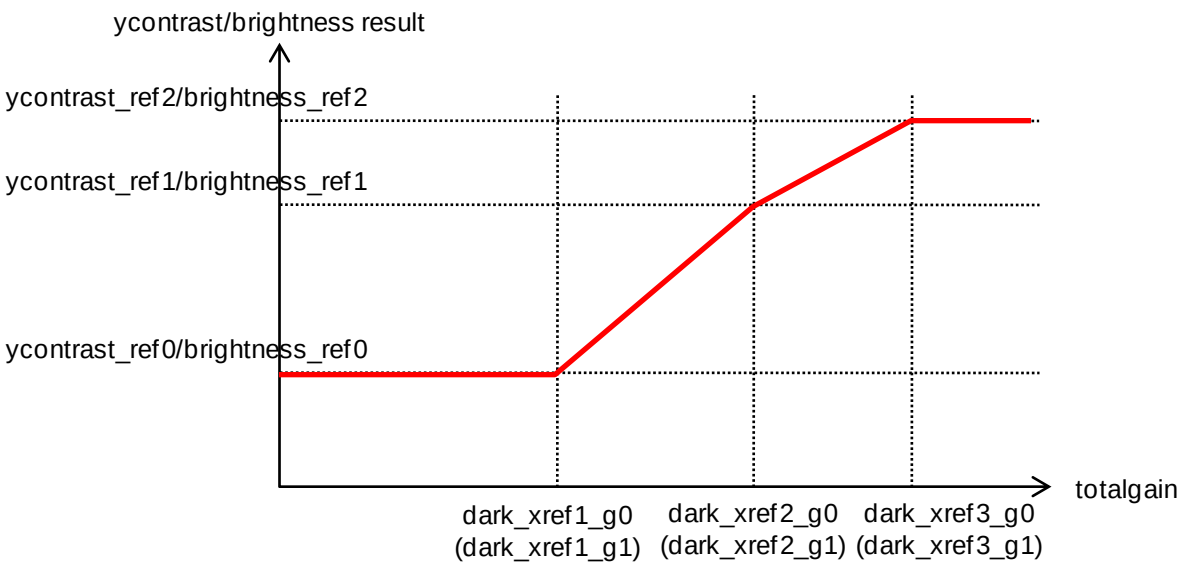
▷ ***Dark filter (2) - Lens shading compensation gain, Noise filter , Interpolation, Offset, High resolution threshold. Contrast , Gamma Correction. Color correction.***

Address bank	Address hex	register name	default (h)	Description	
C	A6	dark_lens0	00	○ Dark lens fitting control :dark_lens0/1/2 conditions : 00h ≤ dark_lens0 ≤ dark_lens1 ≤ dark_lens2 ≤ FFh	1)auto_control4[7] = '0b' => User can define it by manual. 2)auto_control4[7] = '1b' => Automatically defined.
	A7	dark_lens1	00		
	A8	dark_lens2	00		
	A9	dark_lens	00		
	B2	dark_blf0	5F	○Dark bilateral filter fitting control :00h ≤ dark_blf2 ≤ dark_blf1 ≤ dark_blf0 ≤ 7Fh	
	B3	dark_blf1	3F		
	B4	dark_blf2	3F		
	B5	dark_blf	7F		
	B6	dark_nf0	40	○Dark noise floor fitting control : 00h ≤ dark_nf0 ≤ dark_nf1 ≤ dark_nf2 ≤ FFh	
	B7	dark_nf1	40		
	B8	dark_nf2	40		
	B9	dark_nf	01		
	BA	dark_intp0	00	○Dark interpolation fitting control :00h ≤ dark_intp0 ≤ dark_intp1 ≤ dark_intp2 ≤ 1Fh	
	BB	dark_intp1	08		
	BC	dark_intp2	18		
	BD	dark_intp	00		
	BE	dark_dir_offset0	10	○Dark direction offset fitting control :00h≤dark_dir_offset0≤dark_dir_offset1≤dark_dir_offset2≤ 1 Fh	
	BF	dark_dir_offset1	10		
	C0	dark_dir_offset2	10		
	C1	dark_dir_offset	10		
	C2	dark_hr_th0	04	○Dark high resolution TH. :00h ≤ dark_hr_th0 ≤ dark_hr_th1 ≤ dark_hr_th2 ≤ 1Fh	
	C3	dark_hr_th1	08		
	C4	dark_hr_th2	18		
	C5	dark_hr_th	04		
	C7	y_cont_th_ref0	FF	○Dark y contrast th fitting control	
	C8	y_cont_th_ref1	FF		
	C9	y_cont_th_ref2	FF		
	CA	y_cont_th	FF		
	CB	y_cont_slope_ref0	50	○Dark y contrast slope fitting control	
	CC	y_cont_slope_ref1	50		
	CD	y_cont_slope_ref2	50		
	CE	y_cont_slope	50		
	D2	dark_y_gm0	00	○Dark Y gamma fitting control :00h ≤ dark_y_gm0≤dark_y_gm1≤dark_y_gm ≤ 20h	
	D3	dark_y_gm1	10		
	D4	dark_y_gm2	3F		
	D5	dark_y_gm	00		
	D6	dark_rgb_gm0	00	○Dark RGB gamma fitting control :00h ≤ dark_rgb_gm0≤dark_rgb_gm1≤dark_rgb_gm ≤ 20h	
	D7	dark_rgb_gm1	00		
	D8	dark_rgb_gm2	00		
	D9	dark_rgb_gm	00		
	DA	dark_ccr0	00	○Dark color correction fitting control :00h ≤ dark_ccr0 ≤ dark_ccr1 ≤ dark_ccr2 ≤ FFh	
	DB	dark_ccr1	04		
	DC	dark_ccr2	08		
	DD	dark_ccr	00		

▷ ***Dark filter (3) -- Contrast and Brightness***

Address		register name	default (h)	Description
bank	hex			
B	91	ycontrast_ref0	40	Dark Y contrast fitting control
	92	ycontrast_ref1	40	
	93	ycontrast_ref2	40	
	94	ycontrast	40	
	95	ybrightness_ref0	00	Dark Y brightness fitting control
	96	ybrightness_ref1	00	
	97	ybrightness_ref2	00	
	98	ybrightness	00	

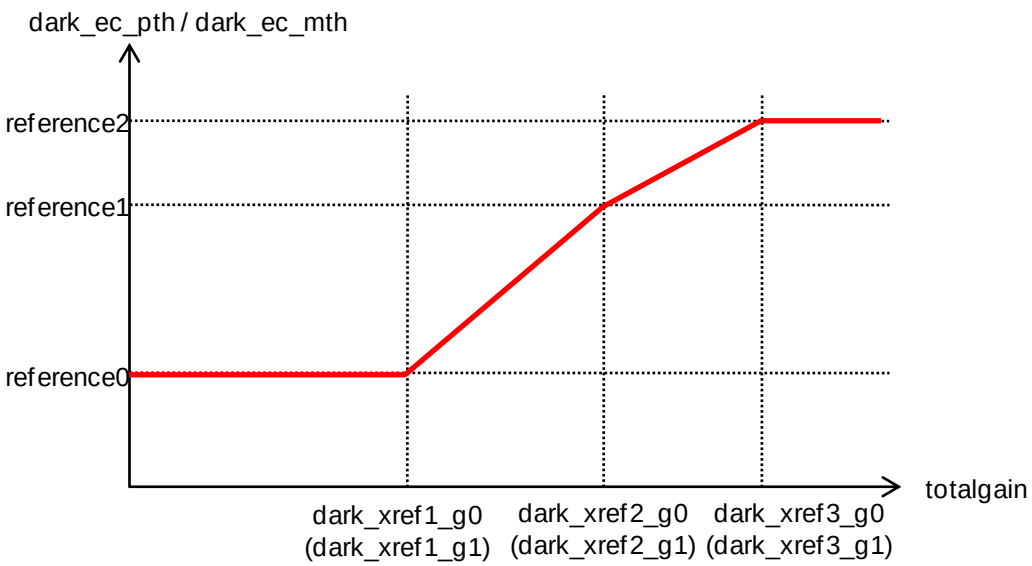
User can control contrast and brightness in an exposure time by controlling ycontrast_ref0~2/ ybrightness_ref0~2 as below figure.
When auto_control3[2] = '0b', then user can program ycontrast/ybrightness manually.
Also, user can change ycontrast/ybrightness with auto_control6[7,6](ycontrast/ybrightness group selection).



▷ ***Dark filter (4) -- edge enhancement***

Address		register name	default (h)	Description
bank	hex			
D	96	dark_ec_pth0	04	Dark edge clamp plus threshold filter control 00h ≤ dark_ec_pth0 ≤ dark_ec_pth1 ≤ dark_ec_pth2 ≤ FFh
	97	dark_ec_pth1	04	
	98	dark_ec_pth2	04	
	99	dark_ec_pth	04	
	9A	dark_ec_mth0	04	Dark edge clamp minus threshold filter control 00h ≤ dark_ec_mth0 ≤ dark_ec_mth1 ≤ dark_ec_mth2 ≤ FFh
	9B	dark_ec_mth1	04	
	9C	dark_ec_mth2	04	
	9D	dark_ec_mth	04	

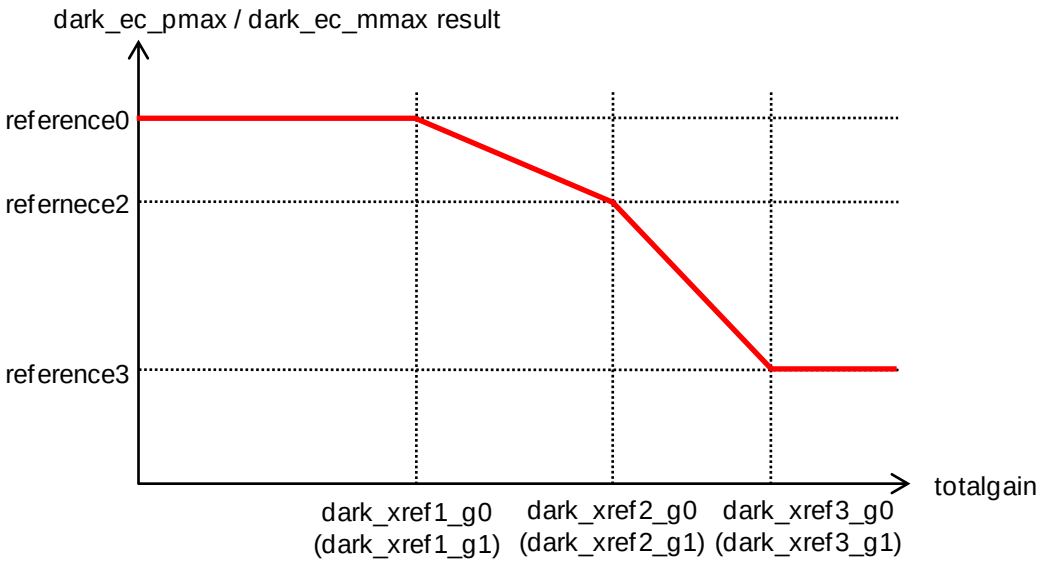
※In case auto_control4[7] is set to '0b' :
User can write the value directly in dark_ec_pth / dark_ec_mth register.
※auto_control4[7] = '1b' : It is fitted automatically as below figure.
※User can select the reference point group by auto_control5[7:6]



▷ ***Dark filter (5) -- edge clamp maximum of edge enhancement***

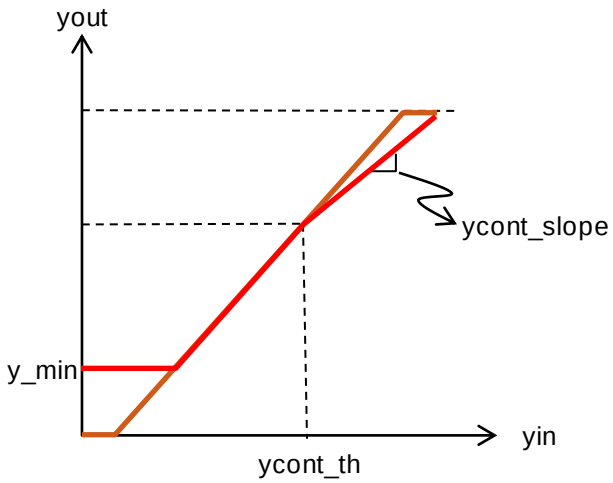
Address		register name	default (h)	Description
bank	hex			
D	9E	dark_ec_pmax0	80	Dark edge clamp plus max filter control 00h ≤ dark_ec_pmax 2≤ dark_ec_pmax 1≤ dark_ec_pmax 0≤ 7Fh
	9F	dark_ec_pmax1	80	
	A0	dark_ec_pmax2	80	
	A1	dark_ec_pmax	80	
	A2	dark_ec_mmax0	80	Dark edge clamp minus max filter control 00h ≤ dark_ec_mmax 2≤ dark_ec_mmax 1≤ dark_ec_mmax 0≤ 7Fh
	A3	dark_ec_mmax1	80	
	A4	dark_ec_mmax2	80	
	A5	dark_ec_mmax	80	

※In case auto_control4[7] is set to '0b' :
User can write the required values directly in dark_ec_pth / dark_ec_mth register.
※auto_control4[7] = '1b' : It is fitted automatically as below figure.
※User can select the reference point group of x -axis by auto_control6[3:2]
and defines the reference point of y-axis by dark_ec_pmax0~2 / dark_ec_mmax0~2



▷ ***Y min***

Address		register	default	Description
bank	hex	name	(h)	
D	94	y_min	00	Control register for Output Y min Y min is minimum vale of output data Y.



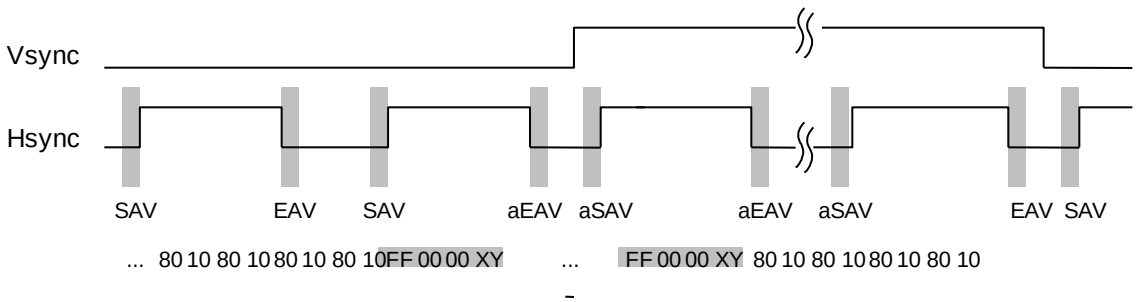
▷ ***CCIR656 control***

Address bank	Address hex	register name	default (h)	Description
D	63	sync_blankEAV_f0	B6	Blank EAV for field0 of CCIR656 data or blank EAV for frame data
	64	sync_blankSAV_f0	AB	Blank SAV for field0 of CCIR656 data or blank SAV for frame data
	65	sync_activeEAV_f0	9D	Active EAV for field0 of CCIR656 data or active EAV for frame data
	66	sync_activeSAV_f0	80	Active SAV for field0 of CCIR656 data or active SAV for frame data
	67	sync_blankEAV_f1	F1	blank EAV for field1 of CCIR656 data
	68	sync_blankSAV_f1	EC	blank SAV for field1 of CCIR656 data
	69	sync_activeEAV_f1	DA	Active EAV for field1 of CCIR656 data
	6A	sync_activeSAV_f1	C7	Active SAV for field1 of CCIR656 data
	6B	sync_CCIR_FF	FF	CCIR data format
	6C	sync_CCIR_00	00	▷ ***sync_ccirFF :*** CCIR data format FFh
	6D	sync_CCIR_80	80	▷ ***sync_ccir00 :*** CCIR data format 00h
	6E	sync_CCIR_10	10	▷ ***sync_ccir80 :*** CCIR data format 80h ▷ ***sync_ccir10 :*** CCIR data format 10h

▷ ***ccir656 sync index value***

EAV and SAV data value for synchronization.

Address	Name	Description
64, 68h	*BlankSAV*	Blank Range Start of Video
63, 67h	*BlankEAV*	Blank Range End of Video
65, 69h	*ActiveEAV*	Active Range End of Video
66, 6Ah	*ActiveSAV*	Active Range Start of Video



▷ **CCIR656 control 1**

Address bank	Address hex	register name	bit#	Bit name	default (h)		Description
D	6F	CCIR 656 control 1	7	bt656_sel	90	1	BT656 mode selection bits @ NTSC mode [Fig11] 00b : even field output(720x240), odd filed output (720x240) 10b : even field output(720x243), odd filed output (720x243) 11b : even field output(720x244), odd filed output (720x243)
			6			0	
			5	hscale_sel		0	Input image horizontal width selection bits 00b : 720, 01b : 640, 10b : 768
			4			1	
			3	winy_sel		0	Digital output vertical size selection bits@ NTSC mode 00b : even field digital output (720x240), odd field digital output (720x240) 01b : even field digital output (720x243), odd field digital output (720x243) 10b : even field digital output (720x244), odd field digital output (720x243) 11b : even field digital output (720x244), odd field digital output (720x244)
			2			0	
			1	x		0	Reserved
			0	x		0	Reserved

▷ **Flicker control (1) Auto flicker detection control register**

Address bank	Address hex	register name	default (h)	Description
C	4A	afd_th_h	02	Auto flicker detection TH between high and low lux. : Auto flicker detection OFF threshold control registers. If current exposure > afd_th, then flicker detection mode will be OFF automatically even if auto flicker detection mode.
	4B	afd_th_m	07	

▷ **Flicker control (2) Flicker control register**

Address bank	Address hex	register name	bit#	Bit name	default (h)		Description
D	73	flicker_control1	7	x	uu	u	Reserved
			6	fd_en		u	60/50Flicker detection enable 0b : disable, 1b : enable
			5	af_1pd_en		u	'1' : if (exposure< 1 flicker_period) then auto_fd_en='1'
			4	af_fh_en		u	'1' : if (exposure > auto_fd_th) then auto_fd_en='1'
			3	manual_A		u	Manual_A
			2	manual_B		u	Manual_B
			1	fd_comp		u	Flicker comp : 00b : 2cycle detect, 01b : 3 cycle detect, else : 4 cycle detect
			0			u	

▷ ***Flicker control (3)***

Address bank	Address hex	register name	default (h)	Description
D	74	auto_fd	0	Auto flicker detection enable monitoring
	75	fd_a_step_h	u	Flicker detection step for A state
	76	fd_a_step_l	u	
	77	fd_b_step_h	3	Flicker detection step for B state
	78	fd_b_step_l	u	
	79	fd_winheight	40	Flicker detection window height
	7A	fd_a_delay	0	Flicker detection delay for A state
	7B	fd_b_delay	0	Flicker detection delay for A state
	7C	fd_th	10	Flicker detection TH.
	7D	fd_period_a_h	u	Flicker period for A state
	7E	fd_period_a_m	u	
	7F	fd_period_a_l	u	
	80	fd_period_b_h	01	Flicker period for B state
	81	fd_period_b_m	u	
	82	fd_period_b_l	u	
	83	fd_period_c_h	u	Flicker period for 1/20 second
	84	fd_period_c_m	u	
	85	fd_minfr	04	Flicker TH. for 1/20 second

▷ Flicker detection step A & B

Before auto flicker detection mode enable, user must set fd_A_step and fd_B_step.
fd_A_step and fd_B_step are calculated by as below.

$$fd\_A\_step = \frac{256*256*4}{fd\_period\_A\_h \,\&\, fd\_period\_A\_m}$$

$$fd\_B\_step = \frac{256*256*4}{fd\_period\_B\_h \,\&\, fd\_period\_B\_m}$$

▷ Flicker period A & B

fd_period_A can be programmed by flicker period for 1/120 sec.
fd_period_B can be programmed by flicker period for 1/100 sec.
Flicker period for 1/120 sec and 1/100 sec are calculated by as below.

$$fd\_period\_A = \frac{256\ d*\ PCLK\ FREQ.}{120d\ *\ framewidth}$$

$$fd\_period\_B = \frac{256\ d*\ PCLK\ FREQ.}{100d\ *\ framewidth}$$

Where, framewidth is register value. PCLK FREQ. is frequency of pixel clock.
default value : U è wire-strapping register

▷ **LED & Moving IR/AR glass filter control**

Address bank	Address hex	register name	bit#	Bit name	default (h)		Description
D	86	LED_control1	7	ledctrl en	00	0	Led control , 0b : disable, 1b : enable
			6	ledctrl manual		0	Led output value @ led control disable
			5	ledctrl polarity		0	Led output polarity change, 0b : normal 1b : Reverse
			4	bwled en		0	Black & white mode @ led on 0b : disable, 1b : enable
			3	mirs en		0	Moving IR/AR glass switch (MIRS) control) 0b : disable, 1b : enable
			2	mirs manual		0	MIRS output value @ MIRS control disable
			1			0	
			0	mirs polarity		0	MIRS output polarity change 0b : normal 1b : Reverse
D	87	LED_control2	7	x	00	0	Reserved
			6	x		0	Reserved
			5	x		0	Reserved
			4	x		0	Reserved
			3	ledctrl mode		0	LEd control mode selection 00b : LED control with CdS 01b : auto LED control without CdS 10b: auto LED control with CdS * Please find Reg. E-33h~E-46h for in detail
			2			0	
			1	bust kill		0	TV encoder color burst kill 0b : disable, 1b: enable
			0	x		0	Reserved

▷ ***Auto IR-LED control***

Address bank	Address hex	register name	default (h)	Description
E	33	ledlight_h	00	LED brightness level monitoring @@led_control2[3:2] = "01b" or "10b
	34	ledlight_m	00	
	35	ledlight_l	00	
	36	led_on	00	LED Status monitoring=> LED ON : 01d, LED Off : 00d @led_control2[3:2] = "01b" or "10b
	37	ledcnt	00	LED ON OFF time delay monitoring
	38	min_ledlight_h	00	LED brightness of Minimum / Maximum @led_control2[3:2] = "01b" or "10b and led_on=1
	39	min_ledlight_m	01	
	3A	max_ledlight_h	03	
	3B	max_ledlight_m	FF	
	3C	led_speed	08	Brightness transition Speed
	3D	led_exposure_t	00	The fixed exposure value @led_control2[3:2] = "01b" or "10b
	3E	led_exposure_h	C2	
	3F	led_exposure_m	A0	
	40	led_exposure_l	00	
	41	led_pp_th	07	The minimum value of the pulse positive width @led_control2[3:2] = "01b" or "10b
	42	led_pw_h	00	The LED positive pulse width @led_control2[3:2] = "01b" or "10b
	43	led_pw_l	00	
	44	led_pp_h	03	LED Pulse width cycle@led_control2[3:2] = "01b" or "10b"
	45	led_pp_l	FF	
	46	led_mtr	00	LED on/off monitoring register @led_control2[3:2] = "00b" or "01b

▷ **SPI address update**

Address		register name	bit#	Bit name	default (h)		Description
bank	hex						
D	92	spi_addr_update	7	x	00	0	Reserved
			6	x		0	Reserved
			5	x		0	Reserved
			4	x		0	Reserved
			3	x		0	Reserved
			2	x		0	Reserved
			1	x		0	Reserved
			0	spi_addr_update		0	Whenever frame start is activate, it start to read the stored OSD data in reference of spi_sadd/spi_paddr. If there is some problem, you should reverse spi_addr_update[0] after writing spi_saddr and spi_paddr.

▷ ***SPI baud rate***

Address bank	Address hex	register name	default (h)	Description
D	A6	spi_baud_rate	0D	SPI baud rate Default value of SPI_baud_rate is 0Dh which corresponds to SPI clock frequency of 1.13MHz. So, before up-loading large amount of data such as OSD data from SPI ROM, SPI_baud_rate must be adjusted to a reasonable value to maximize the data rate. SPI_baud_rate = 0 : SCK= 27.00 MHz = 27/1 SPI_baud_rate = 1 : SCK= 13.50 MHz = 27/2 SPI_baud_rate = 2 : SCK= 09.50 MHz = 27/3 SPI_baud_rate = 3 : SCK= 06.75 MHz = 27/4 SPI_baud_rate = 4 : SCK= 05.40 MHz = 27/5 SPI_baud_rate = 5 : SCK= 04.50 MHz = 27/6 SPI_baud_rate = 6 : SCK= 03.86 MHz = 27/7 SPI_baud_rate = 7 : SCK= 03.38 MHz = 27/8 SPI_baud_rate = 8 : SCK= 03.00 MHz = 27/9 SPI_baud_rate = 9 : SCK= 02.70 MHz = 27/10 SPI_baud_rate = 10 : SCK= 02.25 MHz = 27/12 SPI_baud_rate = 11 : SCK= 01.69 MHz = 27/16 SPI_baud_rate = 12 : SCK= 01.35 MHz = 27/20 SPI_baud_rate = 13 : SCK= 01.13 MHz = 27/24 SPI_baud_rate = 14 : SCK= 00.96 MHz = 27/28 SPI_baud_rate = 15 : SCK= 00.84 MHz = 27/32

▷ **OSD transparency control**

Address bank	Address hex	register name	default (h)	Description
D	A7	osd_opac	10	OSD transparency control. The control range : 0~16d. 0d : transparency 100%, 16d : transparency 0%

▷ **SPI OSD control**

Address bank	Address hex	register name	bit#	Bit name	default (h)		Description
D	A8	*spi_osd_control*	7	x	uu	u	Reserved
			6	x		u	Reserved
			5	x		u	Reserved
			4	x		u	Reserved
			3	x		u	Reserved
			2	x		u	Reserved
			1	osd_boundary		0	OSD boundary osd_boundary = '0': disable osd_boundary = '1': enable
			0	osd_enable		u	OSD display Enable bit [strap_osd_en] osd_enable = '0' : OSD disable osd_enable = '1' : OSD enable default value : U ➔ wire-strapping register

spi_osd_en (strap_osd_en) D-A8h	pg_en (default='1b') E-04h	Parking guide line display
0	0	SPI OSD(x), embedded PG(x)
0	1	SPI OSD(x), embedded PG(x)
1	0	SPI OSD(o), embedded PG(x)
1	1	SPI OSD(x), embedded PG(o)

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▷ OSD data start/stop address

Address bank	Address hex	register name	default (h)	Description
D	A9	spi_saddr_h	00	OSD data start address
	AA	spi_saddr_m	00	
	AB	spi_saddr_l	00	
	AC	spi_paddr_h	00	*OSD data stop address*
	AD	spi_paddr_m	00	
	AE	spi_paddr_l	00	

OSD data start/stop address. SPI master will read osd command stored in SPI-ROM from OSD data start address to OSD data stop address whenever a field start. Actually, user should reverse reg_spi_addr_update to apply osd data start/stop address after writing osd data start/stop address

▷ OSD color value control

Address bank	Address hex	register name	default (h)	Description
D	AF	palette_1_y	90	Palette_1 Y/CB/CR value for OSD color.
	B0	palette_1_cb	35	
	B1	palette_1_cr	22	
	B2	palette_2_y	D2	Palette_2 Y/CB/CR value for OSD color
	B3	palette_2_cb	10	
	B4	palette_2_cr	92	
	B5	palette_3_y	51	Palette_3 Y/CB/CR value for OSD color
	B6	palette_3_cb	5A	
	B7	palette_3_cr	F0	
	B8	palette_4_y	EB	Palette_4 Y/CB/CR value for OSD color
	B9	palette_4_cb	80	
	BA	palette_4_cr	80	
	BB	palette_5_y	6A	Palette_5 Y/CB/CR value for OSD color
	BC	palette_5_cb	CA	
	BD	palette_5_cr	DD	
	BE	palette_6_y	A9	Palette_6 Y/CB/CR value for OSD color
	BF	palette_6_cb	A5	
	C0	palette_6_cr	10	
	C1	palette_7_y	29	Palette_7 Y/CB/CR value for OSD color
	C2	palette_7_cb	F0	
	C3	palette_7_cr	6D	
	C4	palette_8_y	10	Palette_8 Y/CB/CR value for horizontal boundary of OSD line.
	C5	palette_8_cb	80	
	C6	palette_8_cr	80	

▷ ***resolution enhance in Encoder block***

Address bank	Address hex	register name	default (h)	Description
D	C7	resol_gain	08	Resolution enhance gain @Encoder
	FF	resol_th	00	Resolution enhance threshold @Encoder

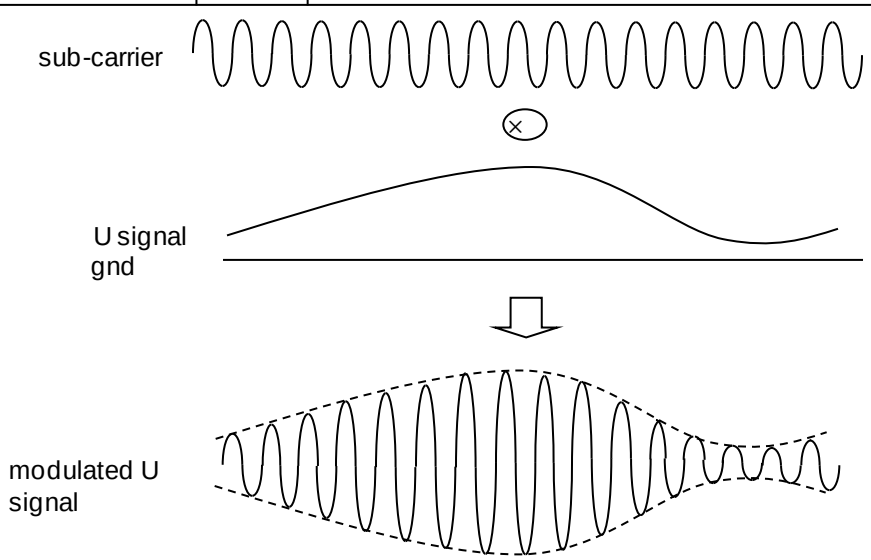
▷ ***gen_lock control of Encoder block***

Address bank	Address hex	register name	default (h)	Description
D	C8	enc_fcnt_genlock	01	Gen_lock control for encoder block
	C9	enc_rcnt_genlock_h	00	
	CA	enc_rcnt_genlock_l	01	
	CB	enc_ccnt_genlock_h	00	
	CC	enc_ccnt_genlock_l	03	

▷ **Encoder control**

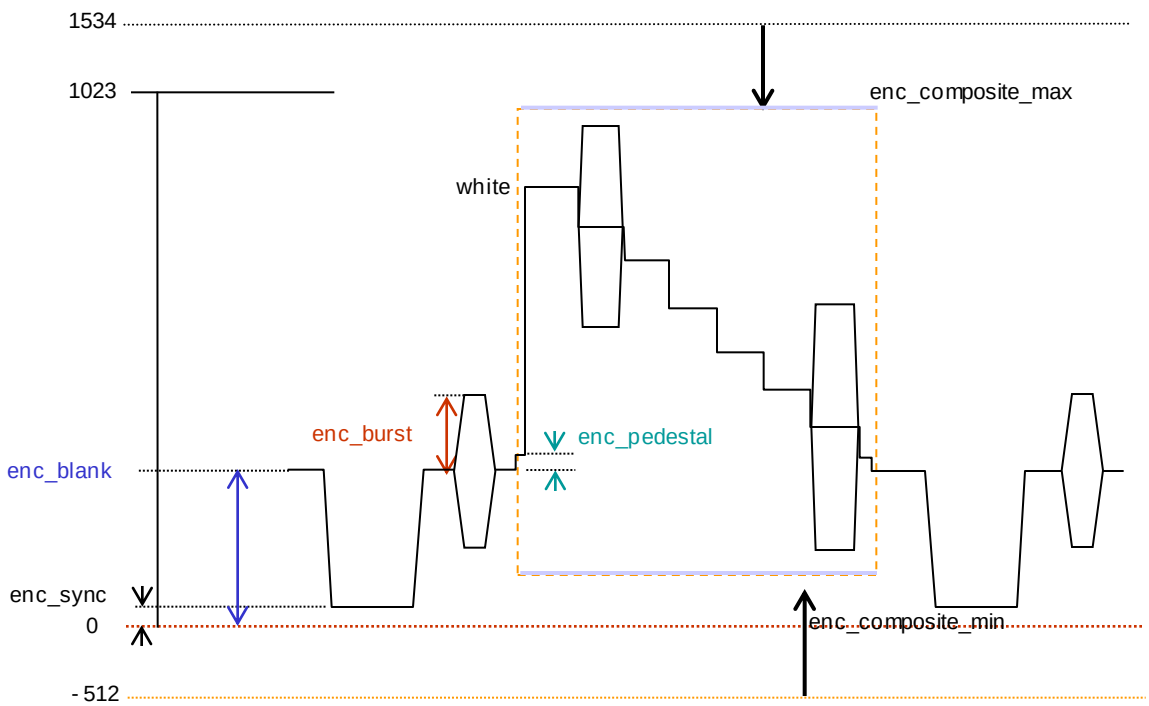
Address bank	Address hex	register name	bit#	Bit name	default (h)		Description
D	CD	enc_control	7	x	44	x	Reserved
			6	enc_lpfY_off		1	Low pass filter control for luminance @Encoder 0b : luminance low pass filter on 1b : luminance low pass filter off
			5	enc_lpfC_off		0	Low pass filter control for chrominance @Encoder 0b : chrominance low pass filter on 1b : chrominance low pass filter off
			4	enc_colorbar_en		0	Color bar on/off for test
			3	enc_colorbar_mode		0	0b : 100% color bar, 1b : 75% color bar
			2	bt656_standard		1	BT656 standard for 525 line system
			1	enc_monitor_sw		0	Monitor switch on off for test
			0	yin_range		0	Input Y range selection 0b : 1~254, 1b : 16~235

Address bank	Address hex	register name	default (h)	Description
D	CE	enc_scfreq	uu	Subcarrier frequency selection for which TV mode default value : U è wire-strapping register "00" : 3.579545 MHz for (M) NTSC, NTSC-J "01" : 4.43361875 MHz for (B, D, G, H, I, N) PAL "10" : 3.58205625 MHz for (Nc) PAL "11" : 3.57561149 MHz for (M) PAL Sub-carrier signal is used for modulating chrominance data via QAM C= U*sin(ωt) + V*cos(ωt)

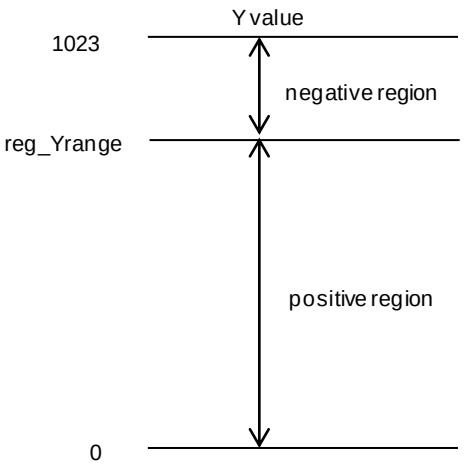


▷ **Composite level parameters**

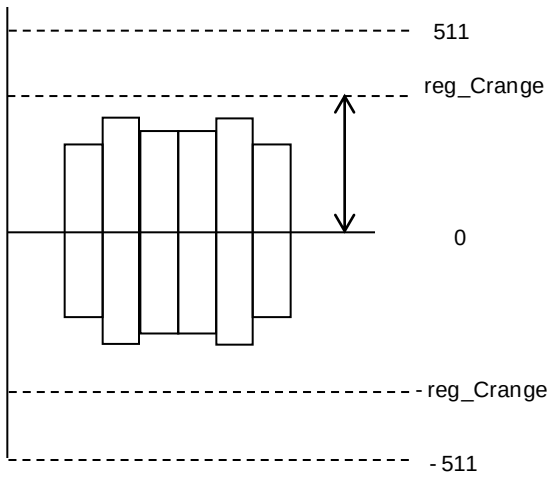
Address bank	Address hex	register name	default (h)	Description
D	CF	enc_sync	10	Encoder sync level
	D0	enc_blankH	00	Encoder blank level
	D1	enc_blankL	U	
	D2	enc_pedestal	U	Encoder pedestal
	D3	enc_burst	U	Burst amplitude
	D4	enc_Ygain	U	Y convergence gain from YCbCr to YUV
	D5	enc_Ugain	U	U convergence gain from YCbCr to YUV
	D6	enc_Vgain	U	V convergence gain from YCbCr to YUV
	D7	enc_Yrange_H	03	Max. luminance
	D8	enc_Yrange_L	20	:Separate Y range into positive and negative regions.
	D9	enc_Crange_H	01	Max. amplitudes of chrominance
	DA	enc_Crange_L	U	:Define maximum level of Chrominance.
	DB	enc_chroma_max_H	03	Maximum chrominance of composite output
	DC	enc_chroma_max_L	U	:Define maximum level of Composite.
	DD	enc_chroma_min_H	00	Minimum chrominance of composite output
	DE	enc_chroma_min_L	U	=>Define minimum level of Composite. =>default value : U => wire-strapping register



reg_enc_composite_max/min registers define the max. and min. of active data level.



reg_Yrange defines the boundary between positive or negative number of Y before composition.
In colorbar, Y might be negative values. It is the reason why the register exists.



reg_Crange designates the maximum amplitude of chroma.
It can be one of 0 to 511.

▷ ***Luminance & chrominance low pass filter for encoder***

Address bank	Address hex	register name	default (h)	Description
D	DF	enc_lpyc0	04	Luminance low-pass filter coefficient
	E0	enc_lpyc1	13	
	E1	enc_lpyc2	13	
	E2	enc_lpyc3	92	
	E3	enc_lpyc4	E4	
	E4	enc_lpys	03	Signs of luminance low-pass filter coefficients
	E5	enc_lpcc0	01	Chrominance low-pass filter coefficient
	E6	enc_lpcc1	03	
	E7	enc_lpcc2	04	
	E8	enc_lpcc3	03	
	E9	enc_lpcc4	00	
	EA	enc_lpcc5	06	
	EB	enc_lpcc6	0F	
	EC	enc_lpcc7	16	
	ED	enc_lpcc8	16	
	EE	enc_lpcc9	0B	
	EF	enc_lpcc10	0F	
	F0	enc_lpcc11	35	
	F1	enc_lpcc12	63	
	F2	enc_lpcc13	8F	
	F3	enc_lpcc14	AE	
	F4	enc_lpcc15	BA	
	F5	enc_lpcsH	03	Signs of chrominance low-pass filter coefficients
	F6	enc_lpcsL	F0	
	F7	enc_y_preclamp	00	Pre-clampping Y into LPF.

▷ ***enc_lpys***

Signs of enc_lpyc0~4.

Bit No.	4	3	2	1	0
mapping	lpyc4	lpyc3	lpyc2	lpyc1	lpyc0

▷ ***enc_lpcs***

Signs of enc_lpcc0~15.

enc_lpcsH

Bit No.	7	6	5	4	3	2	1	0
mapping	lpcc15	lpcc14	lpcc13	lpcc12	lpcc11	lpcc10	lpcc9	lpcc8

enc_lpcsL

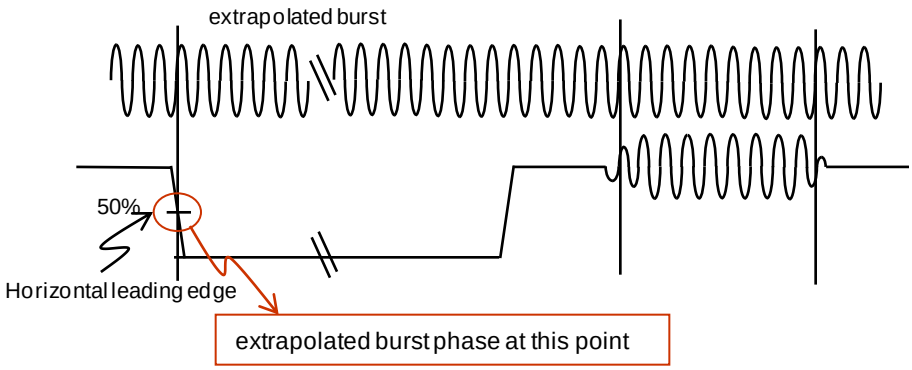
Bit No.	7	6	5	4	3	2	1	0
mapping	lpcc7	lpcc6	lpcc5	lpcc4	lpcc3	lpcc2	lpcc1	lpcc0

▷ ***Subcarrier to horizontal phase offset***

Address bank	Address hex	register name	default (h)	Description
D	F8	enc_SCH_offset_T	00	SCH(subcarrier to horizontal) phase offset 0° = 00 00 00 00 h 90° = 40 00 00 00 h 180° = 80 00 00 00 h 270° = C0 00 00 00 h
	F9	enc_SCH_offset_H	00	
	FA	enc_SCH_offset_M	00	
	FB	enc_SCH_offset_L	00	

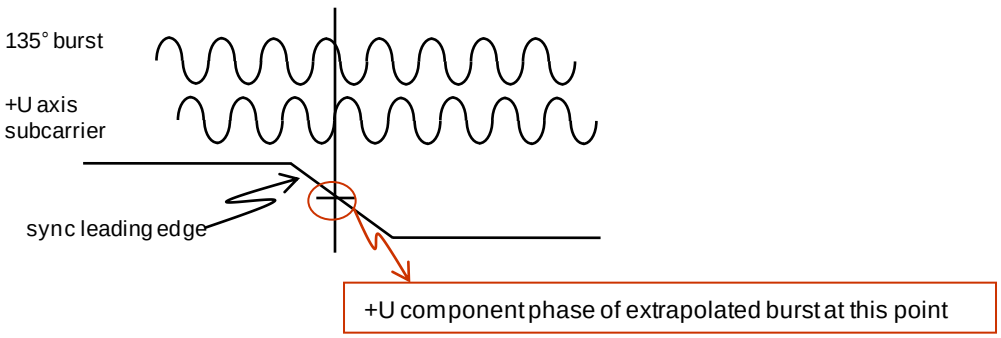
NTSC

Definition: The phase relationship between the leading edge of horizontal sync(at the 50% amplitude point) and the zero crossings of the color burst (by extrapolating the color burst to the leading edge of sync)



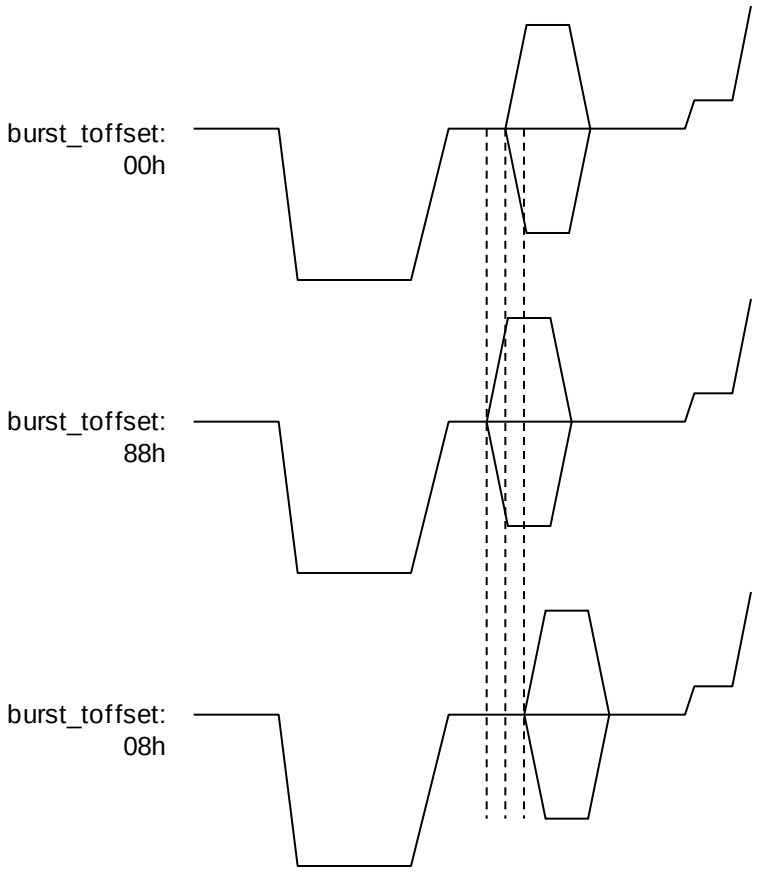
PAL

Definition: The phase of the +U component of the color burst extrapolated to the half-amplitude point of the leading edge of the synchronizing pulse of line 1 of field 1. This means that the phase of the +U axis of the subcarrier is zero relative to the horizontal timing reference point(the mid-point of the leading edge of the line sync pulse)



▷ **Burst time offset**

Address		register	default	Description
bank	hex	name	(h)	
D	FD	burst_toffset	00	Burst time +/- offset It changes burst position on Back Porch. MSB: sign, other bits : magnitude

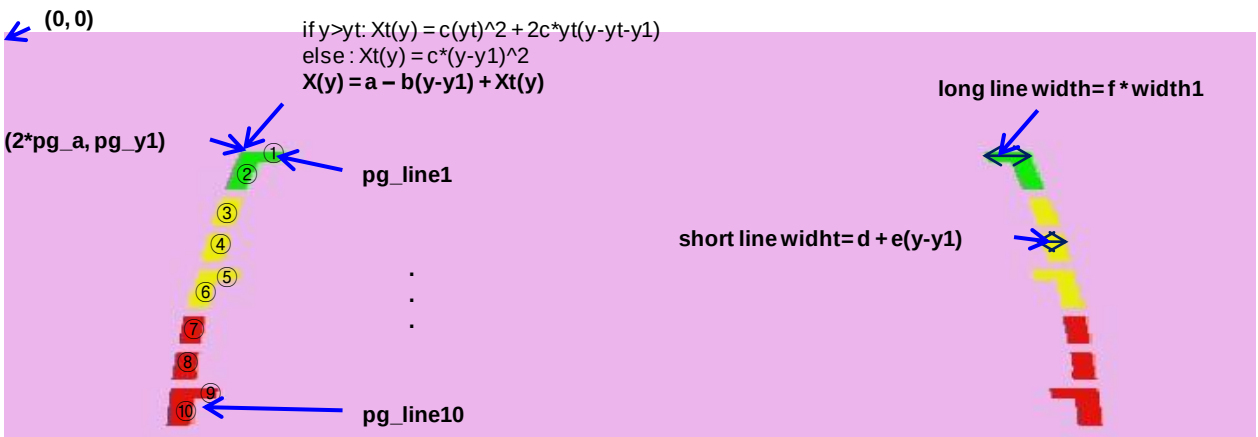


▷ ***Embedded Parking Guide Line control (1)***

Address		register name	bit#	Bit name	default (h)		Description
bank	hex						
E	04	pg_control	7	x	09	x	Reserved
			6	x		x	Reserved
			5	x		x	Reserved
			4	x		x	Reserved
			3	x		1	Reserved
			2	pg_rm		0	remove left side of parking guide line
			1			0	remove right side of parking guide line
			0	pg_enable		1	Embedded parking guide line enable bit. In case user don't use external SPI ROM, it can use the em bedded parking guide line by pg_enable bit control. If you want to use the external parking guide line by using SPI ROM, you should set this bit to '0"

▷ ***Embedded Parking Guide Line control (2)***

Address bank	Address hex	register name	default (h)	Description
E	5	pg_yt	7F	the boundary of straight line and a curve
	6	pg_y1	3C	the start position of 10 points
	7	pg_y2	02	
	8	pg_y3	0B	
	9	pg_y4	19	
	0A	pg_y5	2C	
	0B	pg_y6	42	
	0C	pg_y7	45	
	0D	pg_y8	5F	
	0E	pg_y9	7C	
	0F	pg_y10	81	
	10	pg_a	72	X-axis Start point, X-axis value = 2x(pg_a), Min=01h
	11	pg_b	3E	The slope of embedded parking guide line.
	12	pg_c	87	The weight of slope.
	13	pg_d	07	Embedded parking guide line Width (Min : 04h)
	14	pg_e	0A	Embedded parking guide line width weight.
	15	pg_f	15	long line width
	16	pg_line1	A1	The information decision of each dot line pg_line1~10 (7): line type ➔ '0': short line width '1': long line width pg_line1~10 [6:5]: palette color information of line ➔ palette number 0~3 pg_line1~10 [4:0]: height of each line.
	17	pg_line2	26	
	18	pg_line3	2B	
	19	pg_line4	4F	
	1A	pg_line5	52	
	1B	pg_line6	C2	
	1C	pg_line7	55	
	1D	pg_line8	78	
	1E	pg_line9	E4	
	1F	pg_line10	7E	
	20	pg_center_h	01	It defines the center position of embedded parking guide line.
	21	pg_center_l	3E	



reg_pgcenter

1/3.7 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

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