PIXELPLUS CO., LTD. *Brief Data sheet*

Issue No : PD-701-028

1/4 inch VGA class Analog/Digital Output NTSC/PAL CMOS Image Sensor

PC1030N

Rev 1.2

Last update : 14 . Dec. 2010

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1/4 inch VGA class Analog/Digital Output NTSC/PAL CMOS Image Sensor

▶ Revision History

Version	Date [D/M/Y]	Notes	Writer
0.0	20/05/2008	*(Preliminary)*	Jong Beom Choi
0.1	04/06/2008	Customer datasheet is released	SungJe Cheon
0.2	20/06/2008	DVDD voltage is modified	SungJe Cheon
0.3	04/07/2008	Add DC Characteristics Add AC Characteristics Add Optical Performance Add Power Sequence	Junhee Cho
0.4	09/07/2008	Modify effective pixel area. Fig.10	SungJe Cheon
0.5	22/07/2008	Modify LED Control	Bongju Lee
0.6	28/07/2008	Add VGA digital output only mode	SungJe Cheon
0.7	23/09/2008	Removed “Preliminary” letters	Jincheol Jeong
0.8	06/02/2009	Released Power Sequence	Yoon Shik Kim
0.9	27/03/2009	Change (Total pixel array → Effective pixel array)	Heungseok Park
1.0	21/05/2009	Add Application note	Jongwu Ryu
1.1	22/09/2009	Change(SCLK → SSCLK, SDAT → SSDAT, RCLK → RSCLK, RDAT → RSDAT)	JiKyung Moon
1.2	14/12/2010	Edited for Brief type	Chang hui Ye

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1/4 inch VGA class Analog/Digital Output NTSC/PAL CMOS Image Sensor

▶ Table of Contents

1/4 inch VGA class Analog/Digital Output NTSC/PAL CMOS Image Sensor

▶ Features

▷ 648 x 488 Effective pixel array with RGB bayer color filters and micro-lens and optical black pixel.

▷ Power supply :
AVDD : 2.8V, CVDD : 2.8V, DVDD : 1.8V, HVDD : 2.8 ~ 3.3V

▷ Output formats :
CVBS (NTSC/PAL),
ITU-R. BT601/656(60 fields/sec. interlaced @ 27MHz) with CVBS,
320x240(288) YCbCr422 (30(25)fps. @ 27MHz) with CVBS,
640x480(VGA) YCbCr422 digital output only (30fps. @ 27MHz).

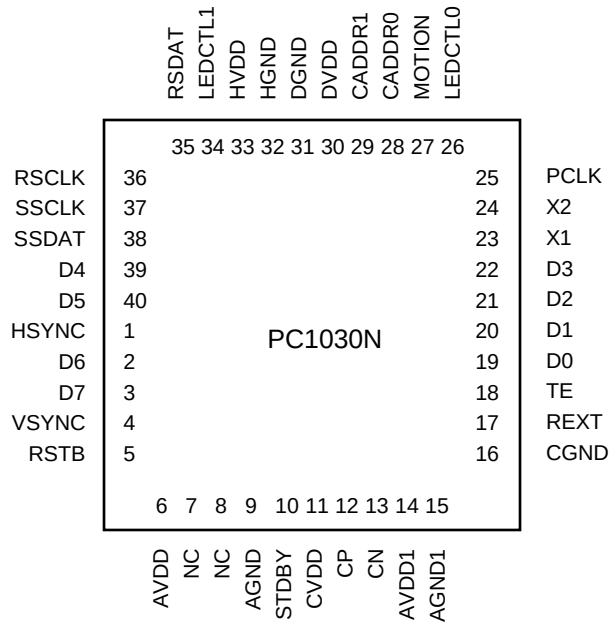
▷ Image processing on chip :
lens shading, gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, brightness, contrast, saturation, auto black level compensation, auto white balance, auto exposure control and back light compensation.

▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus.

▷ VGA / QVGA / QQVGA / CIF / QCIF Scaling.

▷ 50Hz, 60Hz flicker automatic cancellation.

▷ High Image Quality and High low light performance.



[Fig. 1] PIN Description (CLCC)

Optical Format	¼ inch
Pixel Size	5.55 um x 5.55 um
Effective Pixel Array	648 x 488
Effective Image Area	3596.4um x 2708.4um
Clock Frequency	27 MHz
Frame Rate	60(50) fields/sec @ 27MHz
Dark Signal	47.9 [mV/sec] @60'C
Sensitivity	3.16 [V/Lux.sec]
Power Consumption	213 [mW] @ Dynamic
	19.2 [uW] @ Standby
Operating Temp. (Fully Functional Temp.)	-40'C ~ 105'C
Dynamic Range	63.5 [dB] @60'C
SNR	45.6 [dB] @60'C

[Table 1] Typical Parameters

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▶ PIN Descriptions

[Table 2] Pin Descriptions

PIN No.	Name	I/O Type	Functions / Descriptions
1	HSYNC	O	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
2	D6	O	Bit 6 of parallel data output.
3	D7	O	Bit 7 of parallel data output.
4	VSYNC	O	Vertical sync : Indicates the start of a new frame.
5	RSTB	I	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
6	AVDD	P	Analog Power supply : 2.8V DC with 0.1uF capacitor to AGND.
7	N.C		
8	N.C		
9	AGND	P	Analog Power ground
10	STDBY	I	Power standby mode. When STDBY='1' there's no current flow in any analog circuit branch, neither any beat of digital clock. D<9:0> and PCLK, HSYNC, VSYNC pins can be programmed to tri-state or all '1' or all '0'. But it is possible to control internal registers through I2C bus interface in STDBY mode. All registers retain their current values.
11	CVDD	P	DAC Power supply : 2.8V DC with 0.1uF capacitor to AGND.
12	CP	O	Composite signal. (Connect to 75ohm to AGND)
13	CN	O	Connect 37.5ohm to AGND
14	AVDD1	P	Analog Power supply : 2.8V DC with 0.1uF capacitor to AGND.
15	AGND1	P	Analog Power ground
16	CGND	P	DAC Power ground.
17	REXT	I	External Resistor. The resistor value can be changed by user tuning. (Connect to 30Kohm to AGND)
18	TE	I	Chip Test Mode enable. (Connect to HGND)
19	D0	O	Bit 0 of parallel data output.
20	D1	O	Bit 1 of parallel data output.
21	D2	O	Bit 2 of parallel data output.
22	D3	O	Bit 3 of parallel data output.
23	X1	I	Master clock input pad or Crystal input pad
24	X2	O	Crystal output pad
25	PCLK	O	Pixel clock. Data can be latched by external devices at the rising or falling edge of PCLK. The polarity and drivability can be controlled.
26	LEDCTRL0	O	LED Control bit 0. LEDCTRL[1:0] provide 2bit combination of enable signal which can turn-on LED device when low light condition.

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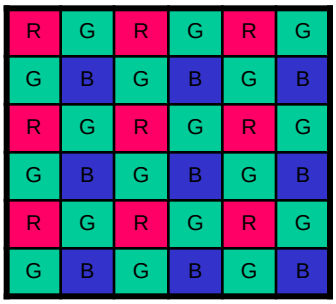
PIN No.	Name	I/O Type	Functions / Descriptions
27	MOTION	O	Motion detection. It lets user or processor know whether there are motion of something on video. When the motion exists on the video, the output goes LOW to HIGH
28	CADDR0	I	Chip address bit 0. Chip address can be changed If this CADDR[1:0] pins are tied to HVDD or HGND.
29	CADDR1	I	Chip address bit 1. Chip address can be changed If this CADDR[1:0] pins are tied to HVDD or HGND.
30	DVDD	P	Digital Power supply : 1.8V DC with 0.1uF to DGND
31	DGND	P	Digital Power ground.
32	HGND	P	I/O Power ground.
33	HVDD	P	I/O Power supply: 2.8~3.3V DC with 0.1uF capacitor to HGND.
34	LEDCTRL1	O	LED Control bit 1. LEDCTRL[1:0] provide 2bit combination of enable signal which can turn-on LED device when low light condition.
35	RSDAT	I/O	2-wire serial interface for external EEPROM.
36	RSCLK	O	2-wire serial interface for external EEPROM
37	SSCLK	I	2-wire serial interface slave clock input.
38	SSDAT	I/O	2-wire serial interface slave databus.
39	D4	O	Bit 4 of parallel data output.
40	D5	O	Bit 5 of parallel data output.

▶ Digital Data Formats



[Fig. 4] Bayer Color filter pattern

Pixel array is covered by Bayer color filters as can be seen in the [Fig. 4]. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PC1030N sensor provides this Bayer pattern RGB data through an 9-bit channel. It takes one PCLK to pass one pixel RGB data to output bus. Generally one pixel of an image consists of R,G,B color components. Since one pixel of bayer RGB is composed of one of the 3 components, the other two components of a pixel must be derived from neighbor pixels. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as an average of its four nearest R neighbors.

This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PC1030K adopts a low pass filter to prevent the interference patterns (called Moire pattern) from degrading the image quality too much. After color interpolation, every pixel has all three color components. And then the pixel data pass image processing block to improve the image quality.

It is possible to extract monochrome luminance data from RGB color components and the conversion equation is : Y = 0.299R + 0.587G + 0.114B where R,G and B are gamma corrected color components. And the color information is separated from luminance information according to following equations.

$$Cb = -0.148R - 0.291G + 0.439, \quad Cr = 0.439R - 0.368G - 0.071B$$

Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality.

Cb1	Y1	Cr1	Y2	Cb3	Y3	Cr3	Y4	…

[Fig. 5] 4:2:2 YCbCr data sequence.

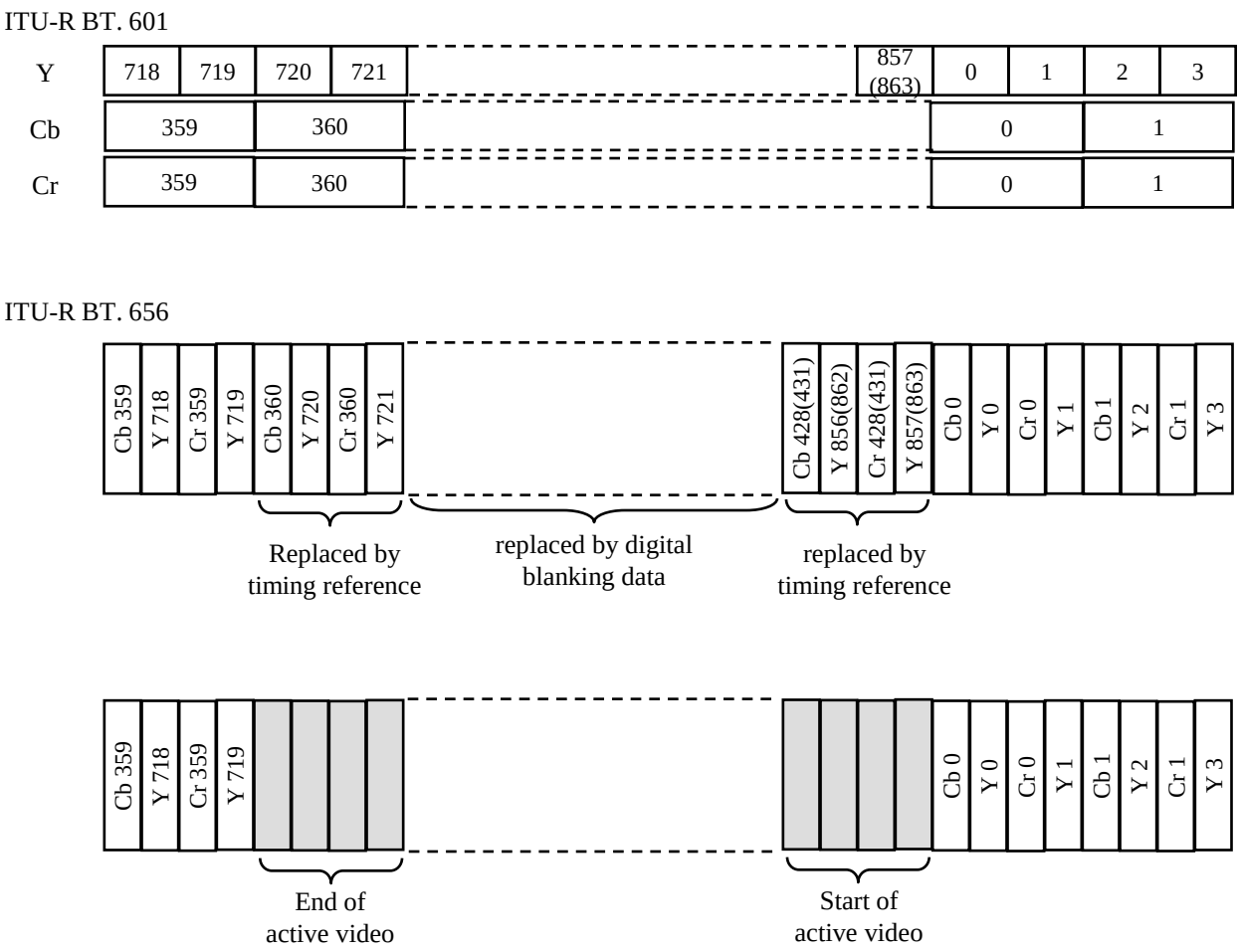
PC1030K supports 4:2:2 YCbCr data format where Cb and Cr components are horizontally sub-sampled such that U and V for every other pixel are omitted. PC1030K also support 4:2:2 YUV data format.

▶ Data and Synchronization Timing

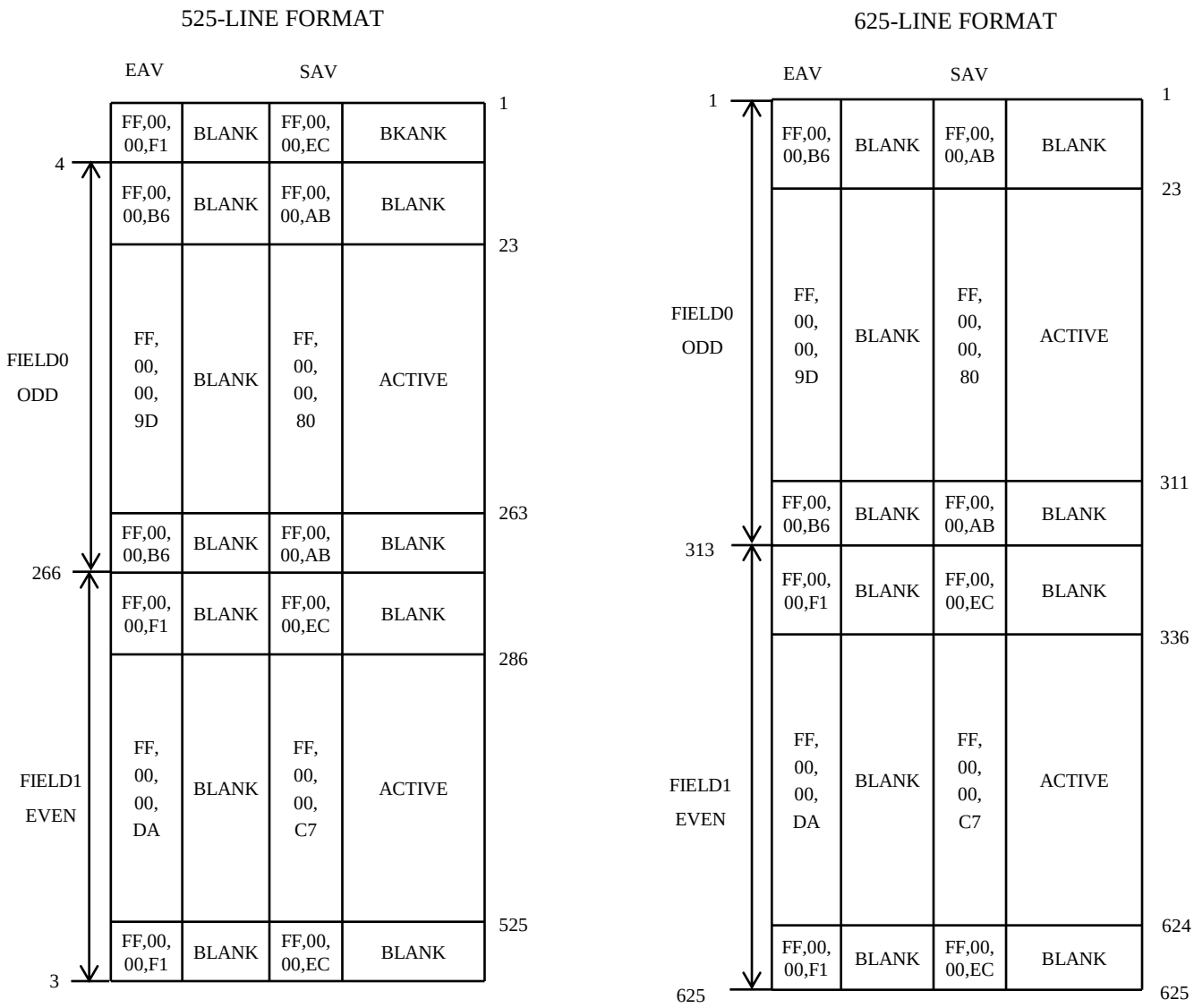
(1) ITU-R BT656 (CCIR656)

[Fig. 6] shows ITU-R BT601 and ITU-R BT656 timing diagram. Sampling clocks of ITU-R BT601 and ITU-R BT656 are 13.5MHz and 27MHz respectively. ITU-R BT656 format is generated from ITU-R BT601 format data by serialization and timing reference. Timing reference indicates Start or End of video. It includes field, vsync and hsync information.

PC1030N provides two kinds of active video sizes with BT656 format such as 720x480i and 720x576i ('i' stands for interlaced scan). The horizontal size is stretched from 640 to 720 pixels. 720x480i size BT656 supports for 525-line video, and 720x576i size BT656 for 625-line video. Horizontal timing of 720x480i and 720x576i size BT656 is shown in [Fig. 6] and vertical Timing diagram is shown in [Fig. 7]



[Fig. 6] Timing diagram of ITU-R BT601 and ITU-R BT656



[Fig. 7] Vertical Timing diagram of ITU-R BT656

• The numbers on the image indicate Line number.

• For 525-line format, active lines are 240 per a field. For 625-line format, active lines are 288 per a field.

• Vertical Timing is slightly different to Typical BT.656 for 525-line format. In active data regions above [Fig. 7], they have only active pixel data not any fixed data (eg. black data).

• (design reference: Video Demystified 3rd edition, chapter 4)

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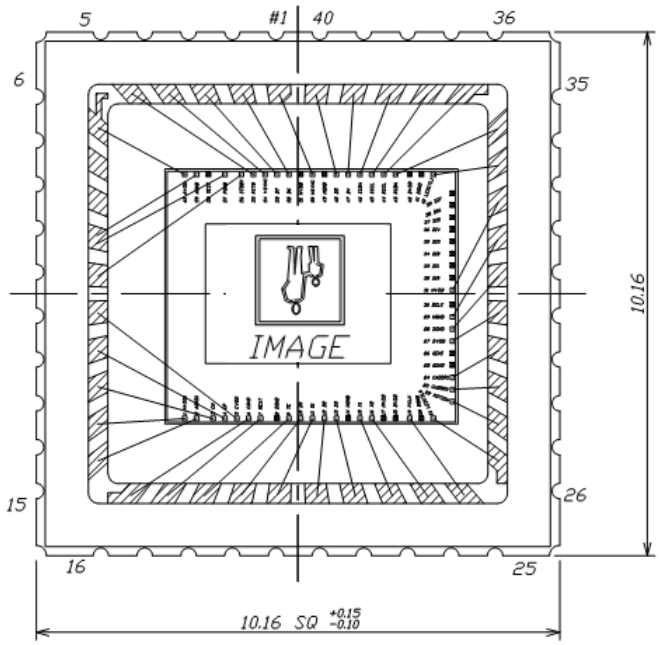
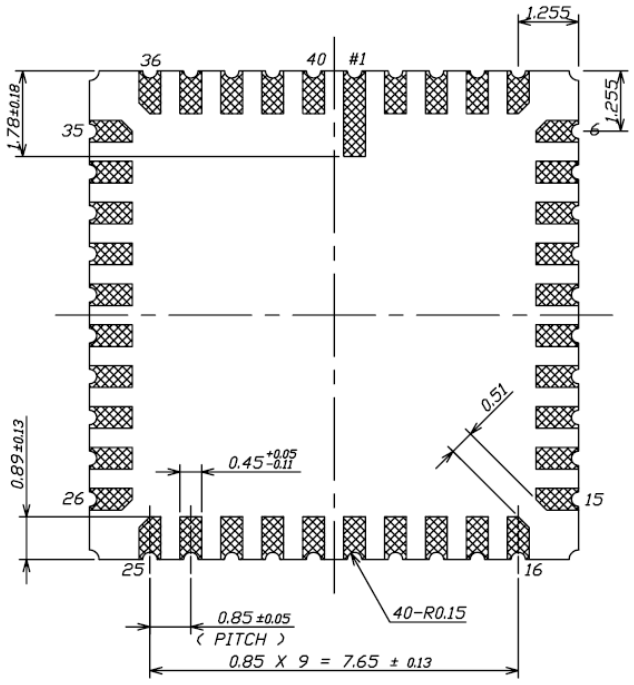
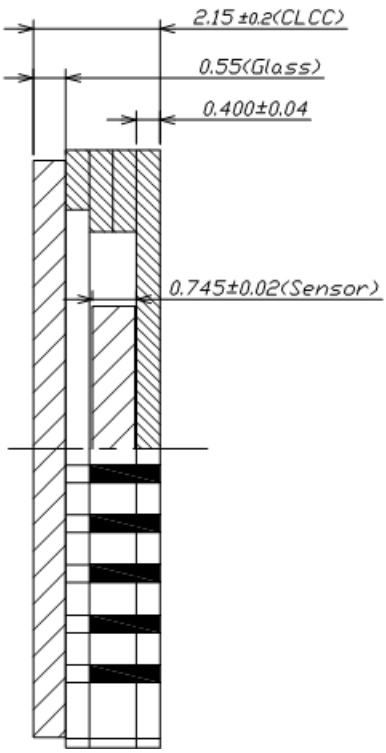


[Image Center = Package center]

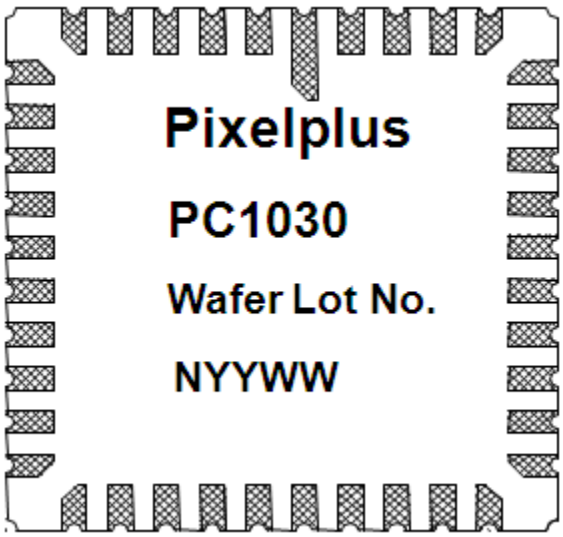
[Top View]



[Bottom View]



[Side View]



Marking Rule

- N: Sensor Version
- YYWW: Work week code

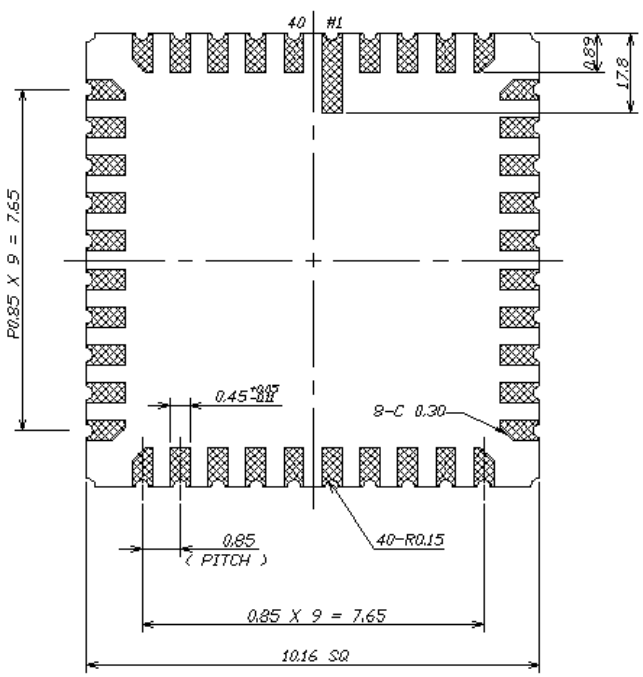
1/4 inch VGA class Analog/Digital Output
NTSC/PAL CMOS Image Sensor

Package Pin Assignment Table

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	HSYNC	11	CVDD	21	D2	31	DGND
2	D6	12	CP	22	D3	32	HGND
3	D7	13	CN	23	X1	33	HVDD
4	VSYNC	14	AVDD1	24	X2	34	LEDCTL1
5	RSTB	15	AGND1	25	PCLK	35	RSDA
6	AVDD	16	CGND	26	LEDCTL0	36	RSCL
7	NC	17	REXT	27	MOTION	37	SSCL
8	NC	18	TE	28	CADDR0	38	SSDA
9	AGND, PGND	19	D0	29	CADDR1	39	D4
10	STDBY	20	D1	30	DVDD	40	D5

Recommended PCB PAD Size for SMT

40CLCC Package Bottom View



Recommended PCB Pattern

BOTTOM View