

PBSS5420D

20 V, 4 A PNP low V_{CEsat} (BISS) transistor

Rev. 02 — 29 September 2008

Product data sheet

1. Product profile

1.1 General description

PNP low V_{CEsat} Breakthrough in Small Signal (BISS) transistor in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

NPN complement: PBSS4420D.

1.2 Features

- Very low collector-emitter saturation resistance
- Ultra low collector-emitter saturation voltage
- 4 A continuous collector current
- Up to 15 A peak current
- High efficiency leading to less heat generation

1.3 Applications

- Power management functions
- Charging circuits
- DC-to-DC conversion
- MOSFET gate driving
- Power switches (e.g. motors, fans)
- Thin Film Transistor (TFT) backlight inverter

1.4 Quick reference data

Table 1. Quick reference data

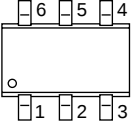
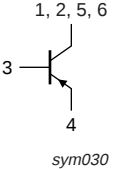
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	-20	V
I_C	collector current		[1] -	-	-4	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	-15	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -4$ A; $I_B = -400$ mA	[2] -	50	70	m Ω

[1] Device mounted on a ceramic Printed-Circuit Board (PCB), Al_2O_3 , standard footprint.

[2] Pulse test: $t_p \leq 300$ μ s; $\delta \leq 0.02$.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	collector		
2	collector		
3	base		
4	emitter		
5	collector		
6	collector		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS5420D	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PBSS5420D	D5

5. Limiting values

Table 5. Limiting values

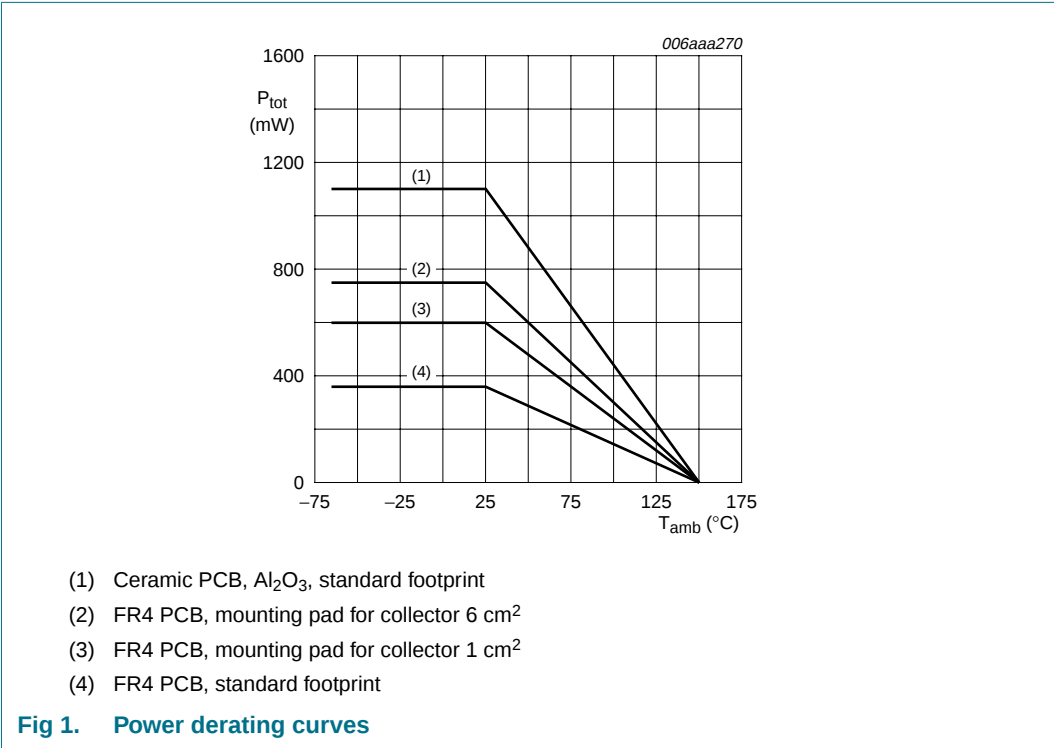
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter	-	−20	V
V _{CEO}	collector-emitter voltage	open base	-	−20	V
V _{EBO}	emitter-base voltage	open collector	-	−5	V
I _C	collector current		[1] -	−4	A
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms	-	−15	A
I _B	base current		-	−0.8	A
I _{BM}	peak base current	single pulse; t _p ≤ 1 ms	-	−2	A
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[2] -	360	mW
			[3] -	600	mW
			[4] -	750	mW
			[1] -	1.1	W
			[2][5] -	2.5	W

Table 5. Limiting values ...continued
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		-65	+150	°C
T_{stg}	storage temperature		-65	+150	°C

- [1] Device mounted on a ceramic PCB, Al_2O_3 , standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
- [4] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm².
- [5] Operated under pulsed conditions: Duty cycle $\delta \leq 10\%$ and pulse width $t_p \leq 10\text{ ms}$.

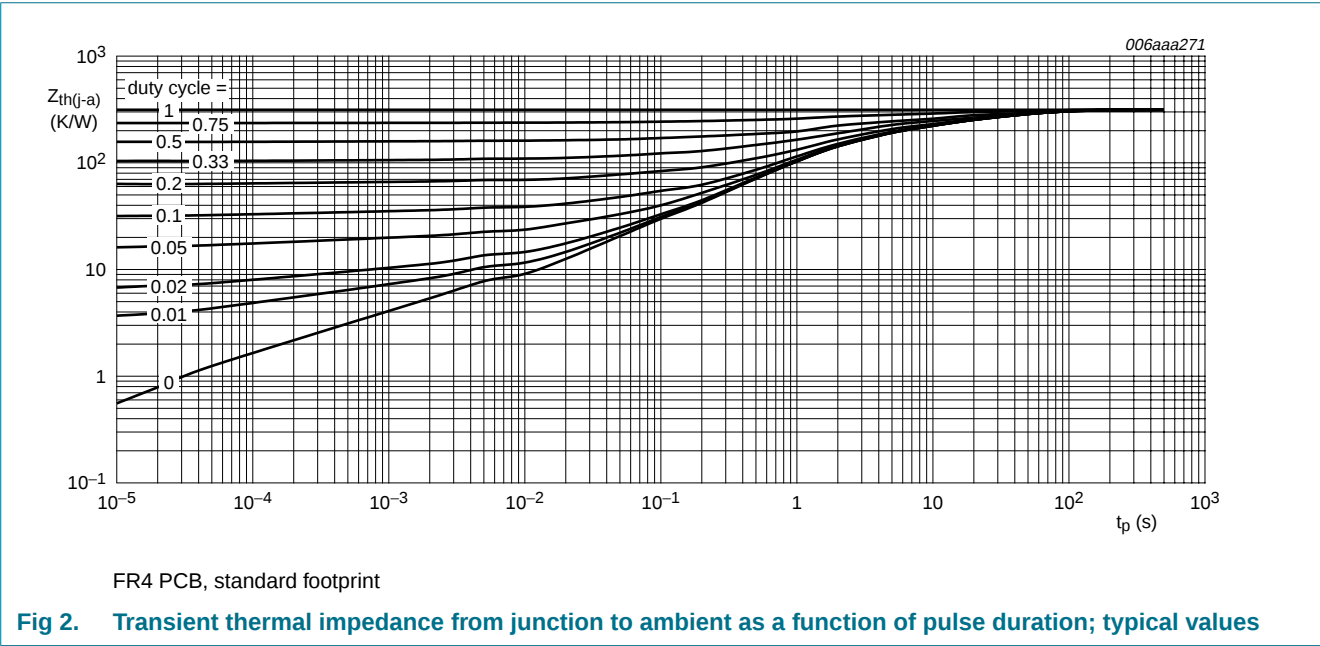


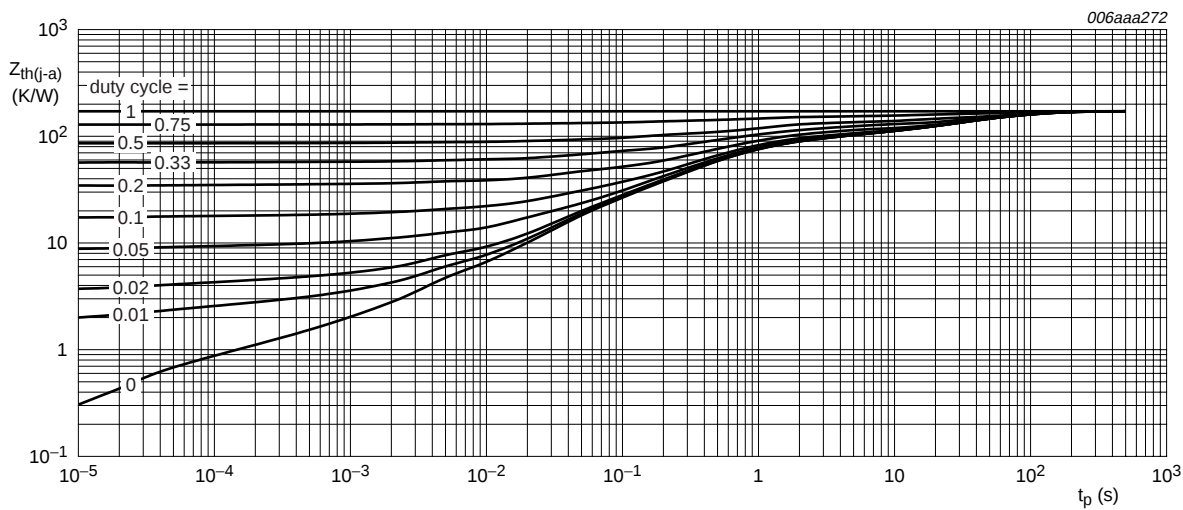
6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	350 K/W
			[2]	-	-	208 K/W
			[3]	-	-	160 K/W
			[4]	-	-	113 K/W
			[1][5]	-	-	50 K/W
R _{th(j-sp)}	thermal resistance from junction to solder point		-	-	45	K/W

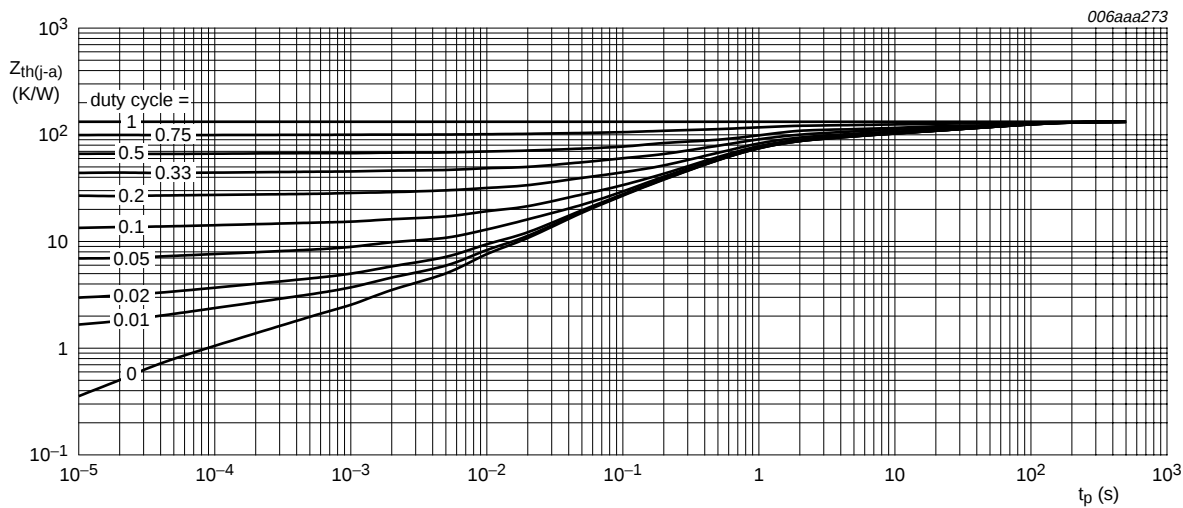
- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm².
- [4] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.
- [5] Operated under pulsed conditions: Duty cycle δ ≤ 10 % and pulse width t_p ≤ 10 ms.





FR4 PCB, mounting pad for collector 1 cm²

Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 6 cm²

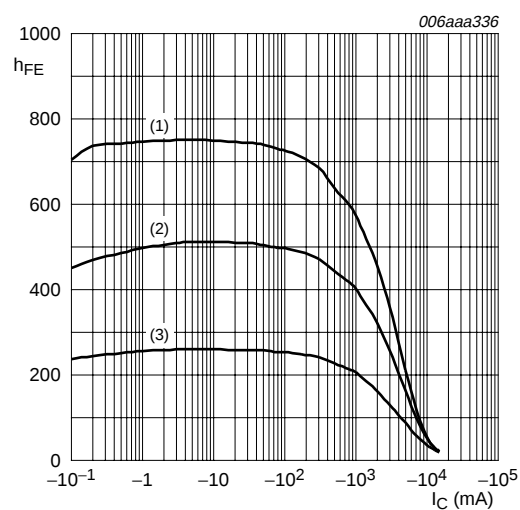
Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

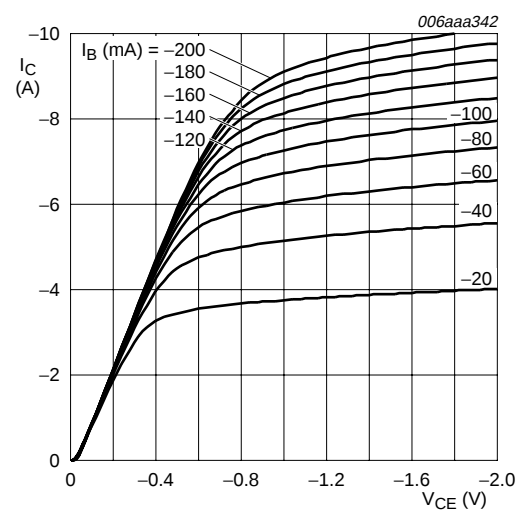
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CBO}	collector-base cut-off current	$V_{CB} = -20\text{ V}; I_E = 0\text{ A}$	-	-	-0.1	μA
		$V_{CB} = -20\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	-50	μA
I_{CES}	collector-emitter cut-off current	$V_{CE} = -20\text{ V}; V_{BE} = 0\text{ V}$	-	-	-0.1	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	-	-	-0.1	μA
h_{FE}	DC current gain	$V_{CE} = -2\text{ V}; I_C = -0.5\text{ A}$	250	400	-	
		$V_{CE} = -2\text{ V}; I_C = -1\text{ A}$ [1]	250	400	-	
		$V_{CE} = -2\text{ V}; I_C = -2\text{ A}$ [1]	200	330	-	
		$V_{CE} = -2\text{ V}; I_C = -4\text{ A}$ [1]	120	200	-	
		$V_{CE} = -2\text{ V}; I_C = -6\text{ A}$ [1]	80	130	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -0.5\text{ A}; I_B = -50\text{ mA}$	-	-35	-50	mV
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	-	-65	-90	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}$	-	-110	-150	mV
		$I_C = -4\text{ A}; I_B = -400\text{ mA}$ [1]	-	-200	-280	mV
		$I_C = -6\text{ A}; I_B = -600\text{ mA}$ [1]	-	-300	-420	mV
R_{CEsat}	collector-emitter saturation resistance	$I_C = -4\text{ A}; I_B = -400\text{ mA}$ [1]	-	50	70	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = -0.5\text{ A}; I_B = -50\text{ mA}$	-	-0.8	-0.85	V
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	-	-0.84	-0.9	V
		$I_C = -1\text{ A}; I_B = -100\text{ mA}$ [1]	-	-0.84	-1	V
		$I_C = -4\text{ A}; I_B = -400\text{ mA}$ [1]	-	-1.0	-1.1	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -2\text{ A}$	-	-0.8	-1	V
t_d	delay time	$V_{CC} = -12.5\text{ V}; I_C = -3\text{ A}; I_{Bon} = -0.15\text{ A}; I_{Boff} = 0.15\text{ A}$	-	10	-	ns
t_r	rise time		-	35	-	ns
t_{on}	turn-on time		-	45	-	ns
t_s	storage time		-	200	-	ns
t_f	fall time		-	80	-	ns
t_{off}	turn-off time		-	280	-	ns
f_T	transition frequency	$V_{CE} = -10\text{ V}; I_C = -0.1\text{ A}; f = 100\text{ MHz}$	-	80	-	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_C = 0\text{ A}; f = 1\text{ MHz}$	-	80	-	pF

[1] Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.



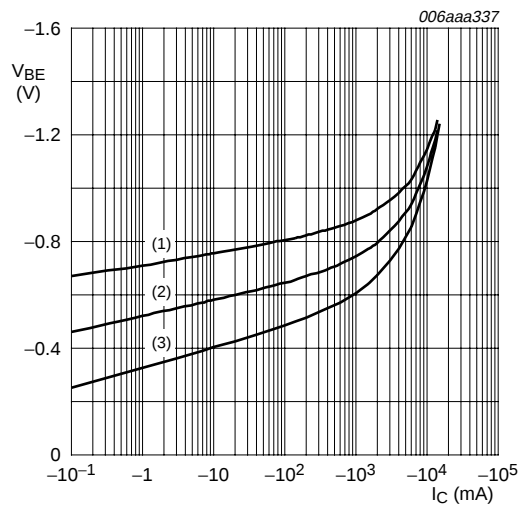
- $V_{CE} = -2$ V
- (1) $T_{amb} = 100$ °C
 - (2) $T_{amb} = 25$ °C
 - (3) $T_{amb} = -55$ °C

Fig 5. DC current gain as a function of collector current; typical values



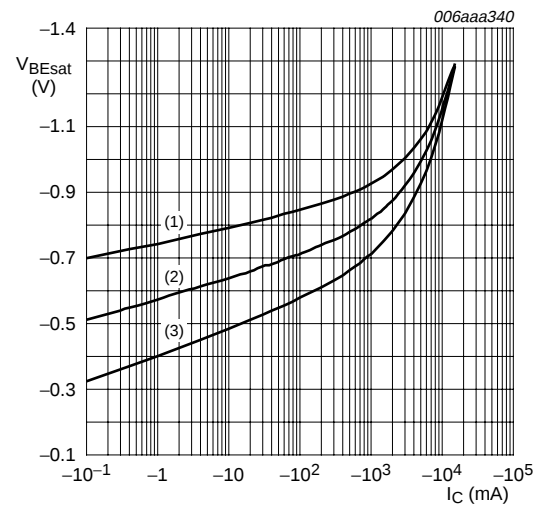
$T_{amb} = 25$ °C

Fig 6. Collector current as a function of collector-emitter voltage; typical values



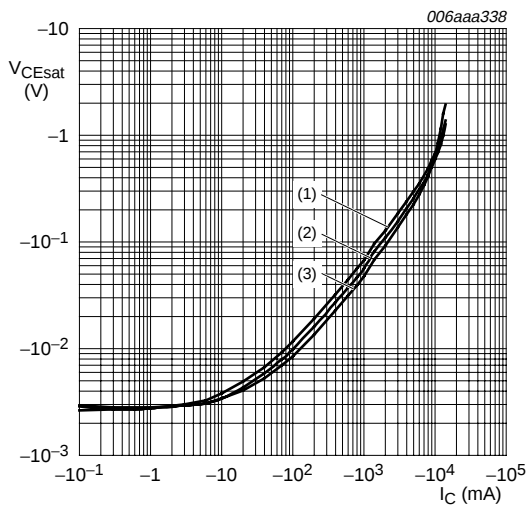
- $V_{CE} = -2$ V
- (1) $T_{amb} = -55$ °C
 - (2) $T_{amb} = 25$ °C
 - (3) $T_{amb} = 100$ °C

Fig 7. Base-emitter voltage as a function of collector current; typical values



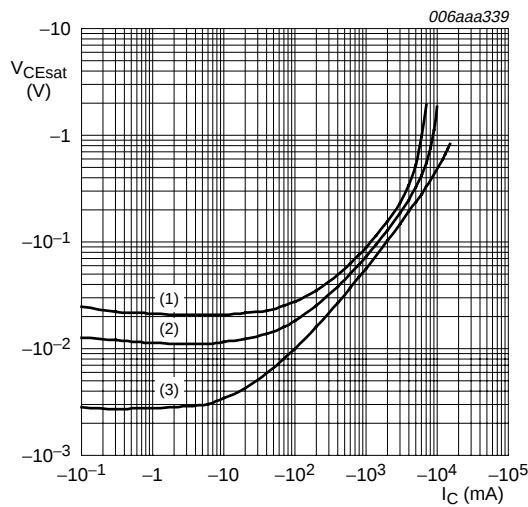
- $I_C/I_B = 20$
- (1) $T_{amb} = -55$ °C
 - (2) $T_{amb} = 25$ °C
 - (3) $T_{amb} = 100$ °C

Fig 8. Base-emitter saturation voltage as a function of collector current; typical values



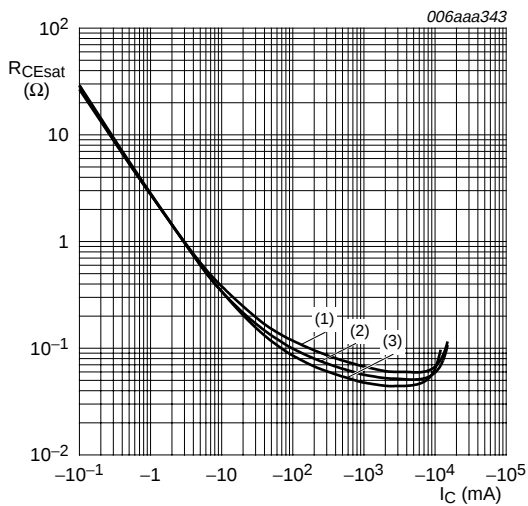
- $I_C/I_B = 20$
- (1) $T_{amb} = 100^\circ C$
 - (2) $T_{amb} = 25^\circ C$
 - (3) $T_{amb} = -55^\circ C$

Fig 9. Collector-emitter saturation voltage as a function of collector current; typical values



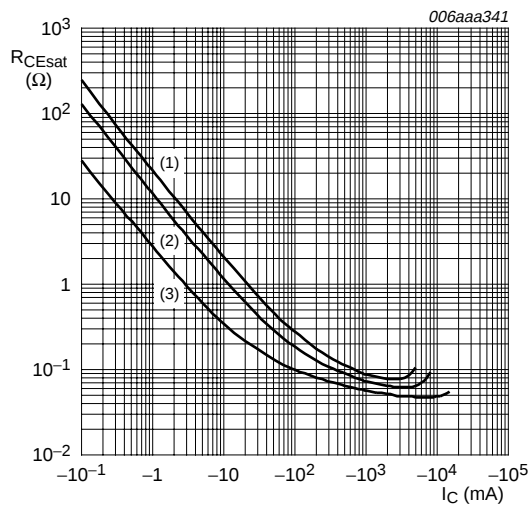
- $T_{amb} = 25^\circ C$
- (1) $I_C/I_B = 100$
 - (2) $I_C/I_B = 50$
 - (3) $I_C/I_B = 10$

Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values



- $I_C/I_B = 20$
- (1) $T_{amb} = 100^\circ C$
 - (2) $T_{amb} = 25^\circ C$
 - (3) $T_{amb} = -55^\circ C$

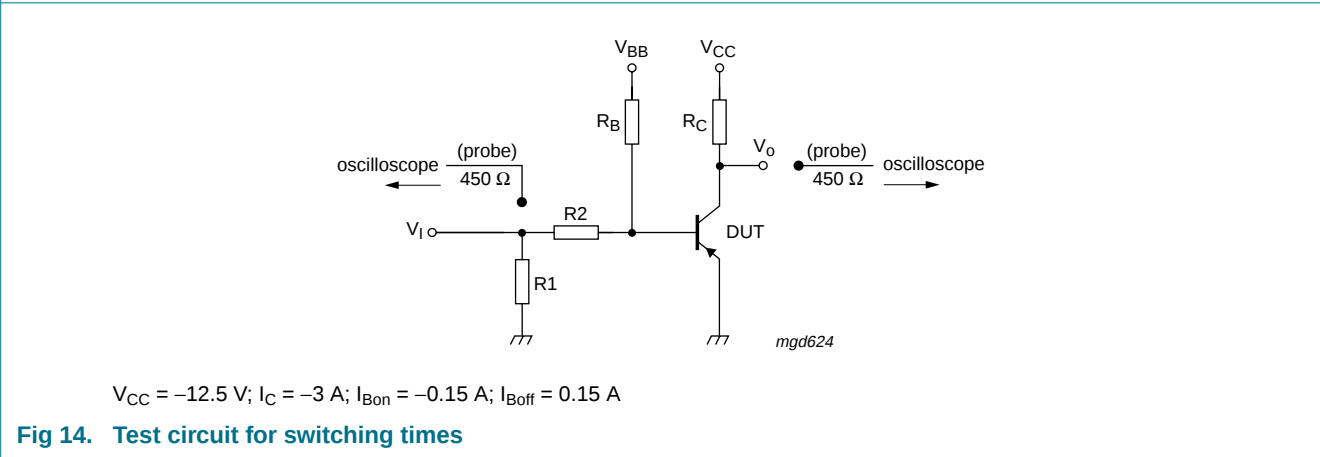
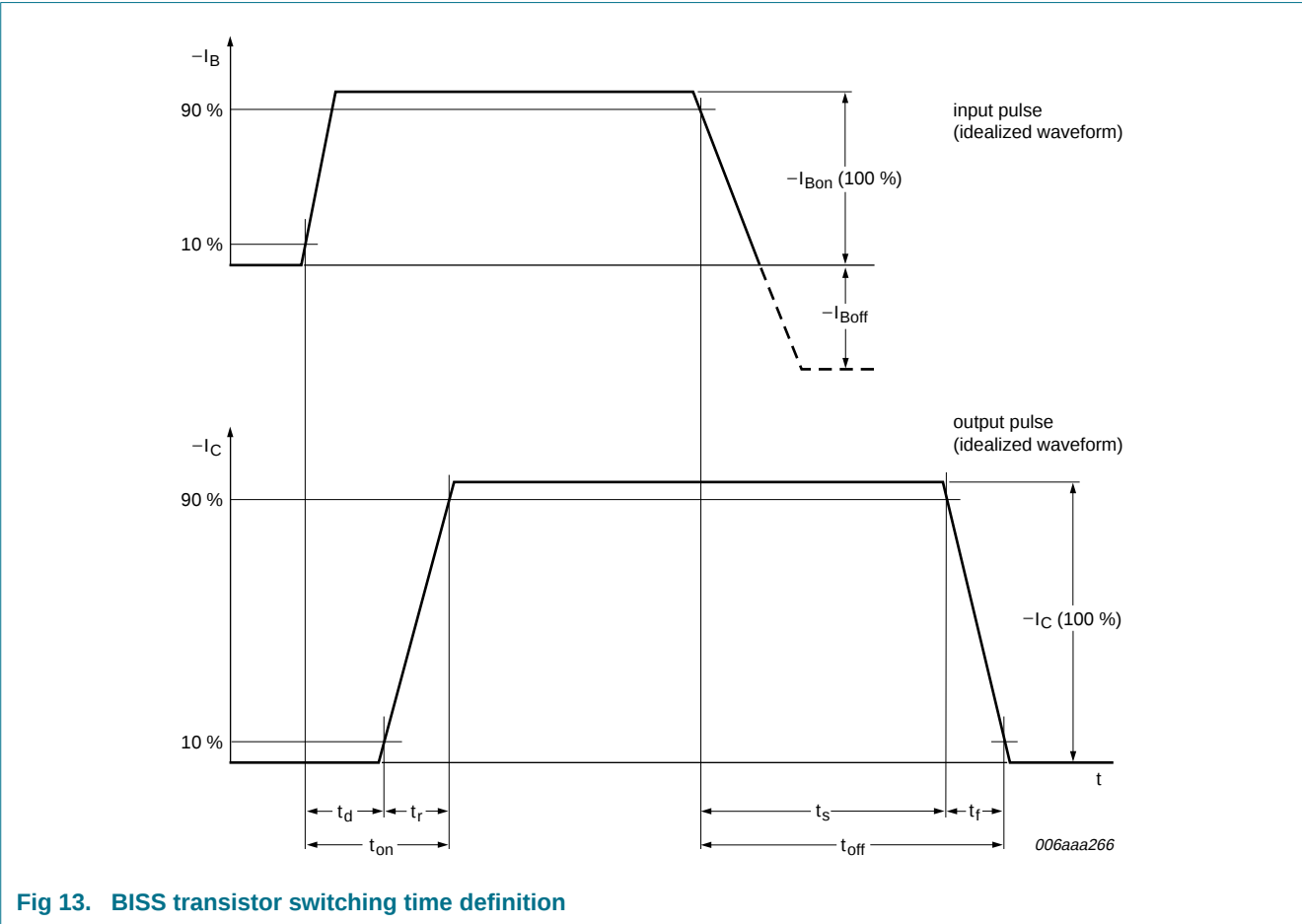
Fig 11. Collector-emitter saturation resistance as a function of collector current; typical values



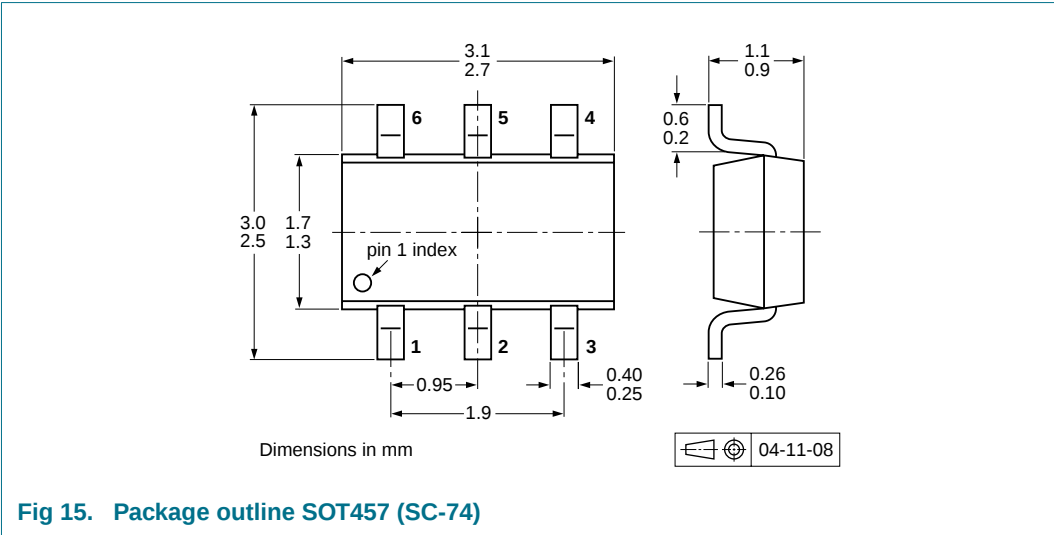
- $T_{amb} = 25^\circ C$
- (1) $I_C/I_B = 100$
 - (2) $I_C/I_B = 50$
 - (3) $I_C/I_B = 10$

Fig 12. Collector-emitter saturation resistance as a function of collector current; typical values

8. Test information



9. Package outline



10. Packing information

Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PBSS5420D	SOT457	4 mm pitch, 8 mm tape and reel; T1	^[2] -115	-135
		4 mm pitch, 8 mm tape and reel; T2	^[3] -125	-165

[1] For further information and the availability of packing methods, see [Section 14](#).

[2] T1: normal taping

[3] T2: reverse taping

11. Soldering

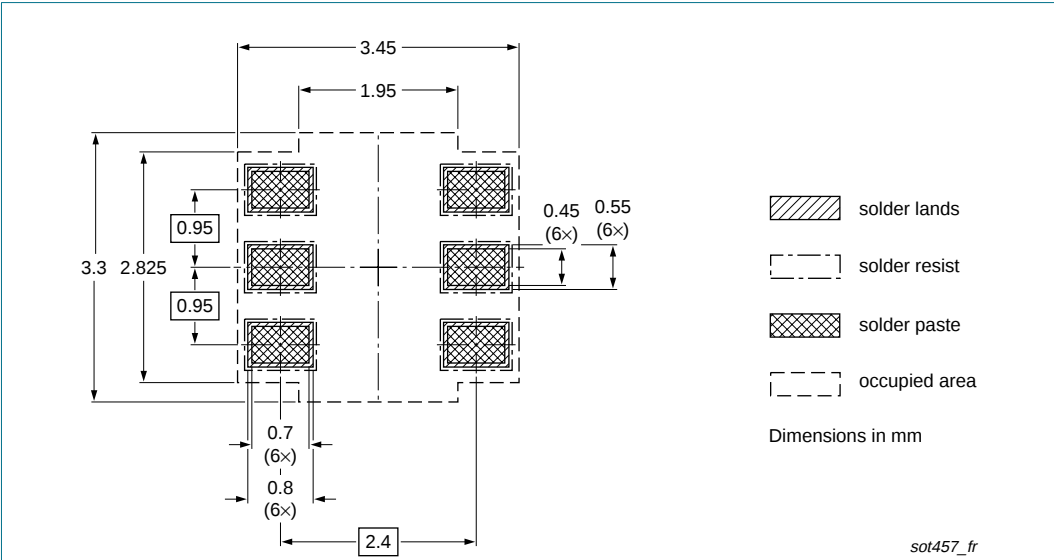


Fig 16. Reflow soldering footprint SOT457 (SC-74)

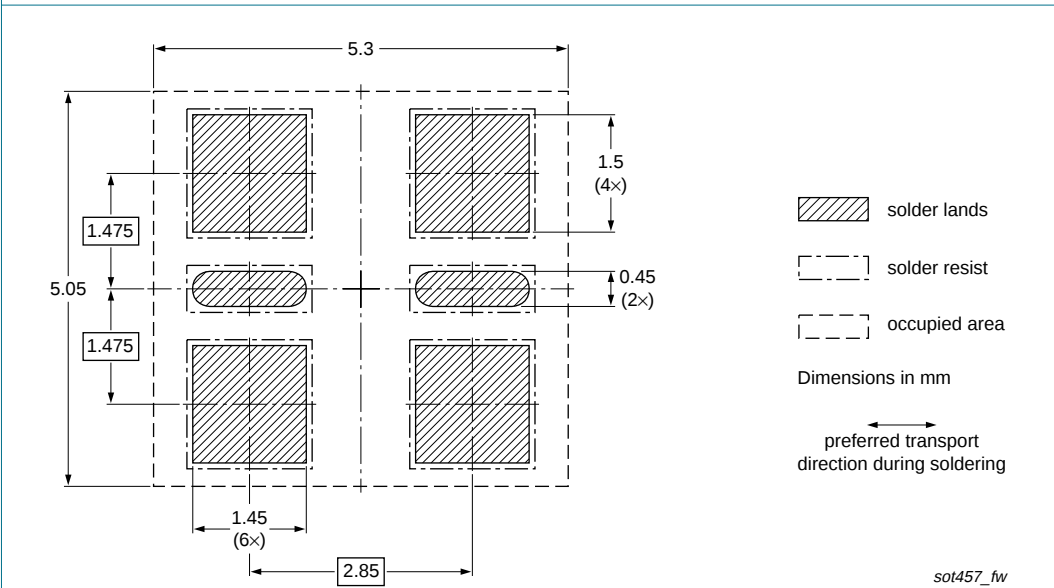


Fig 17. Wave soldering footprint SOT457 (SC-74)

12. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS5420D_2	20080929	Product data sheet	-	PBSS5420D_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Figure 7: amended • Section 11 "Soldering": added • Section 13 "Legal information": updated			
PBSS5420D_1	20050407	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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