Advance Information

PBL 387 72/1

Subscriber Line Interface Circuit

Key Features

- On-chip high voltage ring generation
  - Balanced, up to 80 V_{Peak}
  - Any ring waveform
  - 5 REN ringing load
  - Short circuit safe
  - Automatic gain control of ringing signal
- Low on-hook power consumption in Active State (65mW @ V_{Bat}=-80V)
- Automatic switching between ringing battery (V_{Bat}) and talk battery (V_{TBat})
- Only +5V and Battery supplies needed
- Pulse metering and on-hook transmission
- UL-1950 and MTU compliant on-hook line voltage
- Programmable ring trip threshold
- 3.3V compatible logic interface
- Silent or fast polarity reversal
- 28-pin SOIC package

Applications

- Cable modems
- Voice over DSL (VoDSL)
- Terminal adapters
- ISDN Terminal adapters (NT1+)
- Voice over IP (VoIP)
- Routers
- Integrated Access Devices (IAD)
- Other short loop applications

Description

The PBL 387 72/1 Subscriber Line Interface Circuit (SLIC) is a 90 V bipolar integrated circuit with on-chip high voltage ring generation for use in short loop applications. The PBL 387 72/1 SLIC has been optimized for low power consumption, low total line interface cost and for a high degree of flexibility meeting worldwide requirements.

The PBL 387 72/1 SLIC supplies a balanced ringing signal of any waveform (e.g. sinewave, trapezoidal, etc.)

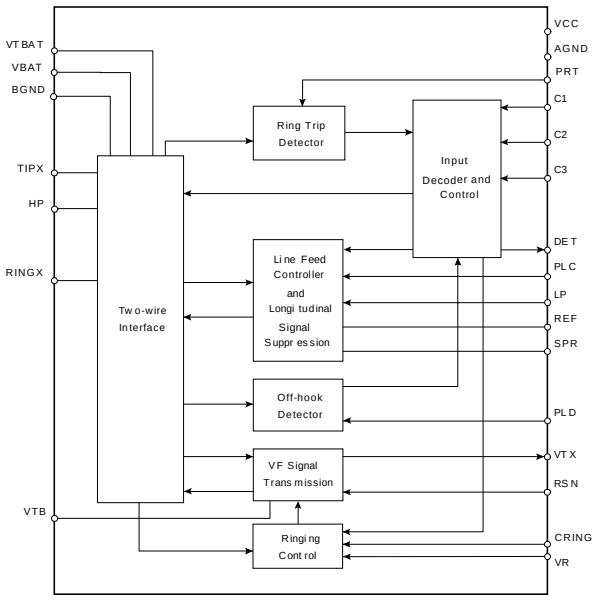


Figure 1. Block diagram

up to 80 V_{Peak} (85 V dc supply) to the subscriber line across a load of up to 5REN

The PBL 387 72/1 supplies programmable constant current to the subscriber loop, sourced from the talk battery. The on-hook line voltage of 43 V to 56 V is derived from the ring battery. All battery switching is internal to the device and is automatic.

To further reduce power consumption the automatic gain control for the ring signal (AGCR) keeps the level always adjusted to the maximum, that can be sourced from the available dc ringing battery.

The SLIC incorporates loop current, ground key and ring trip detection functions. The PBL 387 72/1 is compatible with loop start signaling.

Two- to four-wire and four- to two-wire voice frequency (vf) signal conversion is accomplished by the SLIC in conjunction with any standard codec.

The line terminating impedance and balance impedance is programmable (via hardware or software) and may be complex or real for worldwide compliance.

Tip and ring voltages are UL-1950 compliant, i.e. no two-wire line voltage exceeds 56 V.

The PBL 387 72/1 SLIC is available in a surface mount 28 SOIC package.

Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature, Humidity				
Storage temperature range	T_{Stg}	-55	+150	°C
Operating temperature range	T_{Amb}	-40	+110	°C
Operating junction temperature range, Note 1	T_J	-40	+140	°C
Power supply, -40°C ≤ T_{Amb} ≤ +85°C				
V_{CC} with respect to AGND	V_{CC}	-0.4	6.5	V
V_{TBat} with respect to A/BGND	V_{TBat}	V_{Bat}	0.4	V
V_{Bat} with respect to BGND, continuous	V_{Bat}	-85	0.4	V
Power dissipation				
Continuous power dissipation at T_{Amb} ≤ +85 °C	P_D		TBD	W
Ground				
Voltage between AGND and BGND	V_G	-5	V_{CC}	V
Digital inputs, outputs (C1, C2, C3, DET)				
Input voltage	V_{ID}	-0.4	V_{CC}	V
Output voltage (DET not active)	V_{OD}	-0.4	V_{CC}	V
Output current (DET)	I_{OD}		30	mA
TIPX and RINGX terminals, -40°C < T_{Amb} < +85°C, V_{Bat} = -80 V				
TIPX or RINGX current	I_{TIPX}, I_{RINGX}	-100	+100	mA
TIPX or RINGX voltage, continuous (referenced to AGND)	V_{TA}, V_{RA}	V_{Bat}	2	V
TIPX or RINGX, pulse < 10 ms, t_{Rep} > 10 s, Note 2	V_{TA}, V_{RA}	V_{Bat} -5	5	V
TIPX or RINGX, pulse < 1 µs, t_{Rep} > 10 s, Note 2	V_{TA}, V_{RA}	V_{Bat} -25	10	V
TIP or RING, pulse < 250 ns, t_{Rep} > 10 s, Note 2	V_{TA}, V_{RA}	V_{Bat} -35	15	V

Recommended Operating Condition

Parameter	Symbol	Min	Max	Unit
Ambient temperature	T_{Amb}	-40	+85	°C
V_{CC} with respect to AGND	V_{CC}	4.75	5.25	V
V_{TBat} with respect to BGND	V_{TBat}	V_{Bat}	-10	V
V_{Bat} with respect to BGND	V_{Bat}	-80	-10	V

Notes, Maximum Ratings

1. The circuit includes thermal protection. Operation above maximum junction temperature may degrade device reliability.
2. With the diodes D_B and D_{TB} included, see figure 8.

Electrical Characteristics

-40 °C ≤ T_{Amb} ≤ +85 °C, V_{CC} = +5 V ±5 %, V_{TBat} = -32 V to –10 V, V_{Bat} = -80 V, R_{LC}= 18.7 kΩ, (I_L = 27 mA), Z_L = 600 Ω, R_{LD} = 50 kΩ, R_{F1} = R_{F2} = 0 Ω, R_{Ref} = 15.0 kΩ, C_{HP} = 33 nF, C_{LP}= 0.47 µF, R_T = 120 kΩ, R_{RX} = 120 kΩ. Current definition: current is positive if flowing into a pin unless stated otherwise. 'Active state' includes 'Active, reverse polarity state' unless otherwise specified.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Two-wire port						
Overload level, V_{TRO}	2	Active state				
Off-Hook, I_{Ldc} ≥ 10 mA		1% THD, Note 1		1.0		V_{Peak}
On-Hook, I_{Ldc} ≤ 5 mA				1.0		V_{Peak}
Metering, I_{Ldc} ≥ 10 mA		Z_{LM} = 200 Ω, f = 16 kHz		0.7		V_{Peak}
Input impedance, Z_{TRX}		Note 2		Z_T/200		
Longitudinal impedance, Z_{IoT}, Z_{LoR}		0 < f < 100 Hz		20	35	Ω/wire
Longitudinal current limit, I_{IoT}, I_{LoR}		Active state	28			mA_{rms}/wire
Longitudinal to metallic balance, B_{LM}	3	IEEE standard 455-1985, R_{LT}=R_{LR} = 368 Ω				
		0.2 kHz < f < 1.0 kHz	53	70		dB
		1.0 kHz < f < 3.4 kHz	53	70		dB
Longitudinal to metallic balance, B_{LME}	3	R_{LT}=R_{LR} = 300 Ω				
$B_{LME} = 20 \cdot \log \lvert \frac{E_{Lo}}{V_{TR}} \rvert$	3	Active state				
		0.2 kHz ≤ f ≤ 1.0 kHz	53	70		dB
		1.0 kHz < f < 3.4 kHz	53	70		dB
Longitudinal to four-wire balance, B_{LFE}	3	Active state				
$B_{LFE} = 20 \cdot \log \lvert \frac{E_{Lo}}{V_{TX}} \rvert$		0.2 kHz ≤ f ≤ 1.0 kHz	59	70		dB
		1.0 kHz < f < 3.4 kHz	59	70		dB

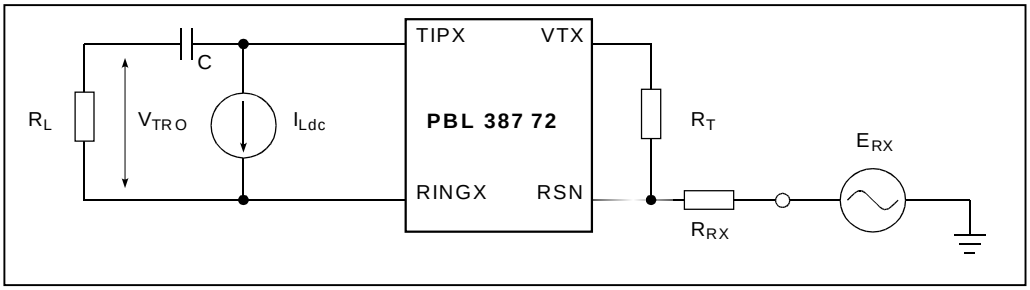


Figure 2. Overload level, V_{TRO}, two-wire port

$$\frac{1}{\omega C} << R_L, R_L = 600\Omega$$

R_T = 120 kΩ, R_{RX} = 120 kΩ

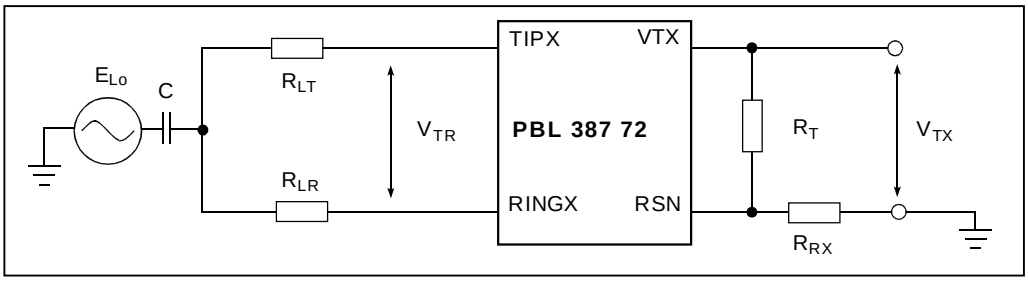


Figure 3. Longitudinal to metallic, B_{LM}, B_{LME} and Longitudinal to four-wire, B_{LFE} balance

$$\frac{1}{\omega C} << 150\Omega, R_{LR} = R_{LT} = 300\Omega$$

or 368Ω

R_T = 120 kΩ, R_{RX} = 120 kΩ

Advance Information

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire to longitudinal balance, B_{FLE}	4	Active state				
$B_{FLE} = 20 \bullet \text{Log}\left\lvert\frac{E_{RX}}{V_{LO}}\right\rvert$		0.2 kHz ≤ f ≤ 3.4 kHz	40	58		dB
Two-wire return loss, r						
$r = 20 \bullet \text{Log}\frac{\lvert Z_{TRX} + Z_L\rvert}{\lvert Z_{TRX} - Z_L\rvert}$		0.2 kHz < f < 0.5 kHz	25			dB
		0.5 kHz < f < 1.0 kHz	27			dB
		1.0 kHz < f < 3.4 kHz, Note 3	23			dB
TIPX idle voltage, V_{Ti}		Active normal, I_L = 0		-1.0		V
RINGX idle voltage, V_{Ri}		Active normal, I_L = 0	-44	-51	-56	V
Open loop voltage, $\lvert V_{TROpen}\rvert$		Active, I_L = 0	43		55	V
Four-wire transmit port (output VTX)						
Overload level, V_{TXO}	5	Off-hook, I_{Ldc} ≥ 10mA				
		Load impedance > 20 kΩ, 0.5				V_{Peak}
		On-hook, I_{Ldc} ≤ 5mA				
		Load impedance > 20 kΩ,0	.5			V_{Peak}
		1% THD, Note 4				
Output offset voltage, ΔV_{TX}			-60	0	60	mV
Output impedance, z_{TX}		0.2 kHz < f < 3.4 kHz		5	20	Ω
Output dc voltage, V_{TXdc}				0V		
Four-wire receive port (RSN, receive summing node)						
RSN dc voltage, V_{RSNdc}		I_{RSN} = 0 mA	-25	GND	+25	mV
RSN impedance		0.2 kHz < f < 3.4 kHz		10	50	Ω
RSN current, I_{RSN}, to metallic loop current ,I_L, gain, α_{RSN}		0.3 kHz < f < 3.4 kHz		400		ratio

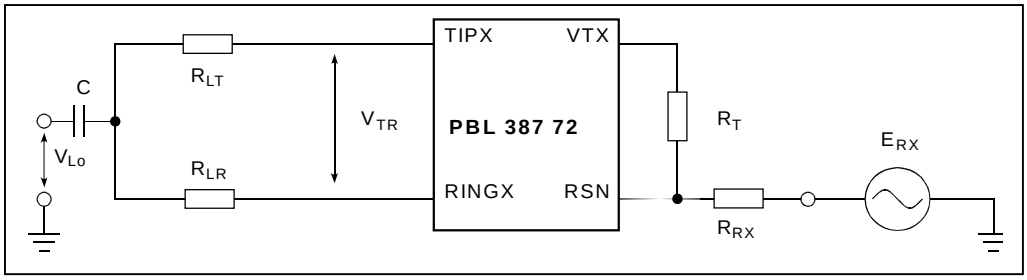


Figure 4. Four-wire to longitudinal, B_{FLE} balance

$\frac{1}{\omega C} << 150\Omega, R_{LR} = R_{LT} = 300\Omega$

R_T = 120 kΩ, R_{RX} = 120 kΩ

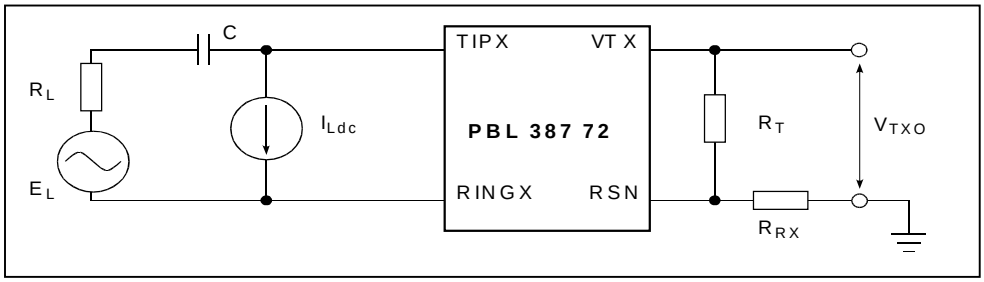


Figure 5. Overload level, V_{TXO}, four-wire transmit port

$\frac{1}{\omega C} << R_L, R_L = 600\Omega$

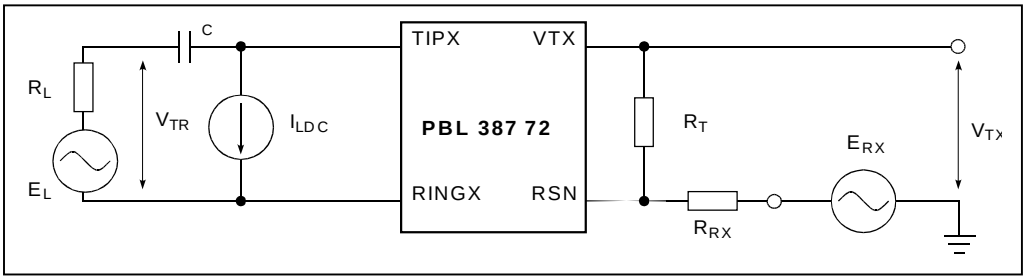
R_T = 120 kΩ, R_{RX} = 120 kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Frequency response						
Two-wire to four-wire, g_{2-4}	6	Relative to 0 dBm, 1.0 kHz. E_{RX} = 0 V				
		0.3 kHz < f < 3.4 kHz	-0.15		0.15	dB
		f = 8.0 kHz, 12 kHz, 16 kHz	-0.5	-0.1	0.1	dB
Four-wire to two-wire, g_{4-2}	6	Relative to 0 dBm, 1.0 kHz. E_L = 0 V				
		0.3 kHz < f < 3.4 kHz	-0.15		0.15	dB
		f = 8 kHz, 12 kHz,	-1.0	-0.2	0	dB
		f = 16 kHz	-1.0	-0.3	0	dB
Four-wire to four-wire, g_{4-4}		Relative to 0 dBm, 1.0 kHz. E_L = 0 V				
		0.3 kHz < f < 3.4 kHz	-0.15		0.15	dB
Insertion loss						
Two-wire to four-wire, G_{2-4}	6	0 dBm, 1.0 kHz, Note 5	-6.22	-6.02	-5.82	dB
		$G_{2-4} = 20 \bullet \mathrm{Log}\left\lvert \frac{V_{TX}}{V_{TR}} \right\rvert$, $E_{RX} = 0$				
Four-wire to two-wire, G_{4-2}	6	0 dBm, 1.0 kHz, Notes 5, 6	-0.2		0.2	dB
		$G_{4-2} = 20 \bullet \mathrm{Log}\left\lvert \frac{V_{TR}}{E_{RX}} \right\rvert$, $E_L = 0$				
Gain tracking						
Two-wire to four-wire	6	Ref. -10 dBm, 1.0 kHz, Note 7 $R_{LDC} \leq 2k\Omega$				
		-40 dBm to +3 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Four-wire to two-wire	6	Ref. -10 dBm, 1.0 kHz, Note 7 $R_{LDC} \leq 2k\Omega$				
		-40 dBm to +3 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Noise						
Idle channel noise at two-wire port (TIPX-RINGX)		C-message weighting		5	12	dBrnC
		Psophometrical weighting Note 8		-85	-78	dBmp
Harmonic distortion						
Two-wire to four-wire	6	0 dBm, 1.0 kHz test signal			-50	dB
Four-wire to two-wire		0.3 kHz < f < 3.4 kHz			-50	dB

Figure 6. Frequency response, insertion loss, gain tracking.

$\frac{1}{\omega C} << R_L, R_L = 600\Omega$

R_T = 120 kΩ, R_{RX} = 120 kΩ



Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Ring signal input, VR						
Bias current, I_{VRdc}		+1 V < V_{Rdc} < -1 V, R_{VR} = 200 kΩ	0	4	15	nA
Bias voltage, V_{VRdc}		R_{VR} = 200 kΩ		0		V
Input impedance, $\lvert z_R \rvert$		0 Hz < f_R < 100 Hz, R_{VR} = ∞ Ω		20		MΩ
Gain, VR to TIPX-RINGX, G_{R-2}		Z_L = 8 kΩ, f = 20 Hz, V_R = 0.6 V_{pk} Note 9		109		ratio
Battery feed characteristics						
Constant loop current, I_{LConst}		$R_{LC} = \frac{500}{I_{LProg}} - \frac{10.4 \bullet \ln(32 \bullet 10^{-3} \bullet I_{LProg})}{I_{LProg}}$ 18 < I_{LProg} < 30 mA	0.95 I_{LProg}	I_{LProg}	1.05 I_{LProg}	mA
Loop current detector						
Programmable threshold, I_{LTh}		$I_{LTh} = \frac{500}{R_{LD}}$, I_{LTh} > 10 mA	0.9•I_{LTh}	I_{LTh}	1.1•I_{LTh}	mA
Ring trip detector						
Programmable threshold, I_{LTh}		$I_{LTh} = \frac{4000}{R_{RT}}$, I_{LTh} > 10 mA	0.9•I_{LTh}	I_{LTh}	1.1•I_{LTh}	mA
Ground key detector						
Ground key detector threshold I_{LTIPX} and I_{LRINGX} current difference to trigger ground key det.			11	15	19	mA
Digital inputs (C1, C2, C3)						
Input low voltage, V_{IL}			0		0.5	V
Input high voltage, V_{IH}			2.5		V_{CC}	V
Input low current, $\lvert I_{IL} \rvert$		V_{IL} = 0.5			200	µA
Input high current, I_{IH}		V_{IH} = 2.5 V			200	µA
Detector output (DET)						
Output low voltage, V_{OL}		I_{OL} = 1 mA	0.1	0.6		V
Internal pull-up resistor to V_{CC}				10		kΩ
Power dissipation (V_{TB}= -24V, V_{bat}=-80V)						
P_1		Open circuit state		16		mW
		Active state				
P_2		Longitudinal current = 0 mA, I_L = 0 mA		65		mW
P_3		R_L = 300Ω (off-hook)		0.50		W
P_4		R_L = 600Ω (off-hook)		0.29		W
		Ringing state				
P_5		R_L = 7kΩ (ac load ≈ 1 bell), I_{Ldc} = 0 mA Ringing: sine, 20 Hz, max. amplitude		0.36		W
Power supply currents (V_{TB}= -24V, V_{bat}=-80V)						
V_{CC} current, I_{CC}		Open circuit state		1.4		mA
V_{TBat} current, I_{TBat}		Open circuit state		0		mA
V_{Bat} current, I_{Bat}		Open circuit state		-0.07		mA
V_{TB} current, I_{TB}		Open circuit state		-0.13		mA
V_{CC} current, I_{CC}		Active state, On-hook		2.4		mA
V_{TBat} current, I_{TBat}		Active state, On-hook		0		mA
V_{Bat} current, I_{Bat}		Active state, On-hook		-0.6		mA
V_{TB} current, I_{TB}		Active state, On-hook		-0.2		mA
V_{CC} current, I_{CC}		Ringing state, On-hook, No ring signal		7.1		mA
V_{TBat} current, I_{TBat}		Ringing state, On-hook, No ring signal		0		mA
V_{Bat} current, I_{Bat}		Ringing state, On-hook, No ring signal		-2.7		mA
V_{TB} current, I_{TB}		Ringing state, On-hook, No ring signal		-1		mA

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Power supply rejection ratios						
V_{CC} to 2- or 4-wire port		Active State f = 1 kHz, V_n = 100 mV		TBD		dB
V_{TBat} to 2- or 4-wire port		Active State f = 1 kHz, V_n = 100 mV		TBD		dB
V_{Bat} to 2- or 4-wire port		Active State f = 1 kHz, V_n = 100 mV		TBD		dB
Temperature guard						
Junction threshold temperature, T_{JG}				150		°C
Thermal Resistance						
Junction to pins, Θ_{JA} , Note 10				50		°C/W
Junction to pins, Θ_{JP}				30		°C/W

Notes, Electrical Characteristics

1. The overload level is automatically expanded to 3 V_{Peak} when the signal level is > 1.0 V_{Peak} and is specified at the two-wire port with the signal source at the four-wire receive port.
2. The two-wire impedance is programmable by selection of external component values according to:
   $Z_{TRX} = Z_T/(G_{2\text{-}4S} \bullet \alpha_{RSN})$
   where:
   Z_{TRX} = impedance between the TIPX and RINGX terminals
   Z_T = programming network between the VTX and RSN terminals
   $G_{2\text{-}4S}$ = transmit gain, nominally = 0.5
   α_{RSN} = receive summing node current gain, nominally = 400. α_{RSN} is the ratio between the current flowing from RINGX to TIPX and the current flowing into the RSN pin (current is defined as positive flowing into the receive summing node, RSN and when flowing from RINGX to TIPX).
3. Higher return loss values can be achieved by adding a reactive component to R_T, the two-wire terminating impedance programming resistance, e.g. by dividing R_T into two equal halves and connecting a capacitor from the common point to ground.
4. The overload level is automatically expanded as needed up to 1.5 V_{Peak} when the signal level >0.5 V_{Peak} and is specified at the four-wire transmit port, VTX, with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is $G_{2\text{-}4S}$ = 0.5.
5. Secondary protection resistors R_{F1} and R_{F2} impact the insertion loss (refer to section Functional Description and Application Information). The specified insertion loss is for $R_{F1} = R_{F2} = 0$.
6. The specified insertion loss tolerance does not include errors caused by external components.
7. The level is specified at the four-wire receive port (E_{RX}, Figure 6) and referenced to a 600 Ω impedance level.
8. The two-wire idle noise is specified with the four-wire receive port grounded (E_{RX} = 0, Figure 6).
   The four-wire idle noise at VTX is the two-wire value reduced by 6 dB and is specified with the two-wire port terminated in 600 Ω (R_L). The VTX noise specification is referenced to a 600 Ω impedance level.
9. AGCR, Automatic Gain Control Ringing, is not activated with a signal level as low as 0.6 V_{Peak}.
10. Junction to ambient thermal resistance is dependent on PCB layout and many others factors external to the PBL 387 72/1 device.

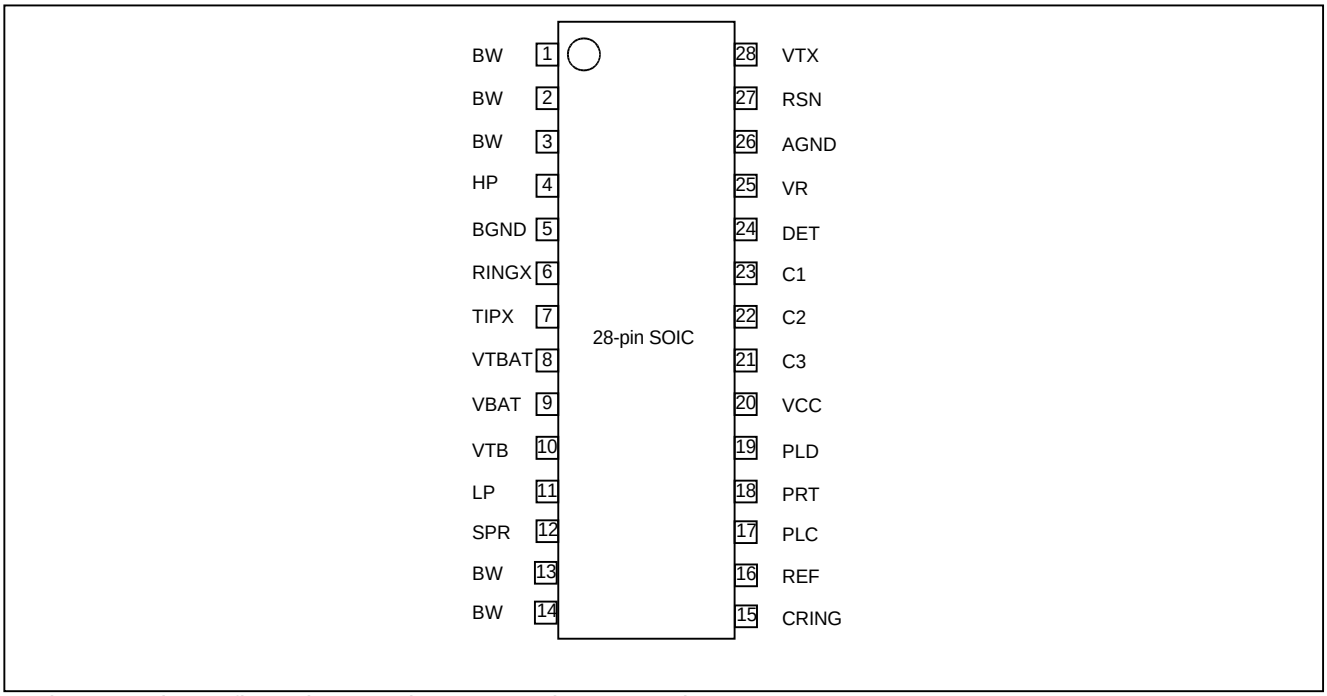


Figure 7. Pin configuration, 28 pin SOIC package, top view

SLIC Operating States

State	C3	C2	C1	SLIC Operating State	Active detector (DET response)
0	0	0	0	TIPX and RINGX open circuit	No active detector (DET is set high)
1	0	0	1	Ringing	Ring trip detector (DET active low)
2010A				ctive	Loop current detector (DET active low)
3011A				ctive, Test of line voltage	Loop voltage measurement (DET pulse train)
4100N				ot applicable	
5101A				ctive, Ground Key, Ground fault test	Ground key detector and loop ground fault detector (DET active high)
6110A				ctive, Reverse polarity	Loop current detector (DET active low)
7111A				ctive Rev polarity, Ground fault test	Loop ground fault detector (DET active high)

Table 1. SLIC operating states.

Pin Description

28L SOIC	Symbol	Description
1B	W	**B**at**w**ing (Note 1)
2B	W	**B**at**w**ing (Note 1)
3B	W	**B**at**w**ing (Note 1)
4H	P	**H**igh **P**ass ac/dc separation capacitor, C_{HP}, connects between this pin and TIPX.
5B	GND	**B**attery **G**rou**nd**. Shall be tied together with AGND.
6	RINGX	The TIPX and RINGX pins connect to the tip and ring leads of the two-wire interface via over voltage protection components (and optional test access switch).
7	TIPX	The TIPX and RINGX pins connect to the tip and ring leads of the two-wire interface via over voltage protection components (and optional test access switch).
8	VTBAT	**T**alk **Bat**tery. The dc loop current is supplied to TIPX and RINGX from this battery voltage. Negative with respect to BGND.
9V	BAT	Ringing **Bat**tery supply voltage. Negative with respect to BGND.
10	VTB	Internal SLIC bias voltage. Connected to the talk battery supply. Refer to the application diagram in Figure 8. May be connected to any voltage between VTB and –5 V.
11	LP	**L**ow **P**ass saturation guard filter capacitor, C_{LP}, connects between this pin and VBAT to filter out noise and improve PSRR.
12	SPR	**S**ilent **P**olarity **R**eversal. The polarity reversal time can be set with a capacitor connected between this pin and AGND.
13	BW	**B**at**w**ing (Note 1)
14	BW	**B**at**w**ing (Note 1)
15	CRING	C_{Ring} connects between this pin and AGND. Required for the ring signal generation.
16	REF	A 15 kΩ resistor connected between this pin and AGND sets an internal SLIC reference current. The value must not be changed.
17	PLC	**P**rogrammable **L**ine **C**urrent. The constant current dc feed is programmed by a resistor, R_{LC}, connected from this pin to AGND.
18	PRT	**P**rogrammable **R**ing **T**rip Resistor, R_{RT}, connected between this pin and AGND. Sets
the		ring trip threshold.
19	PLD	**P**rogrammable **L**oop **D**etector threshold. The loop detection threshold is programmed by a resistor, R_{LD}, connected between this pin and AGND.
20	VCC	+5 V power supply.
21	C3	C1, C2, C3 are digital inputs, which **c**ontrol the SLIC operating
22	C2	states. Refer to Table 1, SLIC Operating States.
23 C1		
24	DET	**Det**ector output. Active low when indicating loop or ring trip detection, active high when indicating ground key detection.
25	VR	Low voltage **r**ing signal input. Reference to ground.
26	AGND	**A**nalog **G**rou**nd**, shall be tied together with BGND.
27	RSN	**R**eceive **S**umming **N**ode. 400 times the current flowing into this pin equals the metallic (transversal) current flowing from RINGX to TIPX. Programming networks for two-wire impedance and receive gain connect to the receive summing node.
28	VTX	**T**ransmit vf output. The ac voltage difference between TIPX and RINGX, the ac metallic voltage, is reproduced as an unbalanced GND referenced signal at VTX with a gain of 0.5. The two-wire impedance-programming network connects between VTX and RSN.

Notes

1. A batwing is a package pin, which provides a low thermal resistance path to the silicon chip via the lead frame. By soldering the batwing pins to PCB copper foil the device can be efficiently cooled. Note that batwing pins are at the same voltage as the VBAT pin (substrate voltage).

Functional Description and Applications Information

Introduction

The Figure 8. diagram shows the PBL 387 72/1 in a typical application with a non-programmable, Combo I, codec. The PBL 387 72/1 can equally well be used with software programmable codecs.

The component values chosen for the application diagram example yield a two-wire impedance of 600 Ω, resistive. The balance resistor is calculated for a line impedance, Z_L (compromise impedance), of 600 Ω, resistive. The two-wire to four-wire gain is set by R_{TX} and R_{FB} to produce the digital mW level at the PCM transmit bus for a signal level of +3 dBm applied to the two-wire input (TIP and RING). A received digital mW at the PCM receive bus results in a –3 dBm signal level across the compromise impedance (600 Ω) connected at the two-wire port (TIP and RING). The gain calculations are based on National Semiconductor combo I codec, TP 3054.

R_{F1}, R_{F2} and the clamp “OVP” make up the overvoltage protection network.
C_{TC} and C_{RC} clamp fast transients that may bypass the OVP clamp and also filter high frequency interference (RFI filter).
C_{HP} and C_{LP} are coupling capacitors within two SLIC feedback loops that control SLIC battery feed and SLIC voice frequency transmission.
C_{TB}, C_B, C_{VCC} are power supply bypass capacitors.
D_{TB} is a diode that is part of the battery switching function.
D_B prevents reverse currents from the VB supply rail during application of negative over voltages.
D_{BB} is normally reverse biased, but conducts supply VTB to the VBAT terminal in case the voltage VB would fail.
R_T sets the two-wire impedance (note that R_T may be replaced with a complex impedance, Z_T, to implement complex terminating impedance).
The ratio between R_{FB} and R_{TX} sets the transmit gain.
R_{RX} sets the receive gain.
R_{LD} sets the loop current detector threshold.
R_{LC} sets the constant dc loop current.
R_{REF} sets a SLIC reference current (must be 15.0 kΩ, 1%, as specified).
R_{RT} sets the ring trip loop current detector threshold.
C_{RING} is used for the high voltage ringing signal AGC (automatic gain control) function.
V_{TB} is the talk battery supply, i.e. the negative supply voltage that sources the loop current.
V_B is the ringing battery, i.e. the negative supply voltage that is used to power the SLIC, while ringing the line.

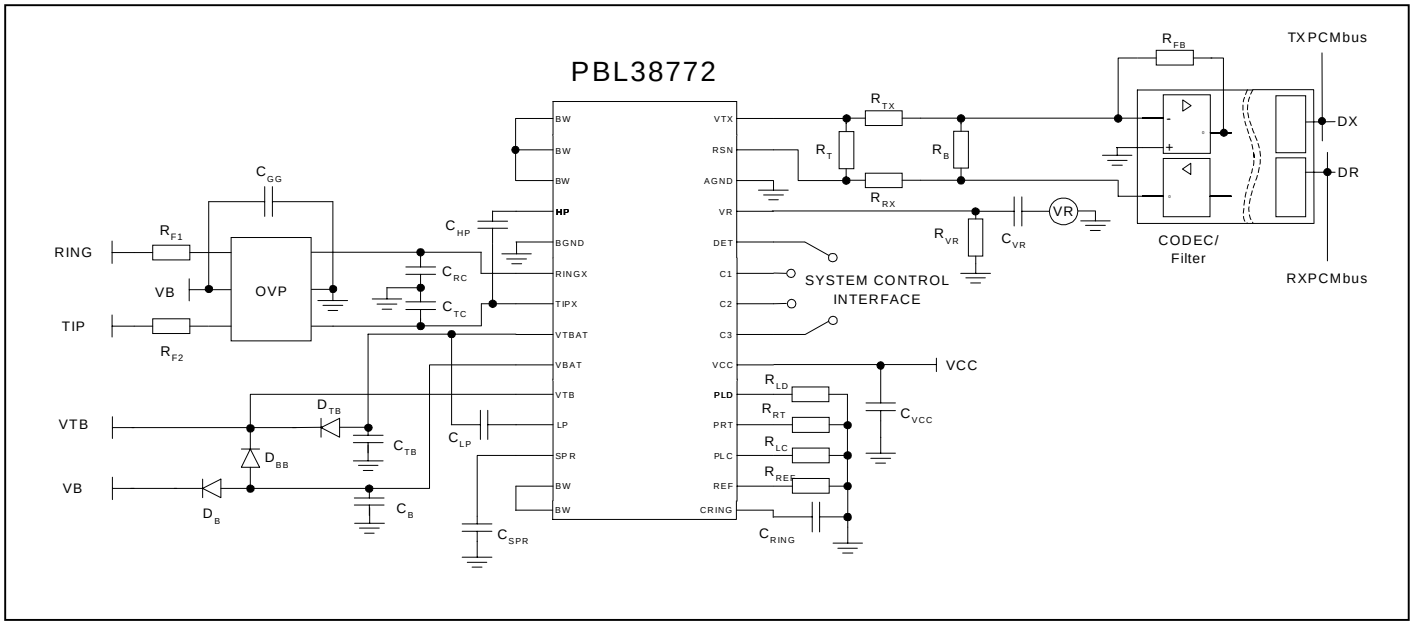


Figure 8. Single channel subscriber line interface with PBL 387 72/1 and Combo I type codec.

RESISTORS:
(values according to IEC-63 E96 series)
R_{LD} = 49.9 kΩ 1% 1/10 W
R_{LC} = 18.7 kΩ 1% 1/10 W
R_{RT} = 69.8 kΩ 1% 1/10 W
R_{REF} = 15.0 kΩ 1% 1/10 W
R_{RX} = 232 kΩ 1% 1/10 W
R_{VR} = 200 kΩ 1% 1/10 W
R_{TX} = 28.0 kΩ 1% 1/10 W
R_T = 104 kΩ 1% 1/10 W
R_{FB} = 73.2 kΩ 1% 1/10 W
R_B = 110 kΩ 1% 1/10 W
R_{F1}=R_{F2}=4 0 Ω 1% match,
Line protection resistor.

CAPACITORS:
(values according to IEC-63 E6 series)
C_{TB} = 150nF 100 V 20%
C_B = 100nF 100 V 20%
C_{VCC} = 100nF 10 V 20%
C_{TC} = 1.0nF 100 V 20%
C_{RC} = 1.0nF 100 V 20%
C_{HP} = 33nF 100 V 20%
C_{LP} = 470nF 100 V 20%
C_{GG} = 220nF 100 V 20%
C_{RING} = 470nF 10 V 20%
C_{VR} = 0.33µF 10 V 20%
C_{SPR} = optional 10 V 20%

DIODES:
D_B = D_{TB} = D_{BB} =1N4448

OVP:
Secondary protection clamp (e g Bourns/Power Innovations TISP PBL3, which serves two lines). The ground terminals of the secondary protection should be connected to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferably to a ground plane.

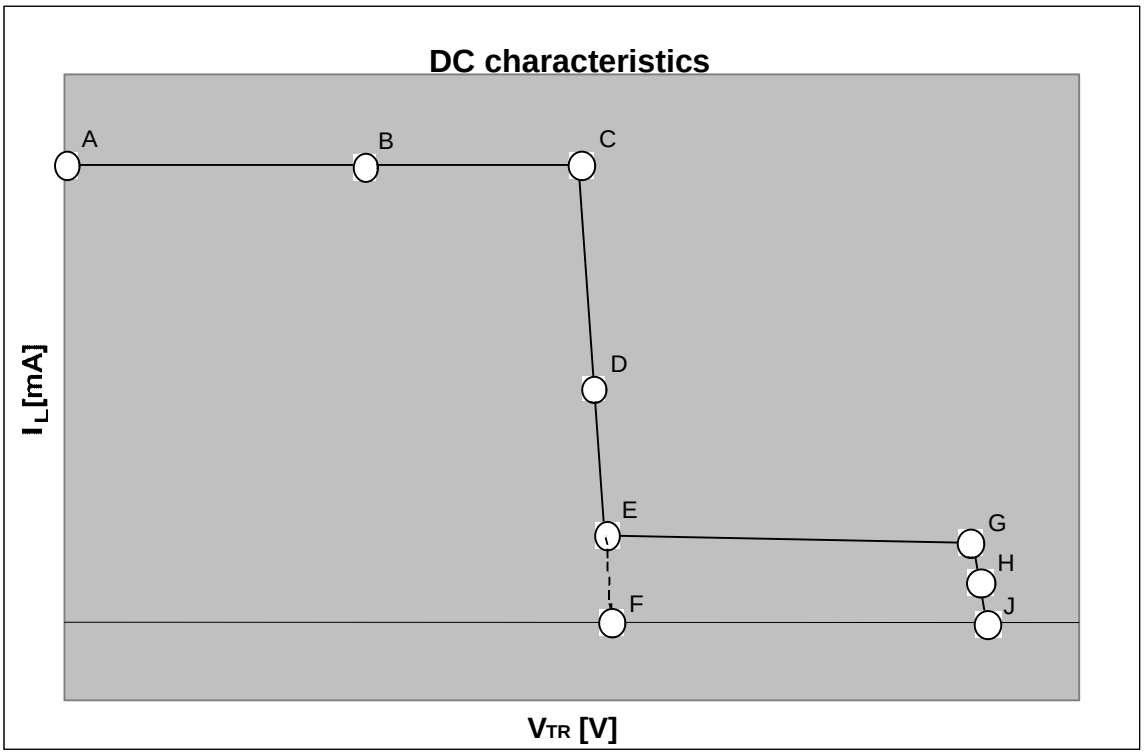


Figure 9. Battery feed characteristic

A: $I_L(@V_{TR}=0) = I_{Lconst} = I_{Lprog}$ $\quad R_{LC} = \frac{500}{I_{Lprog}} - \frac{10.4 \bullet \ln(32 \bullet 10^{-3} \bullet I_{Lprog})}{I_{Lprog}}$ (Note: I_L in mA and R_{LC} in kΩ)

B,C: $I_L = I_{Lconst}$, $V_{TR}(@C) = V_{App} - R_{FEED} \bullet I_{Lprog}$

D: $R_{FEED} = 2 \bullet 25\ \Omega$

E: $I_L \approx 5.5$mA , $V_{TR} = V_{App} - R_{FEED} \bullet 5.5$ mA

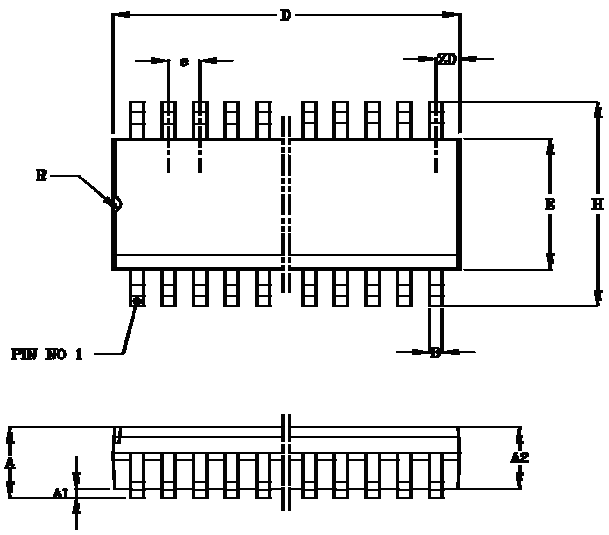
F: $V_{App}(@I_L=0) = V_{TB} - V_F^* - 4.2V$ $\quad ^*V_F$ forward voltage of diode D_{TB}

G: $I_L \approx 5$mA

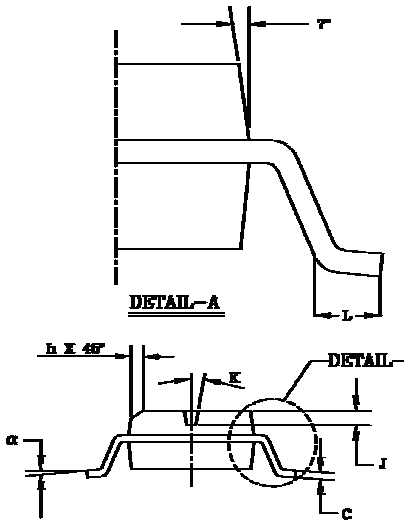
H: $R_{FEED} = 2 \bullet 25\ \Omega$

J: $|V_{TROpen}| \leq 56$ V limited by the SLIC @ $I_L = 0$ mA (open loop voltage)
if V_{BAT} less than 56 V the $V_{TROpen} = |V_{BAT}| - 4.6V$

Mechanical drawing 28 SOIC



SYMBOL	SOIC-28LD	
	MILLIMETERS	
	MIN	MAX
A	2.44	2.64
A1	0.10	0.30
A2	2.24	2.44
B	0.36	0.46
C	0.23	0.32
D	17.73	17.93
E	7.40	7.60
e	1.27 BSC	
H	10.11	10.51
h	0.31	0.71
J	0.53	0.73
K	7° BSC	
L	0.51	1.01
R	0.63	0.89
ZD	0.66 REF	
α	0°	8°



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