PBL 387 10/1 Subscriber Line Interface Circuit

Description

The PBL 387 10/1 ring SLIC (Subscriber Line Interface Circuit) is a bipolar integrated circuit in 90 V technology which replaces the conventional transformer based analog line interface and ringrelay in FITL, WLL, ISDN-TA and other telecommunications equipment with a modern, compact solid state design. Not only is required PCB area reduced, but less component weight and height result as well. The PBL 387 10/1 has been optimized for low cost and to require only a minimum of external components.

The PBL 387 10/1 constant-current feed system, programmable to max 40 mA of line current, can operate with battery supply voltages down to -21 V to reduce line card power dissipation.

The SLIC incorporates loop current, ground key and ring trip detection functions.

Two-to four-wire and four- to two-wire voice frequency (vf) signal conversion is accomplished by the SLIC in conjunction with either a conventional CODEC/filter or with a programmable CODEC/filter (e.g. SLAC, SiCoFi, Combo II). The programmable line terminating impedance could be complex or real to fit every market.

The PBL 387 10/1 package is 28-pin PLCC.

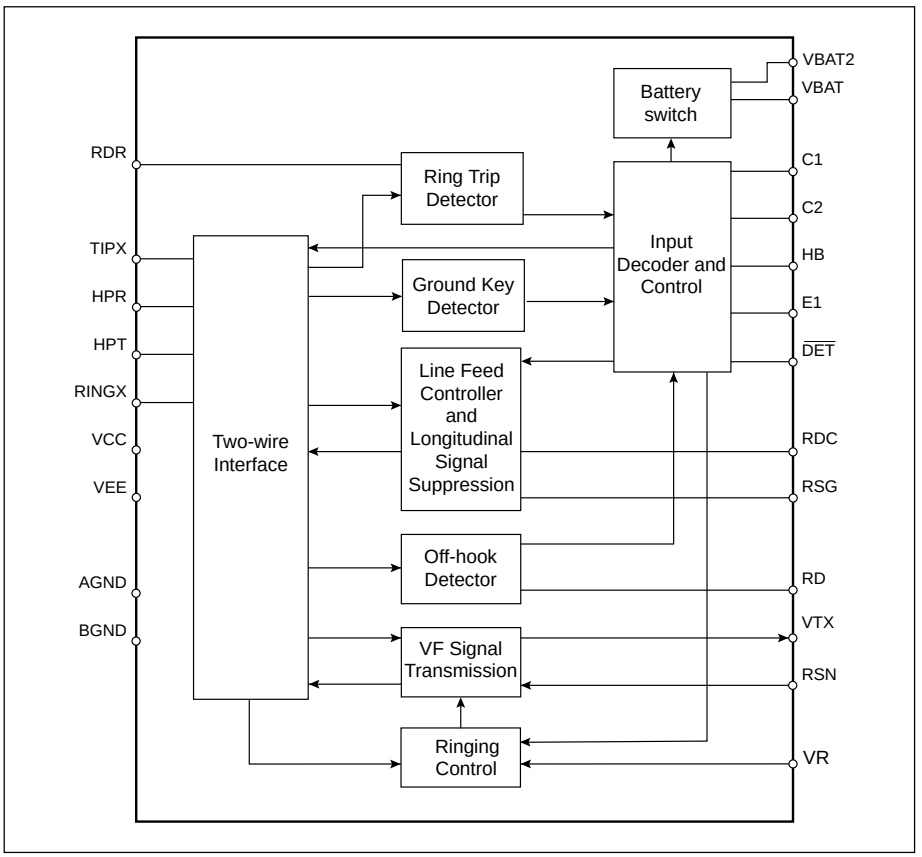
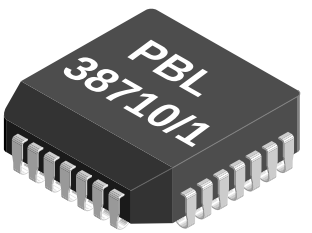


Figure 1. Block diagram.

Key Features

- Ring SLIC eliminates ring relay and conventional ring-generator
- Supports sine wave and trapezoidal ringing
- -85 V battery feed for high voltage ring signal
- On chip automatic battery switch
- Programmable battery feed characteristics
- Battery supply voltage as low as -21 V for power efficient line card designs
- Low on-hook power dissipation, 50 mW @-24 V battery
- Loop current, ring trip and ground key detection functions
- Programmable loop current detector threshold
- Programmable ring trip detector threshold
- Hybrid function with all types of CODEC/filter devices
- Programmable line terminating impedance, complex or real
- On-hook transmission
- Tip-ring open circuit state for subscriber loop power denial



28-pin PLCC

Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature, Humidity				
Storage temperature range	T_{Stg}	-55	+150	°C
Operating junction temperature range	T_J	-40	+140	°C
Power supply, -40°C ≤ T_{Amb} ≤ 85°C				
V_{CC} with respect to AGND	V_{CC}	-0.5	6.5	V
V_{EE} with respect to AGND	V_{EE}	-6.5	0.5	V
V_{Bat} with respect to BGND	V_{Bat}	-85	V_{EE} + 0.5	V
V_{Bat2} with respect to BGND	V_{Bat2}	V_{Bat}	V_{EE} + 0.5	V
Power dissipation				
Continuous power dissipation at T_{Amb} ≤ 85 °CP	$_D$		1.5	W
Peak power dissipation at T_{Amb} = 85 °C, t < 100 ms, t_{Rep} > 1 sec.	P_{DP}		4W	
Ground				
Voltage between AGND and BGND	V_G	-0.3	0.3	V
Digital inputs, outputs (C1, C2, E1, HB, $\overline{DET}$)				
Input voltage	V_{ID}	0V	$_{CC}$	V
Output voltage ($\overline{DET}$ disabled)	V_{OD}	0V	$_{CC}$	V
Output current ($\overline{DET}$ enabled)	I_{OD}		5m	A
Ring voltage, input (VR)				
Input voltage	V_{VR}	V_{EE}	V_{CC}	V
TIPX and RINGX terminals, -40°C ≤ T_{Amb} ≤ 85°C, V_{Bat} = -80V, Active, Disconnect and Stand by states				
TIPX or RINGX voltage, continuous (referenced to AGND), Note 1	V_{TA}, V_{RA}	V_{Bat}	2V	
TIPX or RINGX, pulse < 10 ms, t_{Rep} > 10 s, Note 1	V_{TA}, V_{RA}	V_{Bat} - 5	5	V
TIPX or RINGX, pulse < 1 µs, t_{Rep} > 10 s, Note 1	V_{TA}, V_{RA}	V_{Bat} - 25	10	V
TIP or RING, pulse < 250 ns, t_{Rep} > 10 s, Note 1	V_{TA}, V_{RA}	V_{Bat} - 35	15	V
TIPX or RINGX maximum current supplied			110	mA

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Ambient temperature	T_{amb}	-40	+85	°C
V_{CC} with respect to AGND	V_{CC}	4.75	5.25	V
V_{EE} with respect to AGND	V_{EE}	-5.25	-4.75	V
V_{Bat2} with respect to BGND, Note 2	V_{Bat2}	-58	-24	V
V_{Bat} with respect to BGND	V_{Bat}	-80	V_{Bat2}	V

Notes

1. Whith diodes in series with the V_{Bat} and V_{Bat2} , see figure 12.
2. -24V <V_{Bat2} < -21V may be used in applications requiring maximum vf signal amplitudes less than $3V_{pk}$ (8.75 dBm, 600 Ω).

Electrical Characteristics

-40 °C ≤ T_{Amb} ≤ 85 °C, V_{CC} = +5V ±5 %, V_{EE} = -5V ±5%, V_{Bat} = -80V, V_{Bat2} = -48V, AGND = BGND, R_{DC1}=R_{DC2} =41.7kΩ,R_{SG} = 0Ω, R_D = 33kΩ, R_{DR} = 5.8 kΩ, C_{HP}=10nF, C_{DC} = 1.5 µF, Z_L =600 Ω, state input control pin HB = 0, unless otherwise specified.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Two-wire port						
Overload level, V_{TRO}	2Z	$_L$ = 600 Ω, 1% THD Note 1	3.1			V_{Peak}
Input impedance, Z_{TR}		Note 2				
Longitudinal impedance, Z_{LoT}, Z_{LoR}		0 < f < 100 Hz		12	35	Ω/wire
Longitudinal current limit, I_{LoT}, I_{LoR}		active state	10			mA_{rms}/wire
		stand-by state	8.5			mA_{rms}/wire
Longitudinal to metallic balance, B_{LM}		IEEE standard 455-1985				
		0.2 kHz ≤ f ≤ 1.0 kHz	46	63		dB
		1.0 kHz ≤ f ≤ 3.4 kHz	46	58		dB
Longitudinal to metallic balance, B_{LME}	3	0.2 kHz ≤ f ≤ 1.0 kHz	46	63		dB
		1.0 kHz ≤ f ≤ 3.4 kHz	46	58		dB
		$B_{LME} = 20 \cdot \text{Log} \left\lvert \frac{E_{Lo}}{V_{TR}} \right\rvert$				
Longitudinal to metallic balance, B_{LFE}	3	0.2 kHz ≤ f ≤ 1.0 kHz	46	63		dB
		1.0 kHz ≤ f ≤ 3.4 kHz	46	58		dB
		$B_{LFE} = 20 \cdot \text{Log} \left\lvert \frac{E_{Lo}}{V_{TX}} \right\rvert$				
Metallic to longitudinal balance, B_{MLE}	4	0.2 kHz < f < 3.4 kHz	40			dB
		$B_{MLE} = 20 \cdot \text{Log} \left\lvert \frac{V_{TR}}{V_{Lo}} \right\rvert$, E_{RX} = 0				

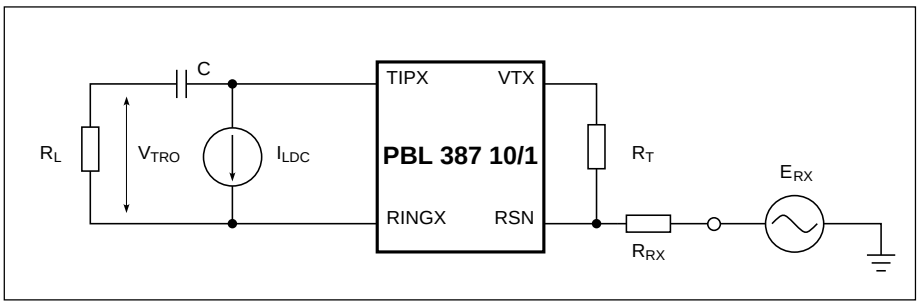


Figure 2. Overload level, V_{TRO}, two-wire port

$\frac{1}{\omega C} << R_L$, R_L= 600 Ω

R_T = 600 kΩ, R_{RX} = 300 kΩ

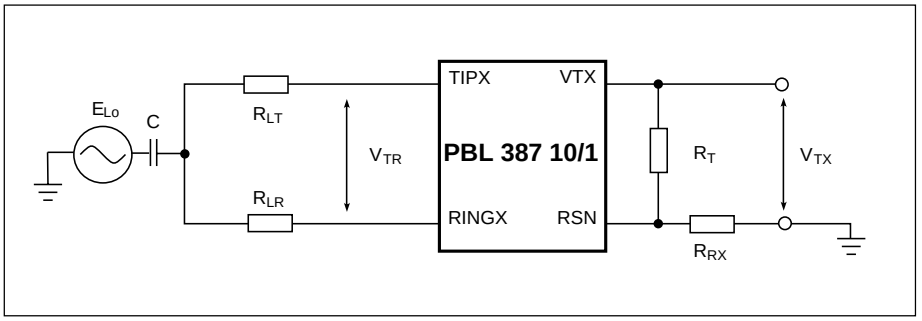


Figure 3. Longitudinal to metallic (B_{LME}) and Longitudinal to four-wire (B_{LFE}) balance

$\frac{1}{\omega C} << 150\ \Omega$, $R_{LT} = R_{LR} = 300\ \Omega$

R_T = 600 kΩ, R_{RX} = 300 kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire to longitudinal balance, B_{FLE}	4	0.2 kHz < f < 3.4 kHz $B_{FLE} = 20 \cdot \text{Log} \left\lvert \frac{E_{RX}}{V_{Lo}} \right\rvert$	40			dB
Two-wire return loss, r		$r = 20 \cdot \text{Log} \frac{\lvert Z_{TR} + Z_L \rvert}{\lvert Z_{TR} - Z_L \rvert}$ $Z_{TR} \approx Z_L$ = nom. 600 Ω				
		0.2 kHz ≤ f ≤ 0.5 kHz	25			dB
		0.5 kHz ≤ f ≤1.0 kHz	27			dB
		1.0 kHz ≤ f ≤ 3.4 kHz, Note 9	23			dB
TIPX idle voltage, V_{Ti}		active, $I_L = 0$		-1.5		V
		stand-by, $I_L = 0$		0.6		V
RINGX idle voltage, V_{Ri}		active, $I_L = 0$		-46.5		V
		stand-by, $I_L = 0$		-47		V
TIPX-RINGX open loop metallic voltage, V_{TR}		$I_L = 0$, $R_{SG} = 0\Omega$, V_{Bat2} = -52V	43.0	45.0	47.0	V
Four-wire transmit port (VTX)						
Overload level, V_{TXO}	5	Load impedance > 20 kΩ, 1% THD, Note 3	3.1			V_{Peak}
Output offset voltage, ΔV_{TX}			-60		60	mV
Output impedance, z_{TX}		0.2 kHz ≤ f ≤ 3.4 kHz		<5	20	Ω
Four-wire receive port (RSN)						
Receive summing node (RSN) dc voltage		I_{RSN} = 0 mA		0		V
Receive summing node (RSN) impedance		0.2 kHz ≤ f ≤ 3.4 kHz		<10	20	Ω
Receive summing node (RSN) current (I_{RSN}) to metallic loop current (I_L) gain, α_{RSN}		0.3 KHz ≤ f ≤ 3.4 kHz		1000		ratio

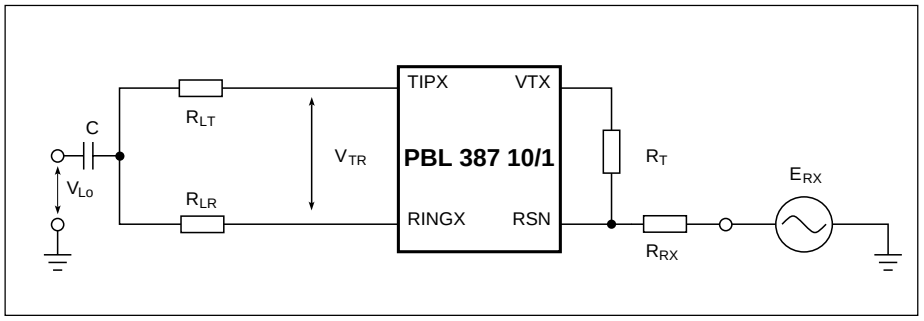


Figure 4. Metallic to longitudinal and four-wire to longitudinal balance

$\frac{1}{\omega C} << 150\ \Omega$, $R_{LT} = R_{LR} = 300\ \Omega$

R_T = 600 kΩ, R_{RX} = 300 kΩ

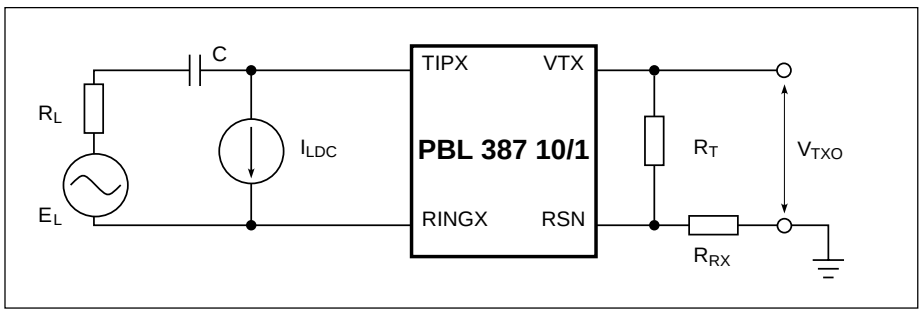


Figure 5. Overload level, V_{TXO}, four-wire transmit port

$\frac{1}{\omega C} << R_L$, R_L= 600 Ω

R_T = 600 kΩ, R_{RX} = 300 kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Frequency response						
Two-wire to four-wire, g_{2-4}	6	0.3 kHz < f < 3.4 kHz relative to 0 dBm, 1.0 kHz. E_{RX} = 0 V	-0.2		0.2	dB
Four-wire to two-wire, g_{4-2}	6	0.3 kHz < f < 3.4 kHz relative to 0 dBm, 1.0 kHz. E_L = 0 V	-0.2		0.2	dB
Four-wire to four-wire, g_{4-4}	6	0.3 kHz < f < 3.4 kHz relative to 0 dBm, 1.0 kHz. E_L = 0 V	-0.2		0.2	dB
Insertion loss						
Two-wire to four-wire, G_{2-4}	6	0 dBm, 1.0 kHz, Note 4 $G_{2-4} = 20 \cdot \text{Log} \left\lvert \frac{V_{TX}}{V_{TR}} \right\rvert$, $E_{RX} = 0$	-0.2		0.2	dB
Four-wire to two-wire, G_{4-2}	6	0 dBm, 1.0 kHz, Notes 4, 5 $G_{4-2} = 20 \cdot \text{Log} \left\lvert \frac{V_{TR}}{E_{RX}} \right\rvert$, $E_L = 0$	-0.2		0.2	dB
Gain tracking						
Two-wire to four-wire	6	Ref. -10 dBm, 1.0 kHz, Note 7				
		-40 dBm to +3 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Four-wire to two-wire	6	Ref. -10 dBm, 1.0 kHz, Note 8				
		-40 dBm to +3 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Noise						
Idle channel noise at two-wire		C-message weighting		10	12	dBrnC
(TIPX-RINGX) or four-wire (VTX) output		Psophometrical weighting Note 6		-80	-78	dBmp
Harmonic distortion						
Two-wire to four-wire		0 dBm, 1.0 kHz test signal		-60		dB
Four-wire to two-wire		0.3 kHz < f < 3.4 kHz		-60		dB

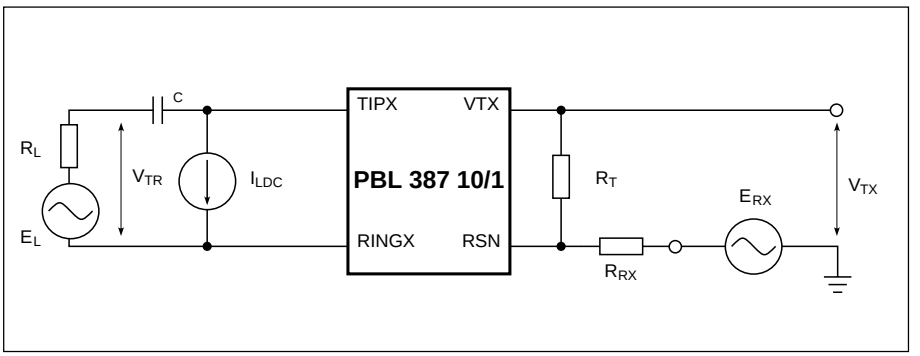


Figure 6. Frequency response, insertion loss, gain tracking.

$\frac{1}{\omega C} << R_L$, $R_L = 600\ \Omega$

$R_T = 600\ k\Omega$, $R_{RX} = 300\ k\Omega$

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Battery feed characteristics						
Constant loop current, I_{LProg}		$I_{LProg} = \frac{2500}{R_{DC1} + R_{DC2}}$, R_{DC1}, R_{DC2} in kΩ	0.88 I_{LProg}	I_{LProg}	1.12 I_{LProg}	mA
Stand-by state loop current, I_L		$I_L = \frac{\lvert V_{Bat} \rvert - 2}{R_L + 2000}$: T_A = 25°C	0.8 I_L	I_L	1.2 I_L	mA
Ring state loop current limit, I_{LLim}		$V_{TIP-RING}$ > 0 V, -40 - 0 °C	70	95		mA
		$V_{TIP-RING}$ < 0 V, -40 - 0 °C	47	70		mA
Ring state loop current limit, I_{LLim}		$V_{TIP-RING}$ > 0 V, 0 - 85 °C	73	95		mA
		$V_{TIP-RING}$ < 0 V, 0 - 85 °C	50	70		mA
Ring injection						
Input impedance, Z_{VR}				10.5		kΩ
		R_L = 7 kΩ, 1.1 V ≤ VR ≤ 1.9 V				
Ring node (VR) voltage to tip-ring voltage (V_{TR}) gain		20 Hz, DC	36.6	38.6	40.6	ratio
Ring signal distortion		20 Hz, Sine		0.5	2.5	%
Loop current detector						
Loop current detector threshold		I_{LTh} = 360 / R_D , R_D = 33 kΩ	0.85 I_{LTh}	I_{LTh}	1.15 I_{LTh}	mA
Ground key detector						
I_{LTIPX} and I_{RINGX} current difference, ΔI_{LOn}, to trigger the ground key detector			5.5	10.5	15.5	mA
Ring trip detector						
Ring trip detector threshold		I_{RTh} = 360 / R_{DR} , R_{DR} = 5.8 kΩ	0.85 I_{RTh}	I_{RTh}	1.15 I_{RTh}	mA
Digital inputs (C1, C2, HB, E1)						
Input low voltage, V_{IL}			0		0.8	V
Input high voltage, V_{IH}			2.0		V_{CC}	V
Input low current, I_{IL}		V_{IL} = 0.4 V				
C1, C2, HB			-700			µA
E1			-100			µA
Input high current, I_{IH}		V_{IH} = 2.4 V			200	µA
Detector output ($\overline{DET}$)						
Output low voltage, V_{OL}		I_{OL} = 2 mA			0.45	V
Output high voltage,V_{OH}		I_{OH} = 100 µA	2.7			V
Internal pull-up resistor			7.0	15.6	27.0	kΩ
Power dissipation (V_{Bat2} = -48V)						
P_1		Open circuit state, C1, C2 = 0, 0		35	60	mW
P_2		Stand-by state, HB =0 C1, C2 = 1, 1; on-hook		60	100	mW
		Active state, C1, C2 = 0, 1				
P_3		On-hook, R_L = ∞ Ω @V_{Bat2} = -24V		130		mW
P_4		Off-hook, R_L = 300 Ω @V_{Bat2} = -24V		610		mW

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Power supply currents						
V_{CC} current, I_{CC}		Open circuit state		2.0		mA
V_{EE} current, I_{EE}		C1, C2 = 0, 0		1.2		mA
V_{Bat} current, I_{Bat}		On-hook		0.2		mA
V_{Bat2} current, I_{Bat2}				0.1		mA
V_{CC} current, I_{CC}		Stand-by state		2.4		mA
V_{EE} current, I_{EE}		C1, C2 = 1, 1		1.1		mA
V_{Bat} current, I_{Bat}		On-hook		0.4		mA
V_{Bat2} current, I_{Bat2}				0.3		mA
V_{CC} current, I_{CC}		Active state		5.9		mA
V_{EE} current, I_{EE}		C1, C2 = 0.1		2.3		mA
V_{Bat} current, I_{Bat}		On-hook		0.2		mA
V_{Bat2} current, I_{Bat2}		V_{Bat} = -80V, V_{Bat2} = -24V		3.1		mA
Power supply rejection ratios						
V_{CC} to 2- or 4-wire port		Active State		45		dB
V_{EE} to 2- or 4-wire port		C1, C2 = 0.1		45		dB
V_{Bat} to 2- or 4-wire port		50Hz < f< 3400Hz, V_n = 100mV_{RMS}		32		dB
V_{Bat2} to 2- or 4-wire port				45		dB
Temperature guard						
Junction threshold temperature, T_{JG}				160		°C
Thermal resistance						
28-pin PLCC, $\theta_{RJP28plcc}$		Junction to terminals 3, 10, 17, 24 connected together		20		°C/W

Notes

1. The overload level is specified at the two-wire port with the signal source at the four-wire receive port.
2. The two-wire impedance is programmable by selection of external component values according to:
   $Z_{TRX} = Z_T/|G_{2-4} \cdot \alpha_{RSN}|$ where:
   Z_{TRX} = impedance between the TIPX and RINGX terminals
   Z_T = programming network between the VTX and RSN terminals
   G_{2-4} = transmit gain, nominally = 1
   α_{RSN} = receive current gain, nominally = -1000 (current defined as positive when flowing into the receive summing node (RSN), and when flowing from Tip to Ring).
3. The overload level is specified at the four-wire transmit port, VTX, with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is G_{2-4} = 1.
4. Fuse resistors R_F impact the insertion loss as explained in the text, section Transmission. The specified insertion loss is for R_F = 0.
5. The specified insertion loss tolerance does not include errors caused by external components.
6. The two-wire idle noise is specified with the port terminated in 600 Ω (R_L) and with the four-wire receive port grounded (E_{RX} = 0).
   The four-wire idle noise at VTX is specified with the two-wire port terminated in 600 Ω (R_L). The noise specification is with respect to a 600 Ω programmed two wire impedance level at VTX. The four-wire receive port is grounded (E_{RX} = 0).
7. The level is specified at the two-wire port.
8. The level is specified at the four-wire receive port and referenced to a 600 Ω programmed two wire impedance level.
9. Higher return loss values can be achieved by adding a reactive component to R_T, the two-wire terminating impedance programming resistance, e.g., by dividing R_T into two equal halves and connecting a capacitor from the common point to ground. For R_T = 600 kΩ this capacitor would be approximately 30 pF. Increasing C_{HP} to 0.033 µF improves low-frequency return loss.

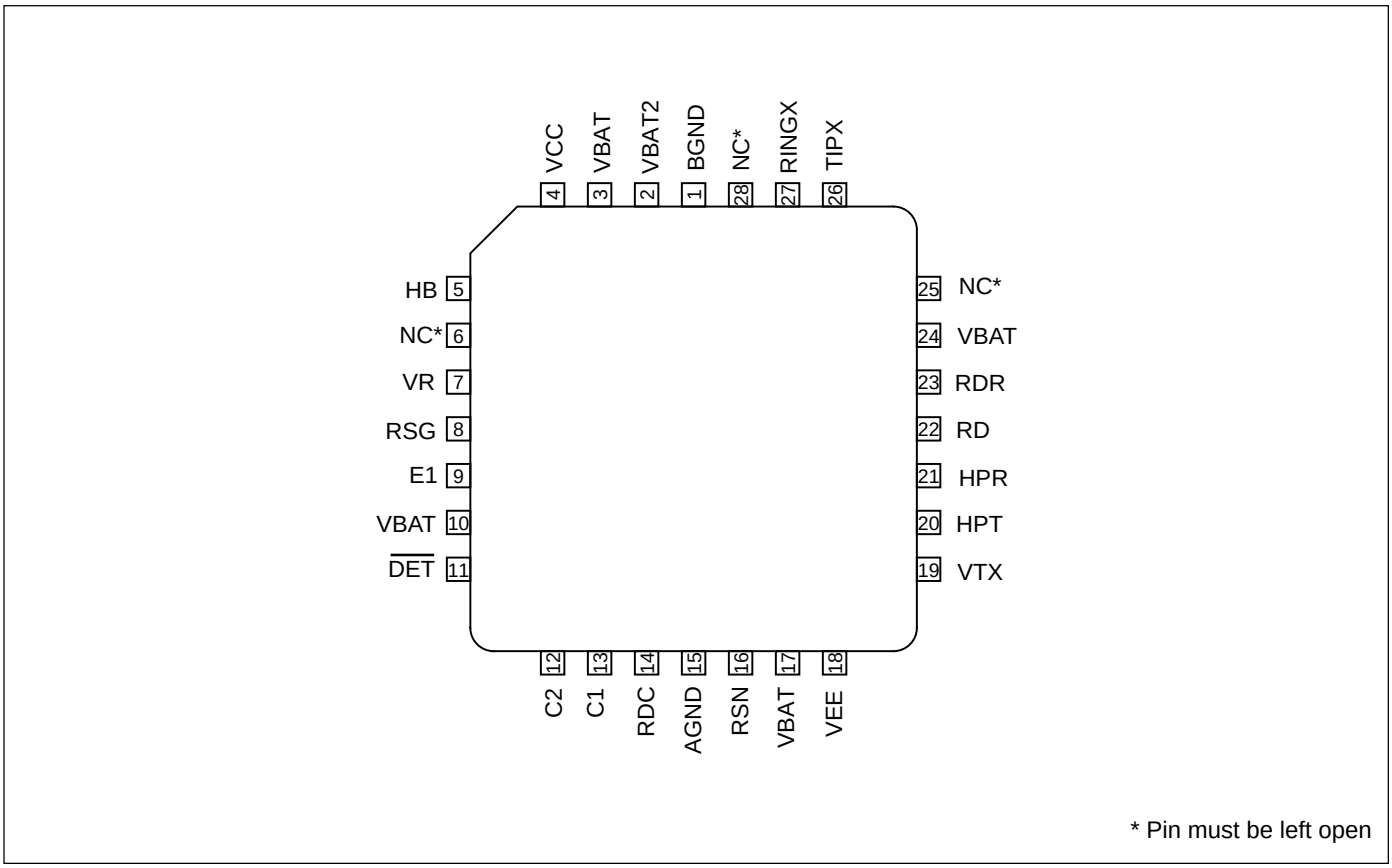


Figure 8. Pin configuration 28-pin PLCC, top view.

Pin Description

Refer to figure 8.

PLCC	Symbol	Description
1	BGND	**G**rou**nd**. Should be tied together with AGND.
2	VBAT2	Low **bat**tery supply voltage.
3	VBAT	High **bat**tery supply voltage.
4	VCC	+5V power supply
5	HB	Enables the **H**igh **B**attery to be present in the stand-by state. The purpose is to be able to offer a high open-loop voltage (battery switch between ring and active state is controlled from the control pins).
6	NC	**N**o internal **C**onnection. Note 1.
7	VR	**V**oltage **R**ing. Low voltage (2Vpk) ringsignal (any waveform) is injected here.
8	RSG	The internal **S**aturation **G**uard programming **R**esistor, R_{SG}, connects from this terminal to VEE . Refer to section "Battery feed" for detailed information.
9	E1	TTL compatible Enable input. Enables desired detector to be gated to the $\overline{\text{DET}}$ output. Refer to section "Control inputs" for detailed information.
10	VBAT	This pin is used for heat sinking and is internally connected to VBAT.
11	$\overline{\text{DET}}$	Detector output. Inputs C1 and C2 together with enable input E1 select one of the three detectors to be connected to the $\overline{\text{DET}}$ output. A logic low at the enabled $\overline{\text{DET}}$ output indicates a triggered detector condition. The $\overline{\text{DET}}$ output is open collector with internal pull-up resistor (approximately 15 kΩ to V_{CC}).
12	C2	C1 and C2 are TTL compatible inputs controlling the SLIC operating states.
13	C1	Refer to section "Control inputs" for details.
14	RDC	Constant current feed is programmed by two resistors connected in series from this pin to the receive summing node (RSN). The resistor junction point is decoupled to GND to isolate the ac signal components.
15	AGND	Ground. Should be tied together with BGND.
16	RSN	Receive summing node. 1000 times the current (dc and ac) flowing into this pin equals the metallic (transversal) current flowing from RINGX to TIPX. Programming networks for constant current feed, two-wire impedance and receive gain connect to the receive summing node.
17	VBAT	This pin is used for heat sinking and is internally connected to pin 3.
18	VEE	-5V power supply.
19	VTX	Transmit vf output. The ac voltage difference between TIPX and RINGX, the ac metallic voltage, is reproduced as an unbalanced GND referenced signal at VTX with a gain of one. The two-wire impedance programming network connects between VTX and RSN.
20	HPT	Tip side of ac/dc separation capacitor C_{HP}. Other end of C_{HP} capacitor connects to pin HPR.
21	HPR	Ring side of ac/dc separation capacitor C_{HP}. Other end of C_{HP} connects to pin HPT.
22	RD	Off-hook detector **P**rogramming **R**esistor R_D in parallel with filter capacitor C_D connect from RD to VEE.
23	RDR	Connect to the "**r**ing trip **d**etector" **r**esistor.
24	VBAT	This pin is used for heat sinking and is internally connected to pin 3.
25	NC	**N**o internal **C**onnection. Note 1.
26	TIPX	The TIPX and RINGX pins connect to the tip and ring leads of the two-wire interface via overvoltage protection components.
27	RINGX	
28	NC	**N**o internal **C**onnection. Note 1.

Note:

1. Terminals marked NC are not internally connected to the chip but may be used for future functions. Do leave open.

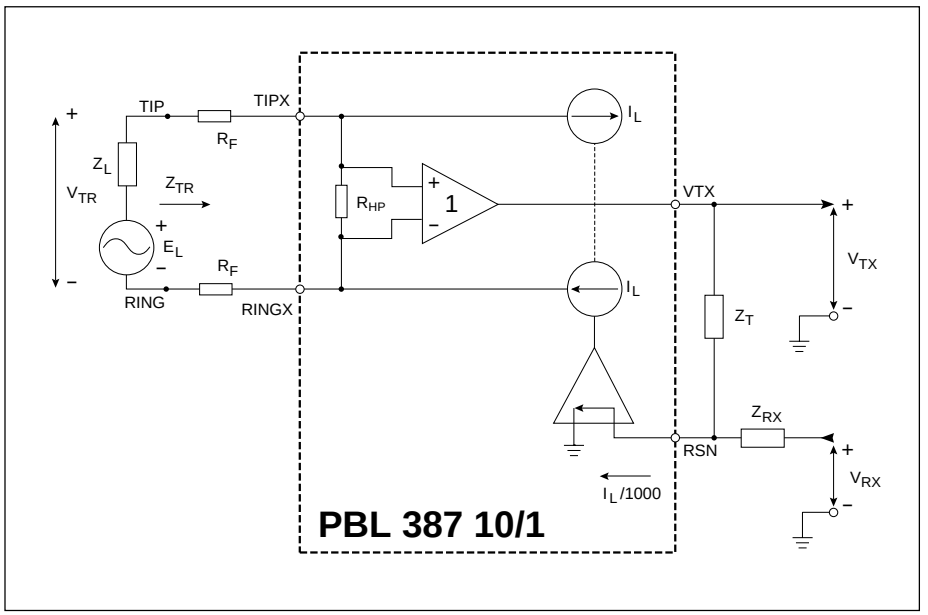


Figure 9. Simplified ac transmission circuit.

Functional Description and Applications Information

Transmission

General

A simplified ac model of the transmission circuits is shown in figure 9. Circuit analysis yields:

$$V_{TR} = V_{TX} + I_L \cdot 2R_F \quad (1)$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_L}{1000} \quad (2)$$

$$V_{TR} = E_L - I_L \cdot Z_L \quad (3)$$

where:

- V_{TX} is a ground referenced version of the ac metallic voltage between the TIPX and RINGX terminals.
- V_{TR} is the ac metallic voltage between tip and ring.
- E_L is the line open circuit ac metallic voltage.
- I_L is the ac metallic current.
- R_F is a fuse resistor.
- Z_L is the line impedance.
- Z_T determines the SLIC TIPX to RINGX impedance at voice frequencies.
- Z_{RX} controls four- to two-wire gain.
- V_{RX} is the analog ground referenced receive signal.

Two-Wire Impedance

To calculate Z_{TR}, the impedance presented to the two-wire line by the SLIC, in active state, including the fuse resistor R_F , let $V_{RX} = 0$.

From (1) and (2):

$$Z_{TR} = \frac{Z_T}{1000} + 2R_F$$

Thus with Z_{TR} and R_F known:

$$Z_T = 1000 \cdot (Z_{TR} - 2R_F)$$

The SLICs two-wire output impedance in ringing state is typically 2· 40 Ω for a 15 -100 Hz ring-signal.

Two-Wire to Four-Wire Gain

From (1) and (2) with $V_{RX} = 0$:

$$G_{2\text{-}4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/1000}{\frac{Z_T}{1000} + 2R_F}$$

Four-Wire to Two-Wire Gain

From (1), (2) and (3) with $E_L = 0$:

$$G_{4\text{-}2} = \frac{V_{TR}}{V_{RX}} = \frac{Z_T}{Z_{RX}} \cdot \frac{Z_L}{\frac{Z_T}{1000} + Z_L + 2R_F}$$

For applications where $Z_T/1000 + 2R_F$ is chosen to be equal to Z_L the expression for $G_{4\text{-}2}$ simplifies to:

$$G_{4\text{-}2} = - \frac{Z_T}{Z_{RX}} \cdot \frac{1}{2}$$

Four-Wire to Four-Wire Gain

From (1), (2) and (3) with $E_L = 0$:

$$G_{4\text{-}4} = \frac{V_{TX}}{V_{RX}} = - \frac{Z_T}{Z_{RX}} \cdot \frac{Z_L + 2R_F}{\frac{Z_T}{1000} + Z_L + 2R_F}$$

Hybrid Function

The hybrid function can easily be implemented utilizing the uncommitted amplifier in conventional CODEC/filter combinations. Please, refer to figure 10. Via impedance Z_B a current proportional to V_{RX} is injected into the summing node of the combination CODEC/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain a voltage proportional to V_{RX} is returned to V_{TX}. This voltage is converted by R_{TX} to a current flowing into the same summing node. These currents can be made to cancel by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \ (E_L = 0)$$

The four-wire to four-wire gain, $G_{4\text{-}4}$, includes the required phase shift and thus the balance network Z_B can be calculated from:

$$Z_B = - R_{TX} \cdot \frac{V_{RX}}{V_{TX}} =$$

$$R_{TX} \cdot \frac{Z_{RX}}{Z_T} \cdot \frac{\frac{Z_T}{1000} + Z_L + 2R_F}{Z_L + 2R_F}$$

If calculation of the Z_B formula above yields a balance network containing an inductor, an alternate method is recommended. Contact Ericsson Microelectronics for assistance.

The PBL 38710/1 SLICs may also be used together with programmable CODEC/filters. The programmable CODEC/filter allows for system controller adjustment of hybrid balance to accommodate different line impedances without change of hardware. In addition, the transmit and receive gain may be adjusted. Please, refer to the programmable CODEC/filter data sheets for design information.

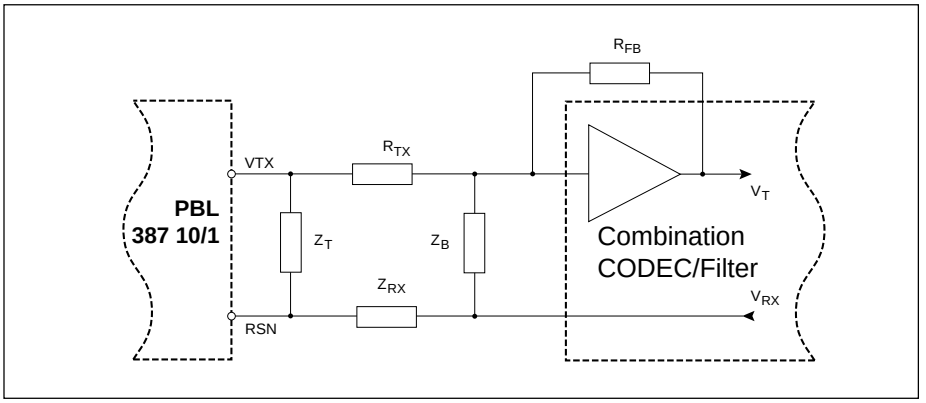


Figure 10. Hybrid funktion.

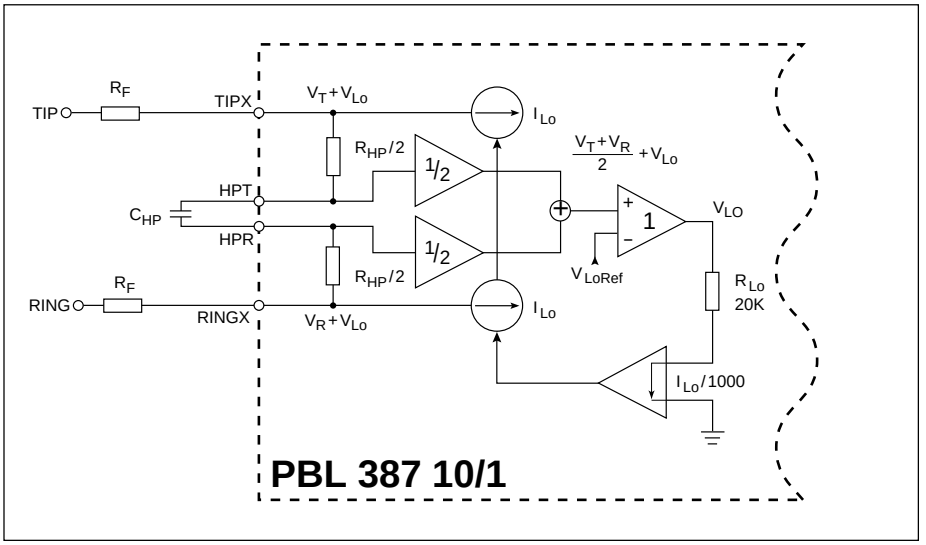


Figure 11. Longitudinal impedance.

Longitudinal Impedance

A feed back loop counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase.

Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions, leaving metallic voltages well within the SLIC common mode range.This is accomplished by comparing the instantaneous two-wire longitudinal voltage to an internal longitudinal reference voltage, V_{LoRef}.

$$V_{LoRef} = \frac{V_{Bat2}}{2} = \frac{V_T + V_R}{2}$$

where V_T and V_R are tip and ring ground referenced voltages without any longitudinal component. As shown below the SLIC appears as 20 Ω per wire to longitudinal disturbances. It should be noted that longitudinal currents may exceed the dc loop current without disturbing the vf transmission. Refer to figure 11.

Circuit analysis yields:

$$\frac{V_{Lo}}{R_{Lo}} = \frac{I_{Lo}}{1000}$$

which reduces to

$R_{LoT} = R_{LoR} = V_{Lo} / I_{Lo} = 20k\Omega/1000 = 20\Omega$

where:

R_{Lo} = 20 kΩ

R_{LoT} = R_{LoR} = longitudinal resistance/wire

V_{Lo} = longitudinal voltage at TIPX,RINGX

I_{Lo} = longitudinal current

Capacitors C_{TC} and C_{RC}

The capacitors designated C_{TC} and C_{RC} in figure 12, connected between TIPX and ground as well as between RINGX and ground, are recommended as an addition to the overvoltage protection network. Very fast transients, appearing on tip and ring, may pass by the active components in the overvoltage protection network before they have had time to activate and could damage the SLIC. C_{TC} and C_{RC} short such very fast transients to ground. C_{TC} and C_{RC} also work as RFI-filters in conjunction with suitable series impedances (i.e. resistances, inductances). Resistors R_{F1} and R_{F2} may be sufficient, but series inductances can be added to form a second order filter. The recommended value for C_{TC} and C_{RC} is 2200 pF. Higher capacitance values may be used, but care must be taken to prevent degradation of either longitudinal balance or return loss. C_{TC} and C_{RC} contribute to a metallic impedance of $1/(\pi \cdot f \cdot C_{TC}) = 1/(\pi \cdot f \cdot C_{RC})$, a TIPX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{TC})$ and a RINGX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{RC})$.

AC - DC Separation Capacitor, C_{HP}

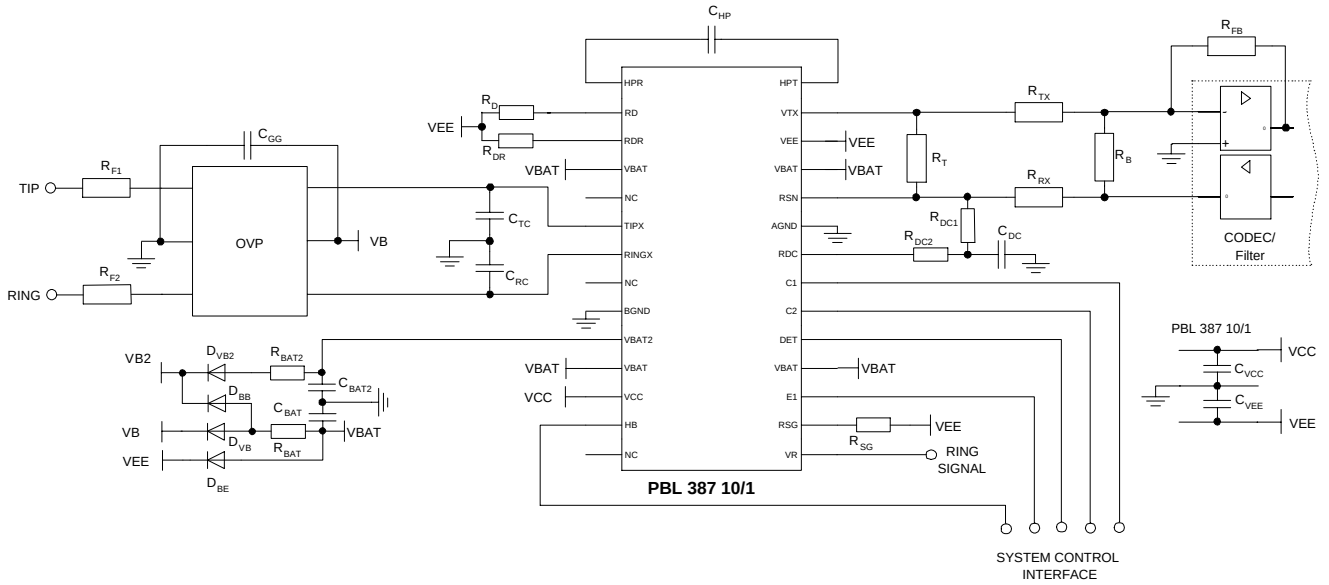
The high pass filter capacitor connected between terminals HPT and HPR provides the separation between circuits sensing tip-ring dc conditions and circuits processing ac signals. A C_{HP} value of 10 nF will position the low end frequency response 3dB break point at 48 Hz (f_{3dB}) according to $f_{3dB} = 1/(2 \cdot \pi \cdot R_{HP} \cdot C_{HP})$ where $R_{HP} \approx 330$ kΩ.

Battery Feed

The block diagram in figure 13 shows the PBL 38710/1 battery feed system and figure 14 illustrates the battery feed characteristics in the active state.

For a tip to ring dc voltage V_{TR} less than the saturation guard reference voltage ,V_{SGRef}, the SLIC emulates a constant current feed characteristic in the active state. The constant current is independent of the actual battery voltage, V_{Bat2}, connected to the SLIC.

With the tip to ring DC voltage V_{TR} exceeding V_{SGRef}, the feed characteristic changes to a nearly-constant voltage feed. This is to prevent the tip and ring drive amplifiers from distorting the AC signal as might have otherwise occurred due to insufficent voltage margin between V_{TR} and V_{Bat2}. Thus the SLIC



RESISTORS:

R_T	442	kΩ	1%	1/10 W
R_{RX}	221	kΩ	1%	1/10 W
R_{TX}	20	kΩ	1%	1/10 W
R_B	15.8	kΩ	1%	1/10 W
R_{DC1}	61.9	kΩ	5%	1/10 W
R_{DC2}	61.9	kΩ	5%	1/10 W
R_{SG}	0	Ω	5%	1/10 W
R_D	39	kΩ	5%	1/10 W
R_{DR}	7	kΩ	5%	1/10 W
R_{F1}, R_{F2}	40	Ω	1%	
R_{BAT}, R_{BAT2}	5.1	Ω	5%	1/10 W
R_{FB}	Depending on Codec/filter			

CAPACITORS:

C_{TC}	2.2	nF	20%	100V
C_{RC}	2.2	nF	20%	100V
C_{HP}	0.01	µF	20%	100V
C_{GG}	220	nF	20%	100V
C_{BAT}	470	nF	20%	100V
C_{BAT2}	470	nF	20%	100V
C_{VEE}	100	nF	20%	10V
C_{DC}	1.5	µF	20%	10V
C_{VCC}	100	nF	20%	10V

DIODES:

D_{BE}	1N4448
D_{BB}	1N4448
D_{VB}	1N4448
D_{VB2}	1N4448

OVP:

TISP PBL2 (Power Innovations)

Design spec.

Z_{TR}	600	Ω
I_L	20	mA
G_{4-2}	1	
G_{2-4}	0.73	
V_{TRO}	3.1	V

Figure 12. Single-channel subscriber line interface with PBL 378 10/1 and combination CODEC/filter.

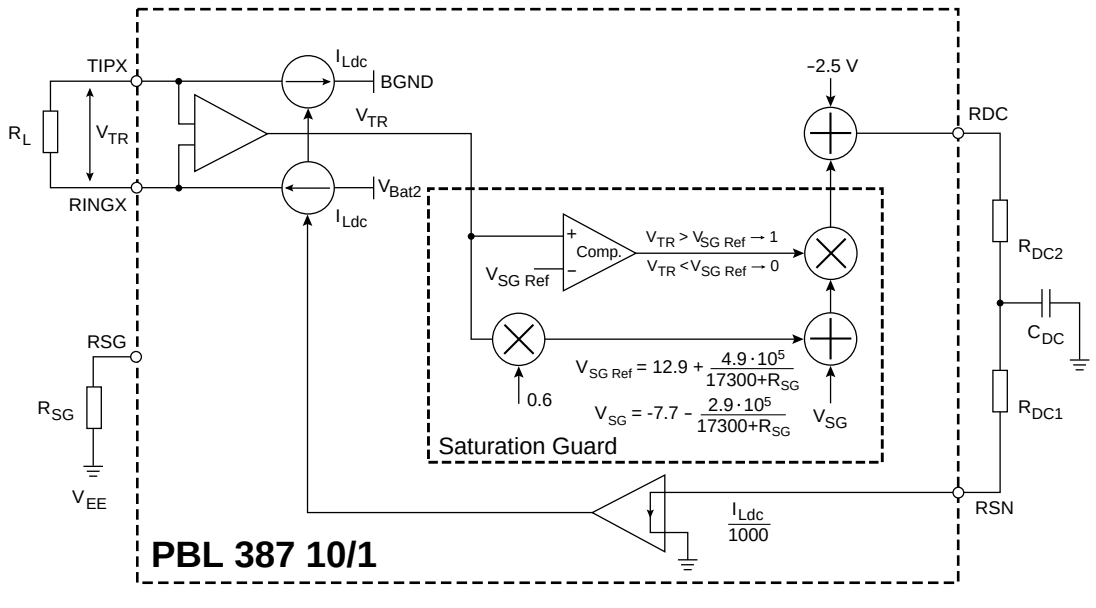
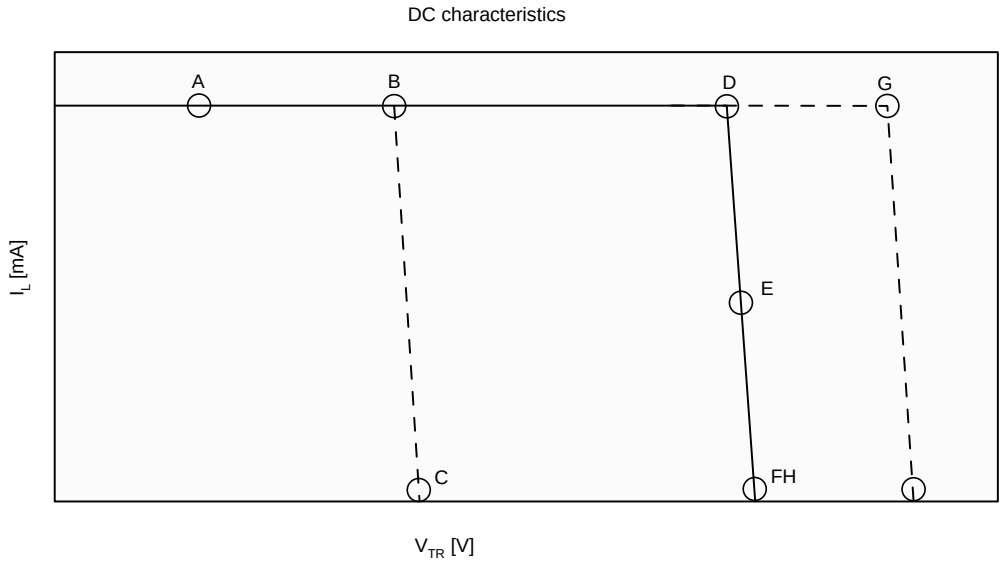


Figure 13. Battery feed (C2, C1 = 1, 0 active state).



A: $I_L = I_{LProg} = \frac{2.5}{R_{DC1} + R_{DC2}} \cdot 1000$

B: V_{SGRef} when R_{SG} -> ∞

C: V_{TR} when R_{SG} -> ∞ and R_L -> ∞

D: $V_{SGRef} = 12.9 + \frac{4.9 \cdot 10^5}{R_{SG} + 17300}$

E:
$$\begin{cases} V_{TR} = R_L \cdot \frac{16.7 + 4.9 \cdot 10^5 / (R_{SG} + 17300)}{R_L + (R_{DC1} + R_{DC2}) / 653} \\ I_L = \frac{1}{3.8} \cdot \frac{2.5}{R_{DC1} + R_{DC2}} \cdot 1000 \cdot (16.7 + \frac{4.9 \cdot 10^5}{R_{SG} + 17300} - V_{TR}) \end{cases}$$

F: $V_{TR} = 16.7 + \frac{4.9 \cdot 10^5}{R_{SG} + 17300}$ when RL —> ∞

G: V_{SGRef} when R_{SG} —> 0

H: V_{TR} when R_{SG} —> 0 and R_L —> ∞

Figure 14. Battery feed characteristics (without protection resistors on the line, active state).

automatically adjusts the tip to ring dc voltage V_{TR} to the maximum safe value.

With the SLIC in the stand-by state (C2,C1=1.1) a resistiv feed characteristic is enabled. To achive a high open loop voltage it is possible to switch the battery feed from V_{Bat2} to V_{Bat}

When the SLIC is in the ringing state V_{Bat} is used in order to achive a ring voltage as high as possible.The battery feed programming is also disconnected.

The following text explains the four battery cases in more detail.

Case 1: SLIC in the active state

$V_{TR} < V_{SGRef}$

In the active state C2=1, C1=0 and V_{Bat2} is used for battery feed. In this operating state tip to ring voltages V_{TR} less than V_{SGRef}, cause the block titled saturation guard (figure 13) to be disabled, i.e. its output is equal to zero.

For this case circuit analysis yields:

$$R_{DC1} + R_{DC2} = \frac{2.5}{I_{LProg}} \cdot 1000$$

where:

I_{LProg} = constant loop current (independent of the loop resistance R_L).

$R_{DC1} + R_{DC2}$ = the programming resistance which sets the constant loop current.

For a tip to ring voltage V_{TR} less than V_{SGRef} the PBL 38710/1 thus emulate a constant current feed with the magnitude of the constant current set by resistors, R_{DC1}, and R_{DC2}.

Capacitor C_{DC} at the R_{DC1} - R_{DC2} common point removes vf signals from the battery feed control loop. C_{DC} is calculated according to:

$$C_{DC} = T \cdot \left(\frac{11}{R_{DC1,2}} + \frac{}{R_{DC}}\right)$$

where T=30 ms. Note that R_{DC1}=R_{DC2} yields minimum C_{DC} value.

Case 2: SLIC in the active State

$V_{TR} > V_{SGRef}$

In the active state C2=1, C1=0 and V_{Bat2} is used for battery feed. The saturation guard reference voltage is user programmable according to:

$$V_{SGRef} = 12,9 \frac{49 \cdot 10^5}{17300 + R_{SG}}$$

where:

R_{SG} = saturation guard reference programming resistor in Ω.

V_{SGRef} = saturation guard reference voltage in volts.

Once the dc metallic voltage, V_{TR}, exceeds the saturation guard reference voltage, V_{SGRef}, the saturation guard becomes active and the following expression describes the battery feed characteristic:

$$V_{TR} = R_L \cdot \frac{16.7 + 4.9 \cdot 10^5 / (R_{SG} + 17300)}{R_L + (R_{DC1} + R_{DC2}) / 653}$$

where R_{SG}, R_L and V_{TR} have the same meaning as described above.

At open loop, i.e. $R_L \rightarrow \infty$, the saturation guard limits the tip-ring voltage to:

$$V_{TR} = 16.7 + 4.9 \cdot 10^5 / (R_{SG} + 17300)$$

Figures 17 through 20 illustrate the PBL 38710/1 loop feed with V_{Bat2} =-48V and V_{Bat2} = -24V.

For applications where the tip-to-ring DC voltage, V_{TR}, approaches the V_{Bat2} value. R_{SG} should be adjusted as follows:

As a general guideline, adjust R_{SG} in the V_{TR} expression above to yield

$V_{TRMax} \leq |V_{Bat\,2}| - 8$ at maximum loop resistance. Maintaining V_{TR} below this limit ensures vf transmission through the SLIC without clipping.

R_{SG} can be calculated from:

$$R_{SG} = \frac{49 \cdot 10^5}{(|V_{Bat2}| - V_{Margin}\left[1 + \frac{(R_{DC12} + R_{DC})}{600 R_L}\right] - 16{,}7} - 17300$$

where:

V_{Margin} = 8V to allow a maximum overload level, V_{TRO}, of 3.1V.

If transmission is required at open loop, i.e. $R_L \rightarrow \infty$, the above expression simplifies to:

$$R_{SG} = \frac{49 \cdot 10^5}{|V_{Bat2}| - V_{Margin} - 16{,}7} - 17300$$

In applications where the longest possible two-wire loop length is important, it is possible to increase the maximum loop resistance at minimum allowable loop current by reducing the voltage margin

$V_{Margin} = |V_{Bat2}| - V_{TRMax}$

from the 8V suggested above. Doing so will, however, reduce the overload level from 3.1 V_{Peak} as shown in figure 21. Figure 22 shows the typical maximum loop resistance at 18 mA as a function of the voltage margin for several values of programmed constant-current feed and $V_{Bat\,2}$ = -48 V.

Case 3: SLIC in the Stand-by State

In the stand-by state C1=1, C2=1and input HB selects the battery to be used for battery feed. With the SLIC operating in the stand-by, power saving state, the tip and ring drive amplifiers are disconnected and a resistive battery feed is engaged. The loop current can be calculated from:

$$I_L \approx \frac{|VBat| - 2}{R_L + 2000}$$

where:

I_L = loop current (A).
R_L = loop resistance (Ω).
V_{Bat} = battery supply voltage (V_{Bat} or V_{Bat2} depends on input HB) (V).

The stand-by short circuit loop current (I_{LSh}) for V_{Bat2} = -28V (HB=0) is then limited to:
$I_{LSh} \approx$ 13.9 mA.

HB=1 enables V_{Bat} for use in applications that demand a high open loop voltage. Note that the equation above is also valid in the high battery state and that the SLIC will not change to active state by itself when the loop current detector goes low. Switching between stand-by and active state is controlled via inputs C1 and C2.

Case 4: SLIC in the Ringing State

In the ringing state C2=0, C1=1 and V_{Bat} is used for battery feed. To calculate loop current during ringing, see the " PBL 38710/1 Power Dissipation " section.

PBL 38710/1 Power Dissipation

Two cases: active (V_{Bat2} is used for battery feed) and ringing (V_{Bat} is used for battery feed). $|V_{Bat}| > |V_{Bat2}|$

The short circuit SLIC power dissipation is (in active state):

$$P_{ShTot} = I_{LSh} \cdot (|V_{Bat2}| - I_{LSh} \cdot 2R_F) + P_3$$

where V_{Bat2} is the battery voltage connected to the SLIC at pin VBAT2.

$$I_{LSh} = \frac{2{,}5 \cdot 1000}{R_{DC12} + R_{DC}}$$

is the constant loop current. P_3 is on hook active state power dissipation (typ 130mW; V_{Bat2} = -24V). Note that a short circuited loop is not a normal operational condition. The terminal equipment will add some dc resistance (typically 150 to 300 Ω) even if the wire resistance is close to 0 Ω. Figure 23 compares line feed power dissipation as a function of loop resistance for three cases: feed resistor dissipation for a conventional 2·400 Ω resistive feed, PBL 38710/1 with 30 mA constant current feed and V_{Bat2} = -48V and PBL 38710/1 with 30 mA constant current feed and V_{Bat2} =-28V. The diagram illustrates the significant PBL 38710/1 power-saving compared to the 2·400 Ω feed.

During ringing the highest power dissipation occurs when the line is 0 Ω and maximum number of bells are connected (5REN).For information about the REN specification see the "Ring Voltage" section.The line current is calculated as:

$$I_L = \frac{|V_{Bat}| - 3}{Z_{Bell} + Z_{Line} + 2R_F + Z_{TR}}$$

where:

Z_{Bell} = bell impedance.
Z_{Line} = line impedance.
R_F = fuse and protection resistors.
Z_{TR} = tip- ring impedance during ringing (typically 2·40 Ω).

The maximum SLIC power dissipation during ringing is calculated as:

$$P_{SLIC} = P_S - P_{Out}$$

where (for a sinusodial shaped ring-signal)

$$P_S = \frac{2 \cdot V_{Bat} \cdot I_{LMax}}{\pi} + P_{TROpen}$$

and

$$P_{Out} = I_{Lrms}^2 \cdot (Z_{Bell} + 2R_F)$$

Example: calculate the maximum slic power dissipation when V_{Bat} = -80V, Z_{Bell} =1.4 kΩ(5USREN), Z_{Line}= 0, R_F = 40 Ω and Z_{TR} = 2·40 Ω. For these component values I_{Lmax} = 47 mA, P_S = 2.8 W (P_{TROpen} =390 mW (typ) @ V_{Bat} = -80V in ringing state), $P_{out} \approx$ 1.7 W and P_{SLIC} = 1.1 W which is less than the maximum allowed power dissipation (P_D =1.5 W, see data sheet).

Temperature Guard

A ring to ground short circuit fault condition as well as other improper operating conditions may cause excessive SLIC power dissipation. If junction temperature increases beyond T_{JG} , the junction threshold temperature, the temperature guard will trigger, causing the SLIC to be set to a high-impedance state. In this high impedance state, power dissipation is reduced and

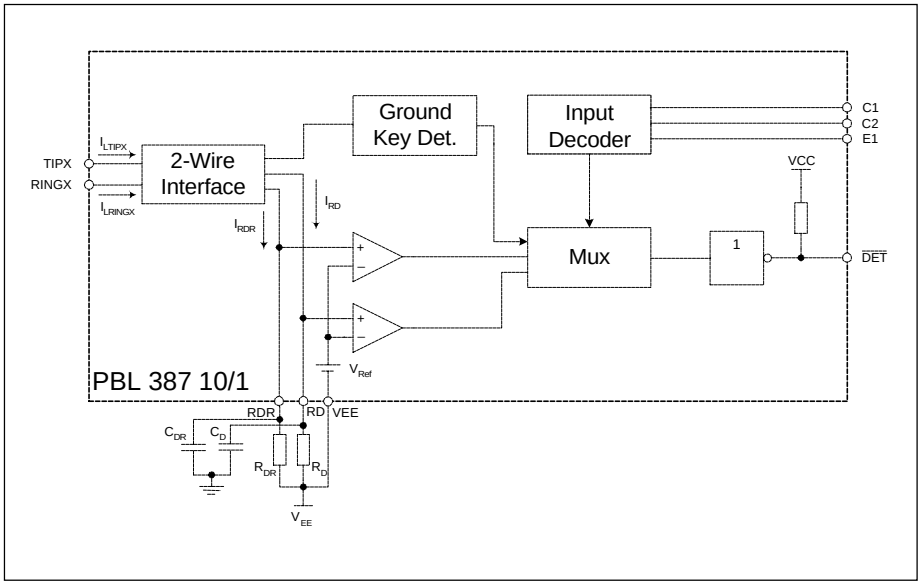


Figure 15. Loop current, ring -trip and ground key detectors.

the junction temperature will return to a safe value. Once below T_{JG}, the SLIC is returned back to its normal operating mode and will remain in that state, assuming the fault condition has been removed. As long as the temperature guard is triggered, the loop current detector will stay in active state.

PBL 38710/1 Long Loop vf Transmission

To ensure that the maximum vf signal intended to be received/transmitted by the SLIC will not experience limiting in the TIPX / RINGX drive amplifiers at long loops, the saturation guard must be correctly programmed. The section, ”Battery Feed, Case 2” describes how to calculate a value for the saturation guard programming resistor R_{SG}.

Loop Monitoring Functions

The loop current, ground key and ring trip detectors report their status through a common output, $\overline{DET}$. The detector to be connected to $\overline{DET}$ is selected via the control inputs. Please refer to section Control Inputs for a description of the control interface.

Loop Current Detector

The loop current detector is indicating that the telephone is off hook by putting the $\overline{DET}$ output to a logical low level when selected.The loop current threshold value, I_{LTh}, at which the loop current detector changes state is programmable by selecting the value of resistor R_D. R_D connects between pin RD and VEE.

Figure 15 shows a block diagram of the loop current detector. The two-wire interface produces a current flowing out of the pin RD:

$$I_{RD} = |I_{LTIPX} - IL_{RINGX}| / 600 = I_L / 300$$

where I_{LTIPX} and I_{LRINGX} are currents flowing into the TIPX and RINGX terminals and I_L is the loop current. The voltage generated by I_{RD} across the programming resistor R_D is compared to an internal reference by a comparator. A logic low results at the $\overline{DET}$ output when the loop current exceeds the on-hook to off-hook detect threshold, I_{LTh}.

The programming resistor, R_D , can be calculated for a desired I_{LTh} from:

$$R_D = 360 / I_{LTh}$$

R_D is in kΩ for I_{LTh} in mA. When the loop current is less than I_{LTh} the $\overline{DET}$ output is logic high . The C_D filter capacitor is calculated according to $C_D = T/R_D$ with time constant T=0.5 ms. Note that C_D may not be required if $\overline{DET}$ is software filtered.

Ground Key Detector

The ground key detector is indicating when the ground key is pressed (active) by putting the output pin $\overline{DET}$ to a logical low level when selected. The ground key detector circuit senses the difference in TIPX and RINGX currents.

Should the current difference exceed the threshold value, ΔI_{LOn} , the detector is triggered. As the current difference decreases the detector is reset at current threshold ΔI_{LOff} . $\Delta I_{LOn} > \Delta I_{LOff}$, i.e. the detector has hysteresis. The triggered detector results in a logic low at the $\overline{DET}$ output assuming the ground key detector has been selected via the control input. For ΔI_{LOn} and ΔI_{LOff} numerical values please refer to table ”Electrical characteristics”.

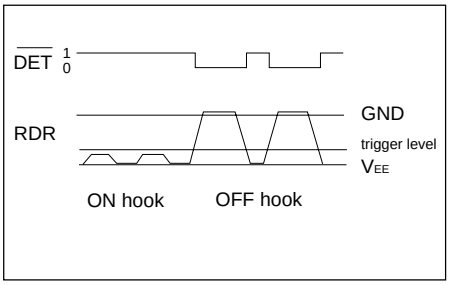


Figure 16. Ring-trip detector behavior.

Ring Trip Detector

The ring trip detector indicates if the line goes off hook while ringing by putting the $\overline{DET}$ output to a logical low level. The impedance changes when the telephone goes off hook and the detector detects the change in the line current. The loop current threshold value, I_{LTh}, at which the ring trip detector changes state is programmable by selecting the value of resistor $R_{DR.}$ R_{DR} connects between pin RDR and VEE.

Figure 15 shows a block diagram of the ring trip detector. The two-wire interface produces a current flowing out of the pin RDR

$$I_{RDR} = |I_{LTIPX} - I_{LRINGX}| / 600 = I_L / 300$$

where I_{LTIPX} and I_{LRINGX} are currents flowing into the TIPX and RINGX terminals and I_L is the loop current. The voltage generated by I_{RDR} across the programming resistor R_{DR} is compared to an internal reference by a comparator. When the loop current exceeds the detector threshold I_{LTh}, then the $\overline{DET}$

output is logic low. The programming resistor, R_{DR} , can be calculated for a desired $I_{LTh}$from:

$R_{DR} = 360 / I_{LTh}$

R_{DR} is in kΩ for I_{LTh} in mA. When the loop current is less than I_{LTh} then the $\overline{DET}$ output is logic high.

For calculation of the loop current during ringing see section " PBL38710/1 Power Dissipation ".

The C_{DR} filter capacitor is calculated according to $C_{DR} = T/R_{D\,R}$ with time constant T=0.5 ms. Note that C_{DR} may not be required if $\overline{DET}$ is software filtered. See figure 16 for the behavior of the states at the $\overline{DET}$ pin and voltage at the RDR pin.

Control Inputs

The PBL 38710/1 SLICs have four TTL compatible digital control inputs HB, E1, C2 and C1.

A decoder in the SLIC interprets the control input condition and sets up the commanded operating state.

Open Circuit State (C2,C1 = 0.0)

In the Open Circuit State the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum. No detectors are active.

Ringing State (C2,C1 = 0.1)

To accomplish a high voltage ring signal the battery feed uses the high voltage,V_{Bat} , when the ringing state is chosen. The SLIC will automatically (without any influence of input HB) switch to the high voltage. A low voltage ring signal at pin VR will be amplified and is transferred to the subscriber as a *balanced* ring signal.For additional information about the ring signal; see the Ring Voltage section.The ring trip detector is indicating off hook with a logic low level at the detector output.

Active State (C2,C1 = 1.0)

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. Vf signal transmission is normal.Both the loop current and the ground key detectors are activated. Input E1 control the selection of one of these detectors to be gated to the $\overline{DET}$ output.

Stand-by State (C2,C1 = 1.1)

Signal transmission is inhibited. In the Stand-by State the line drive amplifiers are disconnected. The loop feed is converted to resistive form.

The battery switch input signal HB controls which battery that is being used for battery feed.

Both the loop and ground key detectors are activated in this operating state. Input E1 control the selection of one of these detectors to be gated to the $\overline{DET}$ output. Table 1 summarizes the above description of the control inputs.

Enable Input (E1)

The TTL compatible input E1 controls the function of the $\overline{DET}$ output in the *active* and *stand-by* states. In open circuit and ringing state the detector to be gated to the $\overline{DET}$ is automatically chosen by the SLIC when one of these states is selected by input signals C1 and C2.

When set to logic level low, in the active or the stand-by state, E1 gates the ground key detector to the $\overline{DET}$ output. And when E1 is set to logic lewel high the loop current detector is gated to the $\overline{DET}$ output.

Table 1 summarizes the description of the E1 input.

Battery Switch (HB)

The TTL compatible input HB controls the switching, in the *stand-by* state, between V_{Bat} at pin VBAT and V_{Bat2} at pin VBAT2. $|V_{Bat}| > |V_{Bat2}|$.(Note that when ringing state is selected by inputs C1 and C2 the SLIC automatically changes to V_{Bat})

When HB is set to logic level low in the stand-by state, the SLIC will use V_{Bat2} for battery feed and if HB is set to logic level high , the SLIC will use the V_{Bat} for battery feed . Table 1 summarizes the description of the HB input.

Note 1					**SLIC operating**		
State	**HB**	**E1**	**C2**	**C1**	**state**	$\overline{DET}$ **output**	**Battery Feed**
1	X	X	0	0	Open circuit	Logic level high	Note 2
2	X	X	0	1	Ringing	Ring trip status	V_{Bat}
3	X	0	1	0	Active	Ground key status	V_{Bat2}
4	X	1	1	0	Active	Loop current status	V_{Bat2}
5	0	0	1	1	Stand-by	Ground key status	V_{Bat2} Note 3
6	0	1	1	1	Stand-by	Loop current status	V_{Bat2} Note 3
7	1	0	1	1	Stand-by	Ground key status	V_{Bat} Note 3
8	1	1	1	1	Stand-by	Loop current status	V_{Bat} Note 3

Table 1. Slic operating states

Notes

1. Input C1 and C2 selects SLIC operating state, input E1 selects detector (except in open circuit- and ringing state) and input HB selects the battery to be used for battery feed in stand-by state. X symbolises "don´t care".
2. In the open circuit state the SLIC present a high impedance to the line and no battery is used for battery feed.
3. In stand-by state input HB must be set to select between V_{Bat2} and V_{Bat} . In the other states the SLIC automatically selects the appropriate battery. $|V_{Bat}| > |V_{Bat2}|$

Ring Voltage

First we define: Crest factor = $\frac{\hat{V}}{V_{rms}}$

Table 2 and 3 define the voltage over the bell under different conditions.The bell is modelled according to the USREN (Ringing Equivalence Number) standard. 1 USREN=6930Ω +8µF @ 20 Hz, so one bell has the impedance 7 kΩ at 20 Hz. 5REN is equal to five 1REN loads in parallel, 1386 Ω+40µF is approx. 1.4 kΩ at 20 Hz.

Load # REN	R_{Line}	Crest factor	Load voltage
1	0	1.41;sin	52.2
3	100	1.41;sin	47.2
5	100	1.41;sin	43.5
1	0	1.20	62.9
3	100	1.20	57.0
5	100	1.20	52.6
1	0	1.05	72.0
3	100	1.05	65.2
5	100	1.05	60.2

Table 2. The load voltage over the bell as a function of the number of bells, line length and ringsignal shape

Table 2 shows the load voltage as a function of line length, number of bells and shape of the ring signal when V_{Bat} = -80V and ringsignal=1.4V_{rms}. Crestfactor 1.41 corresponds to a sinusodial shape of the ringsignal, 1.20 is trapezoid and 1.05 is squarewave. The squarewaves crestfactor is not exactly one because some telephone equipment are not able to detect the steep flanks in a ”perfect” squarewave.

Load voltage	Crest factor	V_{Bat} [V] 3REN	5REN
40	1.41;sin	67.2	73.0
40	1.20	56.4	61.2
50	1.20	70.5	76.1
40	1.05	49.4	53.2
50	1.05	61.3	66.8

Table 3. The required battery voltage to achive a specific voltage over the bell.

In Table 3 the required V_{Bat} to achive a specific voltage over the bell (40 or 50 V) is presented, the load is fixed at 3 or 5REN with 100 Ω wire resistance. The high voltage ring signal from the SLIC will be balanced about V_{Bat}/2.

Overvoltage Protection

The PBL 387 10/1 SLIC must be protected against overvoltages on the telephone line caused by lightning, ac power contact and induction. Refer to Maximum Ratings, TIPX and RINGX terminals, for maximum allowable continuous and transient voltages that may be applied to the SLIC.

Secondary Protection

The circuit shown in figure 12 utilizes series resistors together with a programmable overvoltage protector (e. g. PowerInnovations TISP PBL2), serving as a secondary protection.

The TISP PBL2 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to negative supply voltage (i.e. the battery voltage,V_B). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clamped to ground by a diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage and the protector will crowbar into a low voltage on-state condition, by firing an internal thyristor.

A gate decoupling capacitor, C_{GG}, is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. C_{GG} shall be placed close to the overvoltage protection device. Without the capacitor even the low inductance in the track to the V_{Bat} supply will limit the current and delay the activation of the thyristor clamp.

The fuse resistors R_F serve the dual purposes of being non- destructive energy dissipators, when transients are clamped and of being fuses, when the line is exposed to a power cross.

Note that it is important to always use PTC´s in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore will not protect the SLIC.

Power-up Sequence

The voltage at pin VBAT sets the substrate voltage, which must at all times be kept more negative than the voltage at any other pin to prevent possible latch-up. The optimal power up sequence is ground, VBAT and then other supplies and signal leads.

However, V_{CC} may be connected before VBAT and if the VBAT supply voltage should be absent, a diod connected between V_{EE} and pin VBAT, see diod D_{BE} in figure 12, ensures the presence of the most negative supply voltage at the VBAT pin. The VBAT and VBAT2 pins should not be applied at a faster rate than corresponds to the time constant formed by 5,1 Ω resistors, R_{Bat} and R_{Bat2} in figure 12, in series with the VBAT and the VBAT2 pins and 0,47 mF capacitors, C_{Bat} and C_{Bat2} in figure 12, from the VBAT and VBAT2 pins to ground. These RC networks may be shared with several SLICs.

Printed Circuit Board Layout

Care in PCB layout is essential for proper function.The components connecting to the RSN input should be placed in close proximity to that pin, such that no interference is injected into the RSN pin. Ground plane surrounding the RSN pin is advisable.

Analog ground (AGND) should be connected to battery ground (BGND) on the PCB in one point.

V_{Bat2} = -48 V, R_{SG} = 4 kΩ
Curve A: $R_{DC1} + R_{DC2}$ = 71.4 kΩ
Curve B: $R_{DC1} + R_{DC2}$ = 83.3 kΩ
Curve C: $R_{DC1} + R_{DC2}$ = 100 kΩ
Curve D: $R_{DC1} + R_{DC2}$ = 125 kΩ

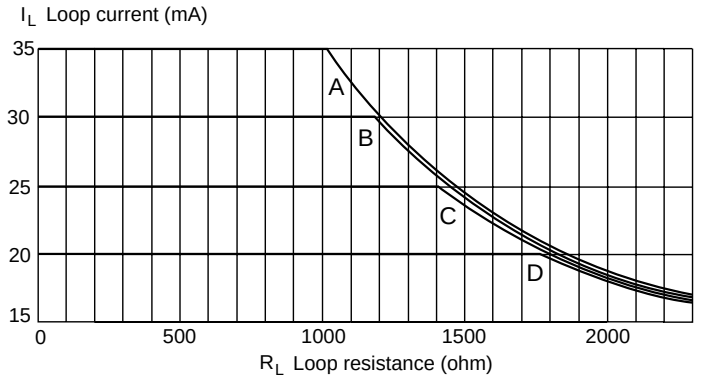


Figure 17. Loop current as a function of loop resistance.

V_{Bat2} = -48 V, R_{SG} = 4 kΩ
Curve A: I_{Const} = 35 mA
Curve B: I_{Const} = 30 mA
Curve C: I_{Const} = 25 mA
Curve D: I_{Const} = 20 mA

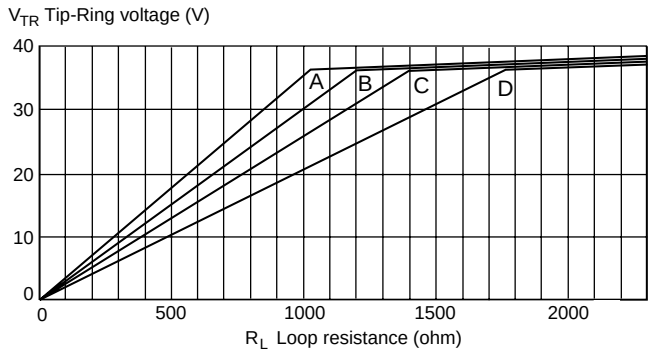


Figure 18. Tip-ring voltage as a function of loop resistance.

V_{Bat2} = -24 V, R_{SG} = ∞
Curve A: $R_{DC1} + R_{DC2}$ = 50.0 kΩ
Curve B: $R_{DC1} + R_{DC2}$ = 62.5 kΩ
Curve C: $R_{DC1} + R_{DC2}$ = 83.3 kΩ
Curve D: $R_{DC1} + R_{DC2}$ = 125 kΩ

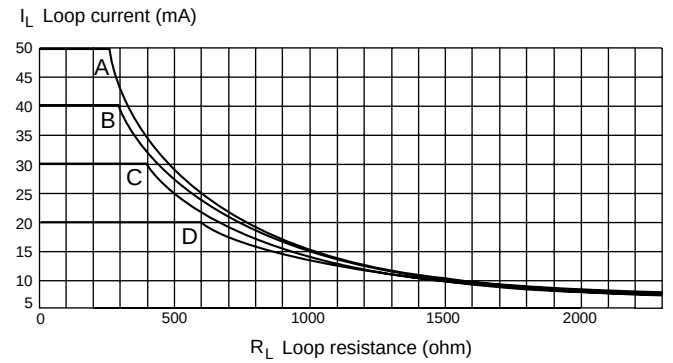


Figure 19. Loop current as a function of loop resistance.

V_{Bat2} = -24 V, R_{SG} = ∞
Curve A: I_{Const} = 50 mA
Curve B: I_{Const} = 40 mA
Curve C: I_{Const} = 30 mA
Curve D: I_{Const} = 20 mA

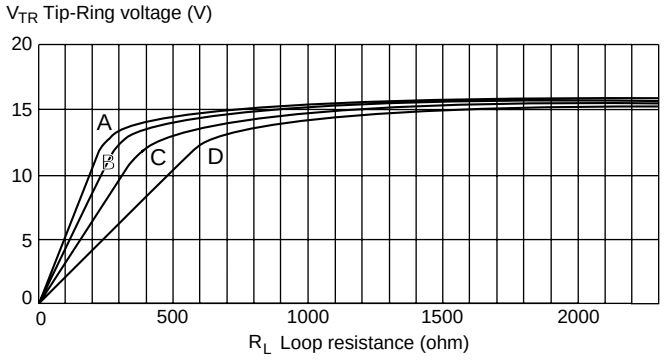
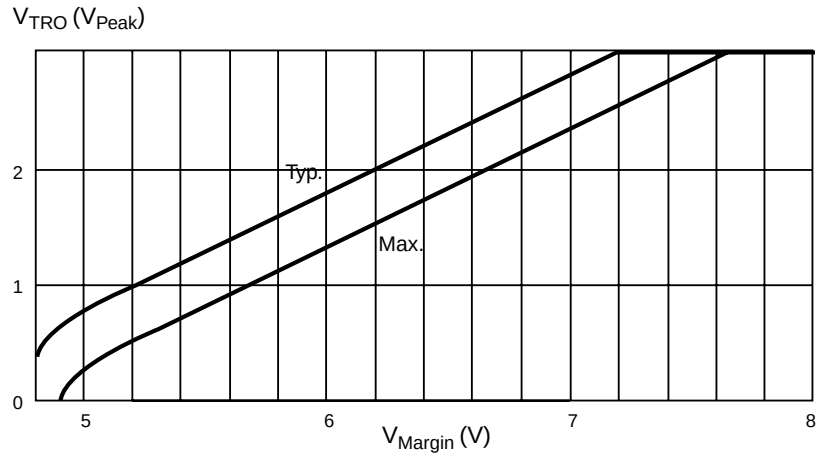
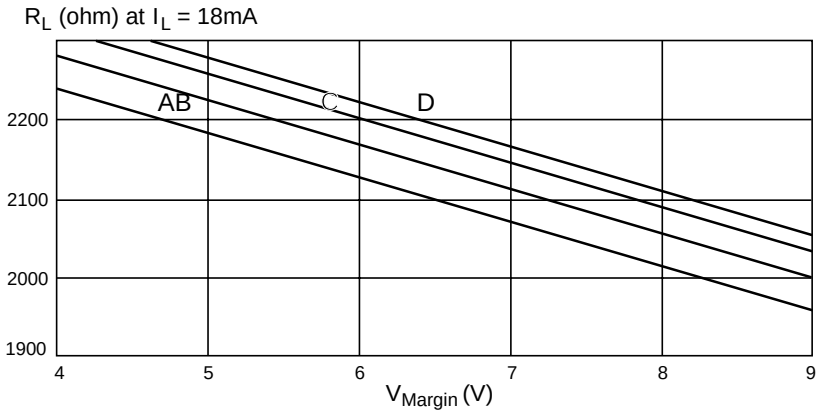


Figure 20. Tip-ring voltage as a function of loop resistance.



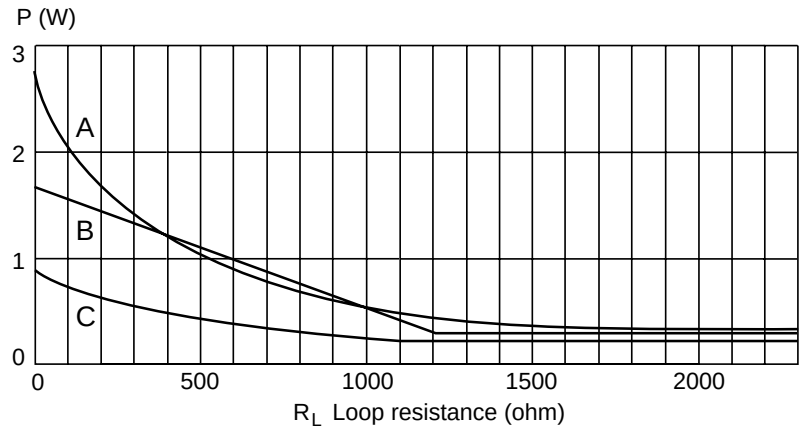
Max. V_{Margin} = *maximum* $|V_{Bat2}| - |V_{TRdc}|$ *required for distortion free transmission of a given* V_{TRO}.

Figure 21. Overload level, V_{TRO} *as a function of* V_{Margin}.



V_{Bat2} = -48 V
Curve A: I_{Const} = 20 mA
Curve B: I_{Const} = 25 mA
Curve C: I_{Const} = 30 mA
Curve D: I_{Const} = 35 mA

Figure 22. Loop resistance at I_L *= 18 mA as a function of* V_{Margin} *at open loop.*



Curve A: Conventional 2x400Ω resistive feed
Curve B: PBL 387 10/1, -48 V, 30 mA
Curve C: PBL 387 10/1, -28 V, 30 mA

Figure 23. Power dissipation.

Ordering Information

Package	Temp. Range	Part No.
28 pin PLCC Tube	-40- +85°C	PBL 387 10/1QNS
28 pin PLCC Tape & Reel	-40- +85°C	PBL 387 10/1QNT

Specifications subject to change without notice.
1522-PBL 387 10/1 Uen Rev. E

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