# XENSIV™ PAS CO2 12 V sensor based on photo acoustic spectroscopy principle


RoHS

Halogen-free

## Features

- **Operating range:** 0 ppm to 32000 ppm
- **Accuracy:** ±30 ppm ±3% of reading between 400 ppm and 5000 ppm
- **Lifetime:** 10 years for indoor mission profile
- **Interface:** $I^2C$, UART, and PWM
- **Package dimension:** 13.8 × 14 × 7.5 $mm^3$
- **Maintenance:** Maintenance-free when using ABOC feature (automatic baseline offset correction)

## Potential applications

High accuracy, compact size, and SMD capability make the XENSIV™ PAS CO2 sensor ideal for indoor air quality monitoring solutions in the market with numerous potential applications.

- HVAC (heating, ventilation, air conditioning)
- Home appliances
- Smart home IoT devices
- In-cabin air quality monitoring unit
- Agriculture/greenhouses

## Description

Infineon has leveraged its knowledge in sensors and MEMS technologies to develop a disruptive gas sensor for $CO_2$ sensing. The XENSIV™ PAS CO2 is a real $CO_2$ sensor combining NDIR technology with Infineon's high SNR MEMS microphones, allowing for state-of-the-art accuracy in an exceptionally small form factor.

The sensor is based on the photoacoustic spectroscopy (PAS) principle, where $CO_2$ molecules within the sensor cavity absorb infrared light, generating small pressure changes that are detected by an acoustic detector. $CO_2$ concentration is then delivered in the form of a direct ppm readout, thanks to the integrated microcontroller. Highly accurate $CO_2$ readings are guaranteed.

| OPN number | Package | SP number |
|---|---|---|
| PASCO2V01AUMA3 | LG-MLGA-14-1 | SP006037335 |

# Table of contents

# 1 Block diagram

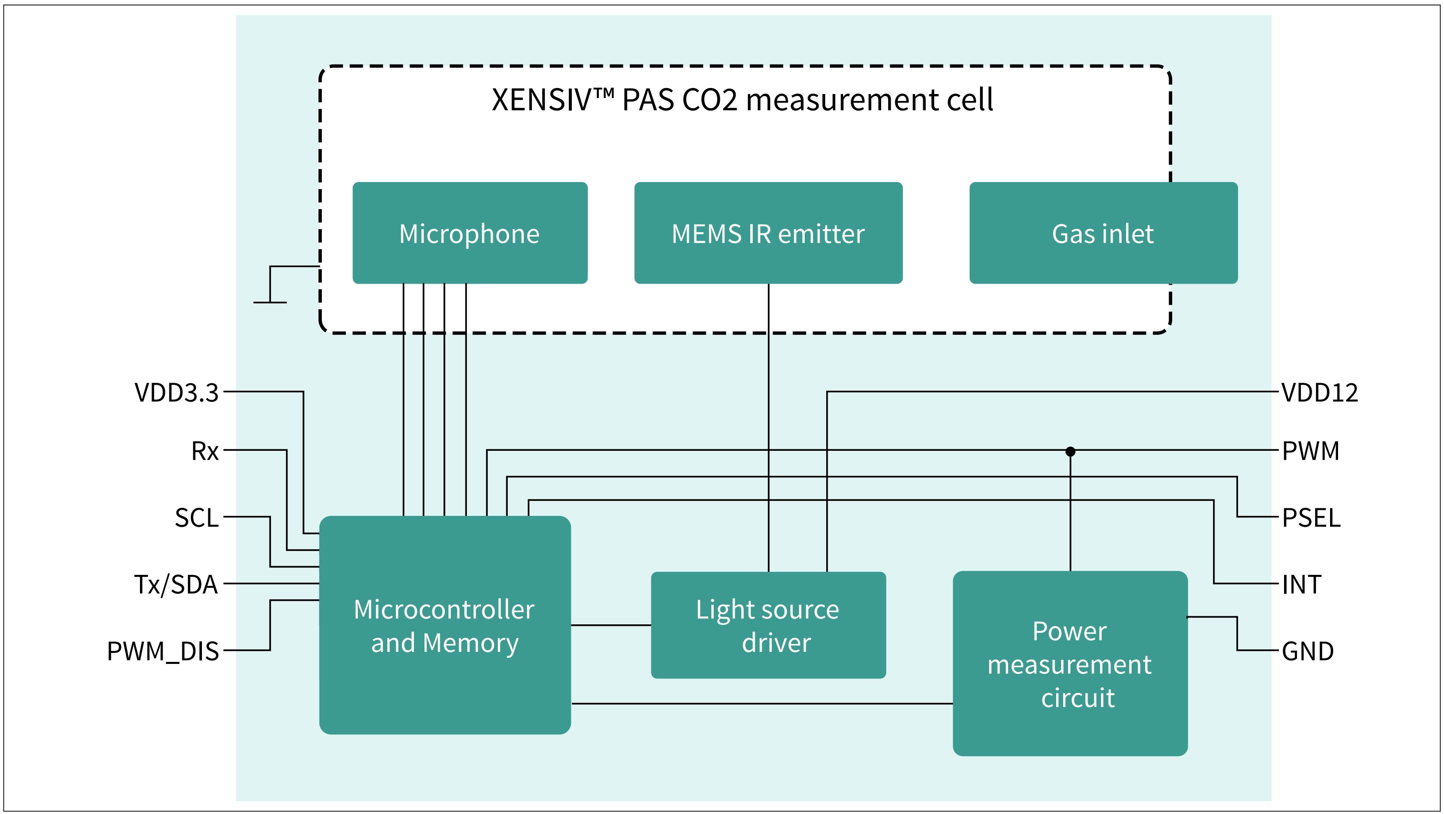


**Figure 1** **Block diagram of XENSIV™ PAS CO2**

# 2 Pin-out diagram

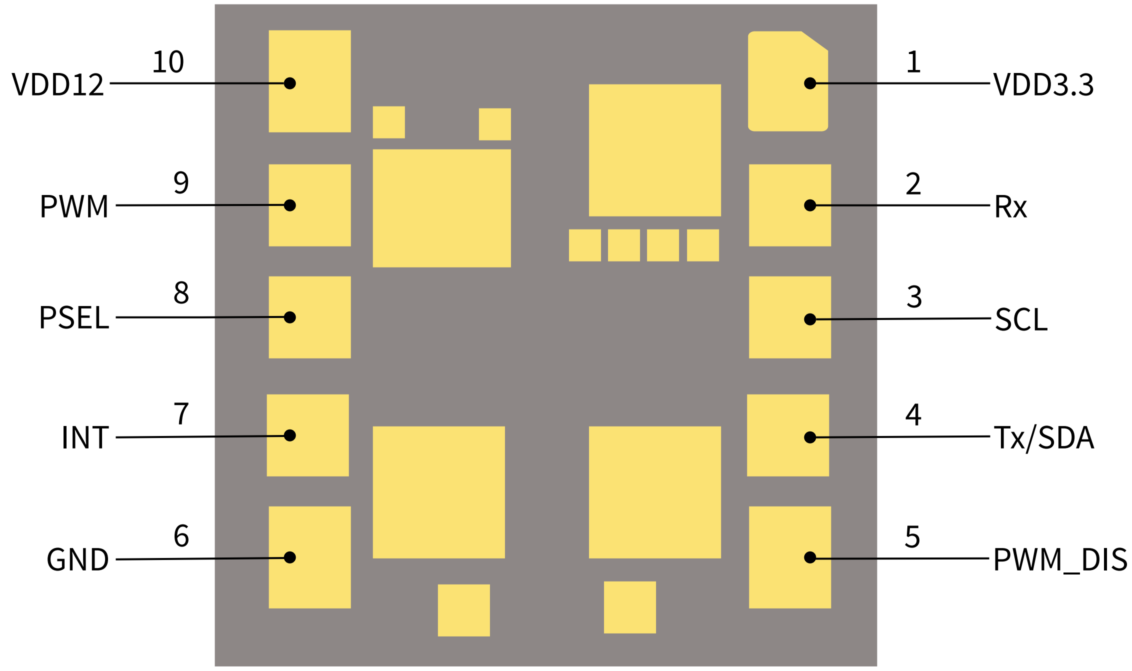


**Figure 2** Pin-out diagram (bottom view)

**Table 1** Pin description

| PIN | Symbol | Type | Description |
|---|---|---|---|
| 1 | VDD3.3 | Power supply (3.3 V) | 3.3 V digital power supply |
| 2 | Rx | Input/output | UART receiver pin (3.3 V domain) |
| 3 | SCL | Input/output | $I^2C$ clock pin (3.3 V domain) |
| 4 | Tx/SDA | Output | UART transmitter pin (3.3 V domain)/$I^2C$ data pin (3.3 V domain) |
| 5 | PWM_DIS | Input | PWM disable input pin (3.3 V domain) |
| 6 | GND | Ground | Ground |
| 7 | INT | Output | Interrupt output pin (3.3 V domain) |
| 8 | PSEL | Input | Communication interface select input pin (3.3 V domain) |
| 9 | PWM | Output | PWM output pin (3.3 V domain) |
| 10 | VDD12 | Power supply (12 V) | 12 V power supply for the IR emitter |

# 3 Typical sensor response to $CO_2$ concentration change

Measurement condition: VDD12 = 12.0 V, VDD3.3 = 3.3 V, $T_{amb}$ = 25°C, $p$ = 1013 hPa and % r.H. = 30%

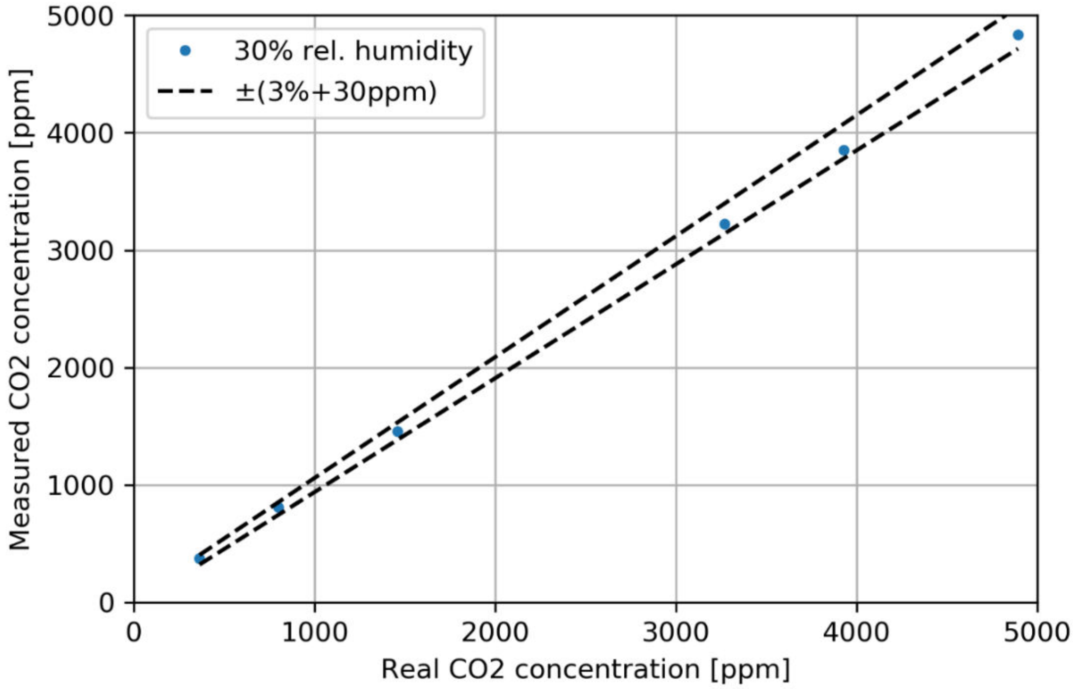


**Figure 3** **Typical sensor response to $CO_2$ concentration change**

# 4 Characteristics and parameters

## 4.1 Specification

### 4.1.1 Operating range

To ensure proper operation of the sensor, the following operating conditions must not be exceeded. All parameters specified in the subsequent sections refer to these operating conditions unless otherwise specified.

**Table 2 Operating range**

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $CO_2$ measurement range1) | $C_{CO2}$ | 0 | | 32000 | ppm | Functional measurement range |
| Ambient temperature1) | $T_{amb}$ | 0 | | 50 | °C | |
| Relative humidity1) | rH | 0 | | 85 | % | Non-condensing |
| Pressure1) | $p$ | 750 | 1013 | 1150 | hPa | |
| Supply voltage1) | VDD3.3 | 3 | 3.3 | 3.6 | V | |
| | VDD12 | 10.8 | 12 | 13.2 | V | |
| Lifetime1) | $t_{life}$ | | 10 | | Year | Depends on mission profile |

1) Not subject to production test. This parameter is verified by design/characterization.

### 4.1.2 Storage conditions

Storage condition refers to dry pack: packed, evacuated, desiccant[1], humidity indicator card (HIC) sealed moisture barrier bag.

**Table 3 Storage condition**

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Storage temperature1) | $T_{storage}$ | 5 | | 40 | °C | <90% r.H.2) |
| Storage time1) | $t_{storage}$ | | | 3 | Year | |
| Storage temperature during transport1) | $T_{storage\_transport}$ | -20 | | 60 | °C | |
| Storage time during transport1) | $t_{storage\_transport}$ | | | 10 | Day | |

1) Not subject to production test. This parameter is verified by design/characterization.
2) Condensation and bedewing shall be avoided.

1 Number of desiccant units to be calculated according to JEDEC Standard 033.

### 4.1.3 Timing characteristics

**Table 4 Timing characteristics**

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Sampling time[1] | $t_{sampling}$ | 10 | 60 | 4095 | s | Sensor accuracy may be affected when sampling rates exceed 1 meas/min |
| Time to sensor ready[1] | $t_{sensor\_rdy}$ | | | 1 | s | |
| Time to early notification[1][2] | $t_{early\_noti}$ | | 2 | | s | |
| $I^2C$ clock frequency[1] | $f_{I2C}$ | | 100 | | kHz | |
| | | | 400 | | | |
| PWM frequency[1] | $f_{pwm}$ | | 80 | | Hz | |
| UART baud rate[1] | $f_{baud}$ | | 9.6 | | kbps | |

1) Not subject to production test. This parameter is verified by design/characterization.
2) Relevant for continuous mode of operation.

Typical measurement timing sequence for I$^2$C and UART is presented in Figure 4.

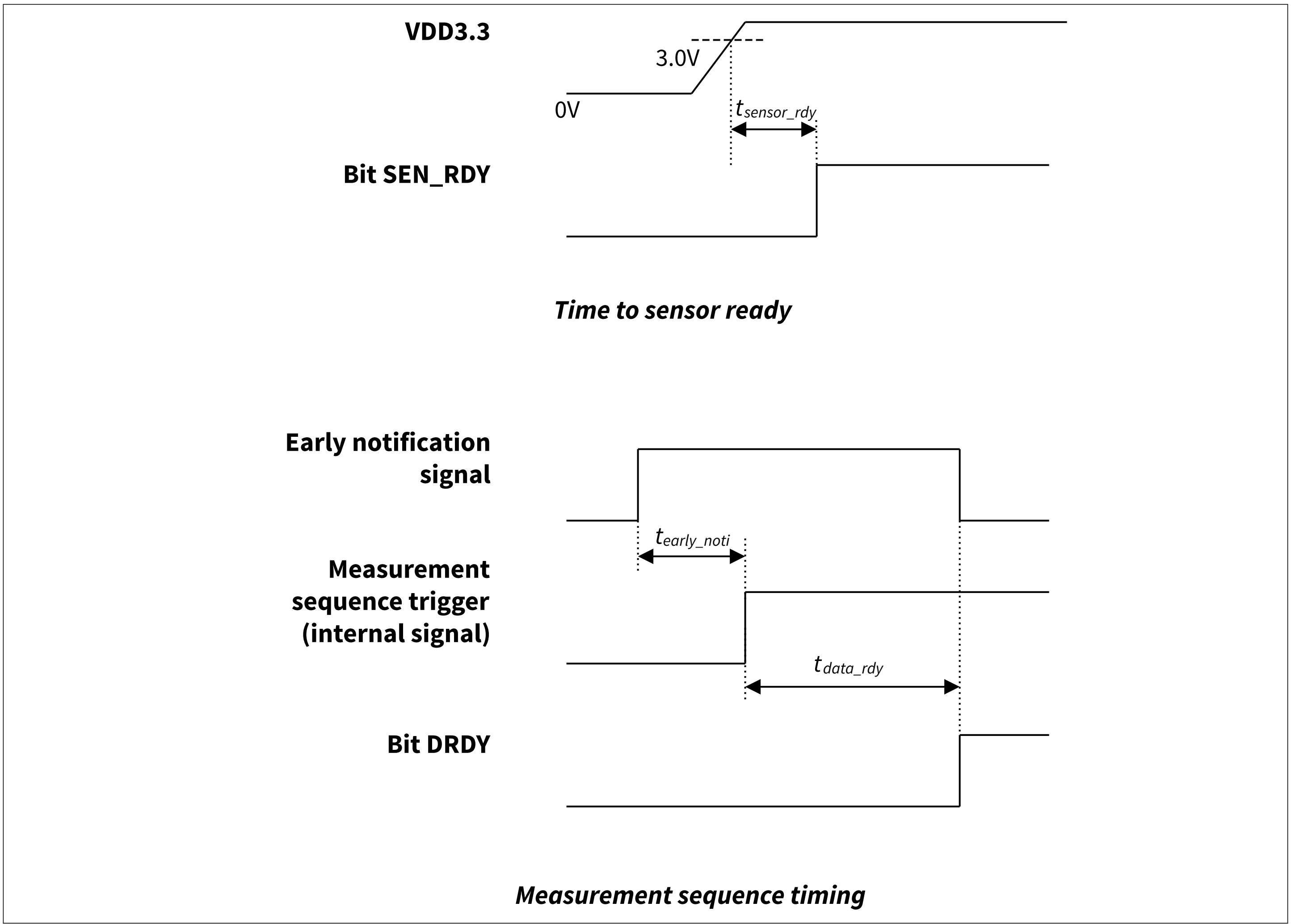


**Figure 4** **Illustration of the timing characteristic parameters**

### 4.1.4 Absolute maximum ratings

**Table 5 Absolute maximum ratings**

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| MSL level | MSL | | 3 | | | |
| Maximum ambient temperature | $T_{amb\_max}$ | -10 | | 60 | °C | |
| Maximum relative humidity | $rH_{max}$ | 0 | | 95 | % | |
| 12 V supply voltage | $V_{VDD12}$ | 9.6 | | 14.4 | V | |
| 3.3 V supply voltage | $V_{VDD3.3}$ | 3.0 | | 3.6 | V | |
| Reflow temperature | $T_r$ | | | 245 | °C | JEDEC J-STD-020E |
| ESD human body model | $V_{ESD\_HBM}$ | -2 | | 2 | kV | HBM (JS001) |
| ESD charge discharge model | $V_{ESD\_CDM}$ | | | 500 | V | CDM (JS002) |

***Note**: Stresses above the values listed as "Absolute Maximum Ratings" may cause permanent damage to the devices. Exposure to absolute maximum rating conditions for extended period of time may affect device reliability.*

### 4.1.5 Current rating and power consumption

All parameters specified in Table 5 refer to the following operating conditions unless otherwise specified: VDD3.3 = 3.3 V, VDD12 = 12.0 V, $T_{amb}$ = 25°C, % r.H. = 30%, $p$ = 1013 hPa.

**Table 6 Current rating**

| Parameter | Symbol | Pin | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Peak current[1)] | $I_{peak\ 5}$ | VDD12 | | 130 | 150 | mA | |
| Peak current[1)] | $I_{peak\ 3.3}$ | VDD3.3 | | 10 | | mA | |
| Average current[1)] | $I_{avg\ 5}$ | VDD12 | | 0.8 | | mA | At 1 meas/min |
| Average current[1)] | $I_{avg\ 3.3}$ | VDD3.3 | | 6.1 | | mA | At 1 meas/min |
| Average power[1)] | $P_{avg}$ | | | 30 | | mW | At 1 meas/min |

*1)* Not subject to production test. This parameter is verified by design/characterization.

### 4.1.6 $CO_2$ transfer function

All parameters specified in the following sections refer to the operating conditions unless otherwise specified: VDD3.3 = 3.3 V, VDD12 = 12.0 V, $T_{amb}$ = 25°C, % r.H. = 30%, $p$ = 1013 hPa, and $t_{sampling}$ = 1 meas/min.

**Table 7 $CO_2$ transfer function**

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Accuracy[1] | Acc | -30 ppm -3% of reading | | +30 ppm +3% of reading | ppm | $C_{CO2}$: 400-3000 ppm |
| | | | ±30 ppm +3% of reading | | | $C_{CO2}$: 3001-5000 ppm |
| Response time[2] | $t_{63}$ | | 90 | | s | |
| Resolution[2] | Res | | 1 | | ppm | |
| Repeatability[2] [3] | $R$ | | | 10 | ppm | 3 times standard deviation at fixed $C_{CO2}$: 1000 ppm |
| Pressure stability[2] | $p_{error}$ | | 0 | | %/hPa | With pressure compensation feature enabled |
| Acoustic stability[2] | $SPL_{error}$ | 3 | 6 | 15 | ppm | Up to 95 dB for pink noise from 100 Hz to 10 kHz |

1) Accuracy verified using certified calibration gas mixtures and high-precision reference sensors. Uncertainty in calibration gas mixtures of ±2% needs to be considered. Temporary deviations in accuracy caused by assembly, rough handling or harsh environmental conditions can be compensated using forced compensation scheme (FCS) or automatic baseline offset correction (ABOC).
2) Not subject to production test. This parameter is verified by design/characterization.
3) Stepwise Reaction IIR filter is enabled.

## 4.2 Digital interfaces

The XENSIV™ PAS CO2 supports I$^2$C, UART, and PWM. The I$^2$C and UART interfaces are described in detail in the following chapters.

### 4.2.1 I$^2$C interface

The device complies with the I$^2$C protocol. When I$^2$C is selected as a serial communication interface, the device acts as an I$^2$C slave. The main characteristics of the interface are described below:

- Slave mode only
- I$^2$C clock frequency: 100 kHz and 400 kHz
- 7-bit slave address: 0×28
- No CRC
- The device supports clock stretching
- 8-bit addressing mode supported (7-bit address + RW)
- Bulk read and write supported (device auto-increments automatically the address)
- Address 0×00 not supported

Further details of the protocol are covered in the separate application note.

### 4.2.1.1 I$^2$C transaction format

The I$^2$C transaction has the following structure: a start condition followed by four bytes followed a stop condition.

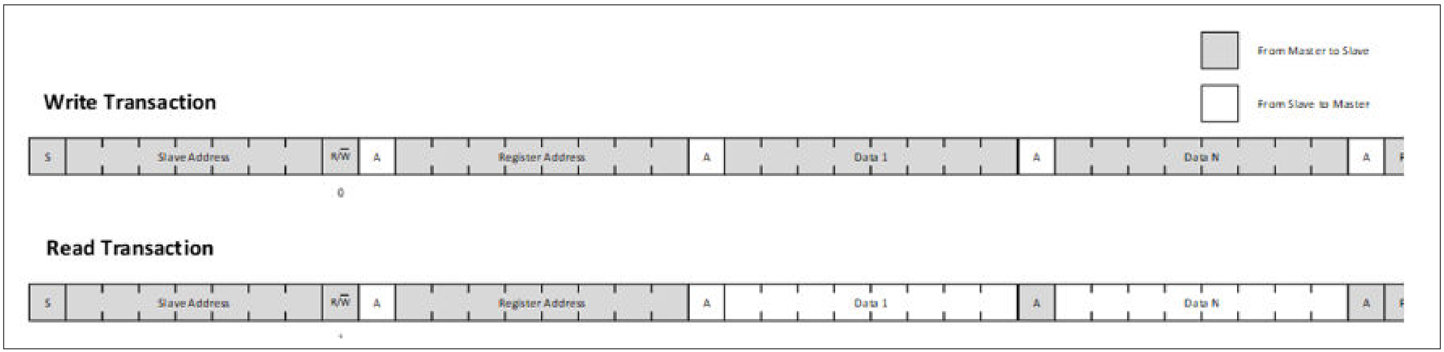


**Figure 5** I$^2$C write and read transaction

**Table 8** I$^2$C transaction

| Byte | Description | Value | Comments |
|---|---|---|---|
| | Start condition | | |
| 1 | Header | (Slave address << 1) \| R/W | |
| 2 | First data-byte | As per user request/register value | Read: data provided by the slave<br>Write: data provided by the user |
| N+2 | Data byte N | As per user request/register value | Read: data provided by the slave<br>Write: data provided by the user |
| | End condition | | |

### 4.2.1.2 I$^2$C timing characteristics

Due to the wired-AND configuration of an I$^2$C bus system, the port drivers on the SCL and SDA signal lines need to operate in open-drain mode. The high level of these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbits/s, approximately 2 kOhm for operation at 400 kbits/s.

**Table 9** I$^2$C standard mode timing

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Fall time of both SDA and SCL | t1 | | | 300 | ns | |
| Rise time of both SDA and SCL | t2 | | | 1000 | ns | |
| Data hold time | t3 | 0 | | | µs | |
| Data set-up time | t4 | 250 | | | ns | |
| LOW period of SCL clock | t5 | 4.7 | | | µs | |
| HIGH period of SCL clock | t6 | 4.0 | | | µs | |
| Hold time for a (repeated) START condition | t7 | 4.0 | | | µs | |
| Set-up time for (repeated) START condition | t8 | 4.7 | | | µs | |

**(table continues...)**

**Table 9** **(continued) I²C standard mode timing**

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Set-up time for STOP condition | t9 | 4.0 | | | µs | |
| Bus free time between a STOP and START condition | t10 | 4.7 | | | µs | |
| Capacitive load for each bus line | $C_b$ | | | 400 | pF | |

**Table 10** **I²C fast mode timing**

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Fall time of both SDA and SCL | t1 | 20 + 0.1*$C_b$ | | 300 | ns | $C_b$ refers to the total capacitance of one bus line in pF |
| Rise time of both SDA and SCL | t2 | 20 + 0.1*$C_b$ | | 300 | ns | $C_b$ refers to the total capacitance of one bus line in pF |
| Data hold time | t3 | 0 | | | µs | |
| Data set-up time | t4 | 100 | | | ns | |
| LOW period of SCL clock | t5 | 1.3 | | | µs | |
| HIGH period of SCL clock | t6 | 0.6 | | | µs | |
| Hold time for a (repeated) START condition | t7 | 0.6 | | | µs | |
| Set-up time for (repeated) START condition | t8 | 0.6 | | | µs | |
| Set-up time for STOP condition | t9 | 0.6 | | | µs | |
| Bus free time between a STOP and START condition | t10 | 1.3 | | | µs | |
| Capacitive load for each bus line | $C_b$ | | | 400 | pF | |

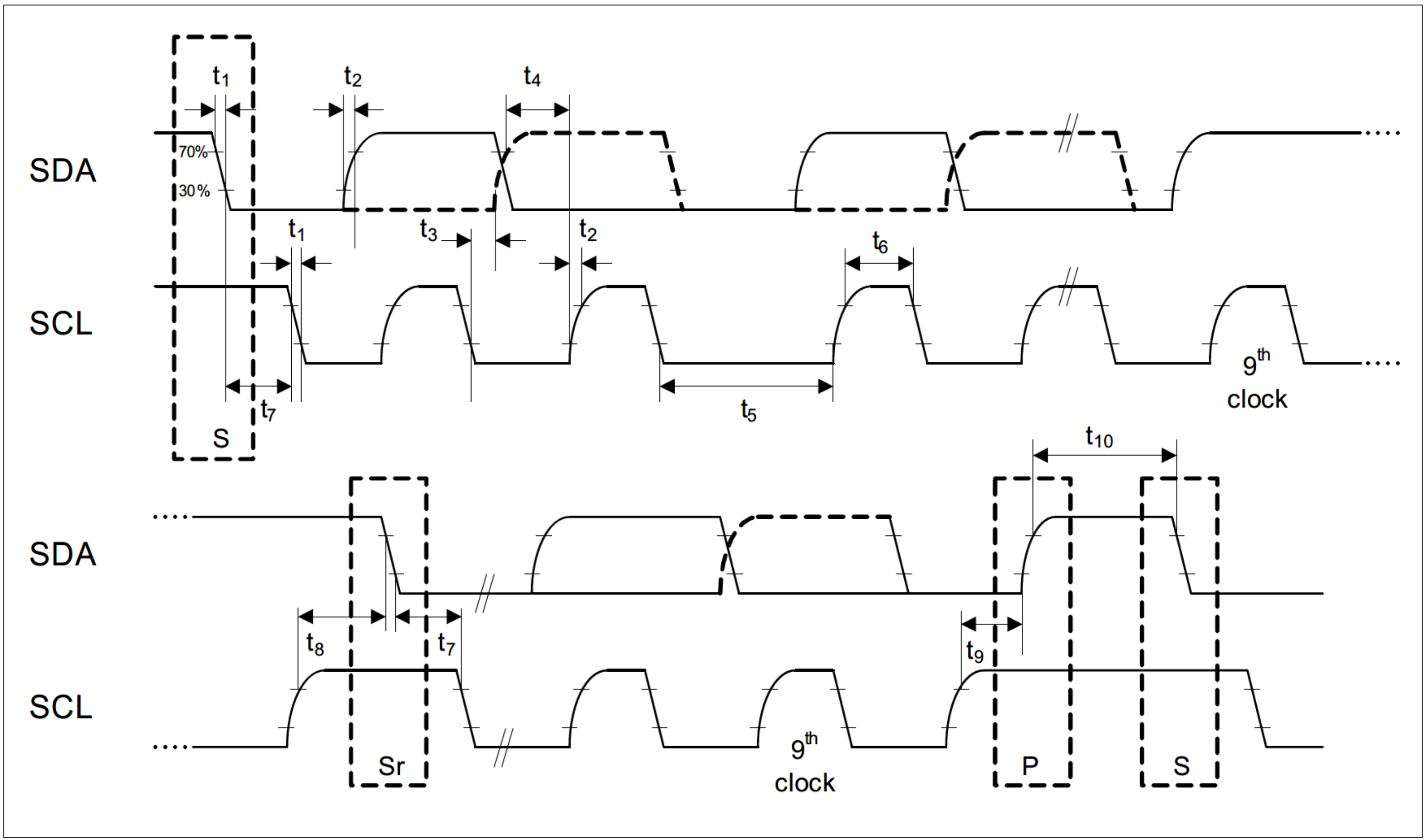


**Figure 6** $I^2C$ standard and fast mode timing

## 4.2.2 UART interface

When UART is selected as a serial communication interface, the device acts as a UART slave. The device operates via UART for point-to-point communication. Bus operation is not supported. As a result, it is recommended that the master uses a time-out mechanism. The basic format of a valid UART frame is 1 start bit, 8 data bits, no parity bit, and 1 stop bit. The master combines several UART frames into a message (read or write). The combination of master request and slave answer defines a transaction. The main characteristics of the interface are described below:

- Point to point operation – no bus support
- Slave operation only
- UART clock frequency = 9.6 kHz
- Format: 1 start bit, 8 data bits, no parity bit, 1 stop bit. Supports direct connection with a terminal program

## 4.3 Application circuit examples

### 4.3.1 I²C application circuit example

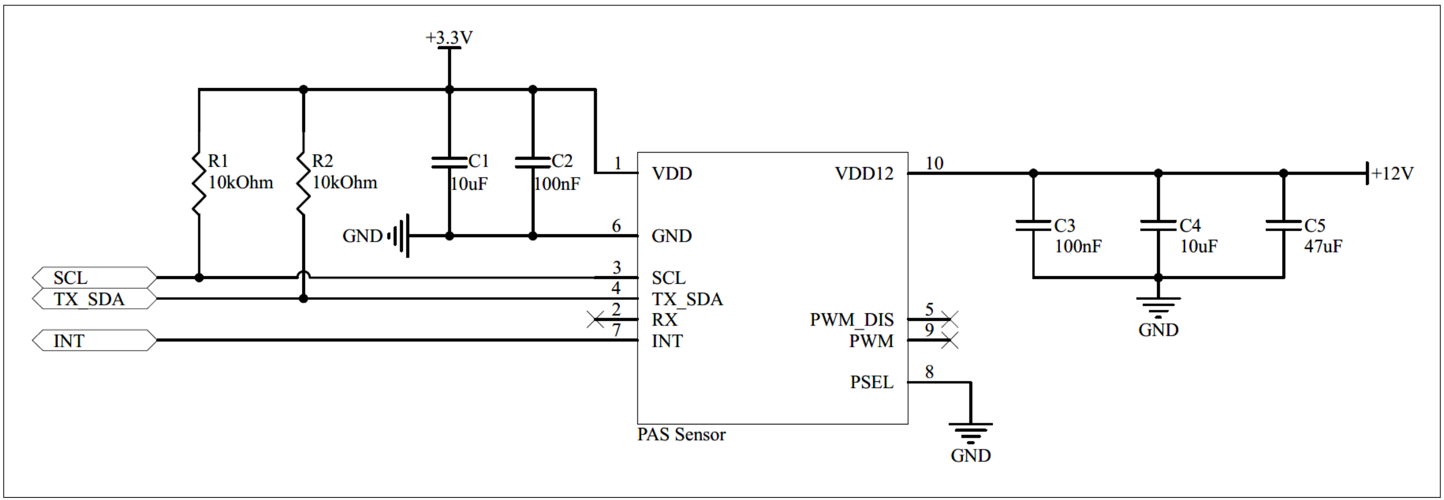


**Figure 7 Application circuit example for I²C**

With this configuration, the device will start in Idle mode of operation. Internal pull up is present on PWM_DIS pin.

### 4.3.2 UART application circuit example

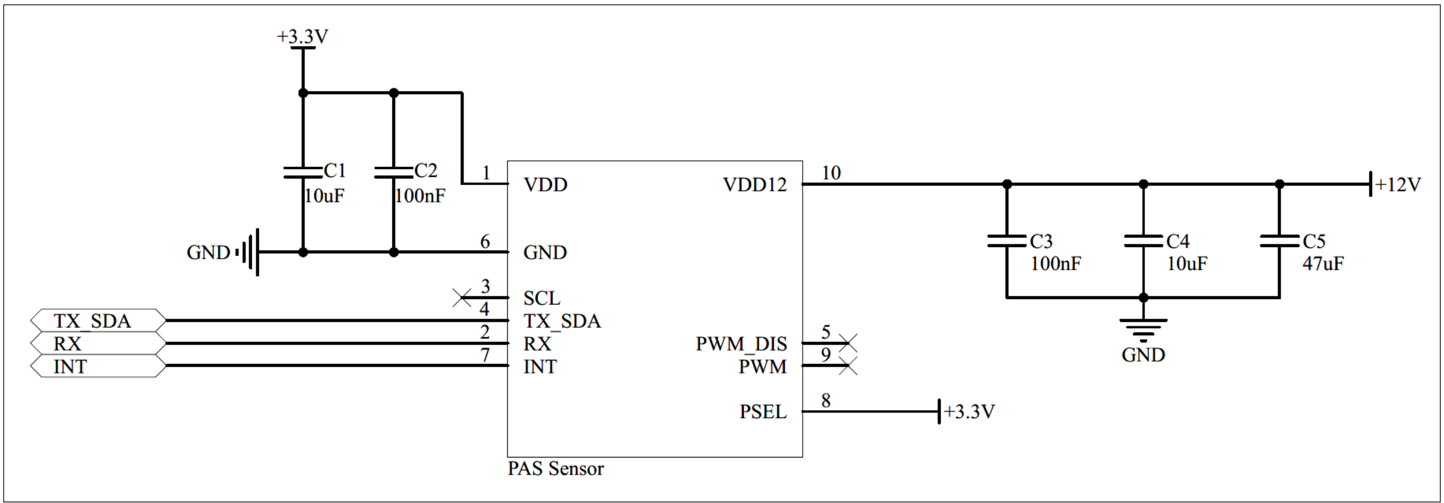


**Figure 8 Application circuit example for UART**

With this configuration, the device will start in Idle mode of operation. Internal pull up is present on PWM_DIS pin.

### 4.3.3 PWM application circuit example

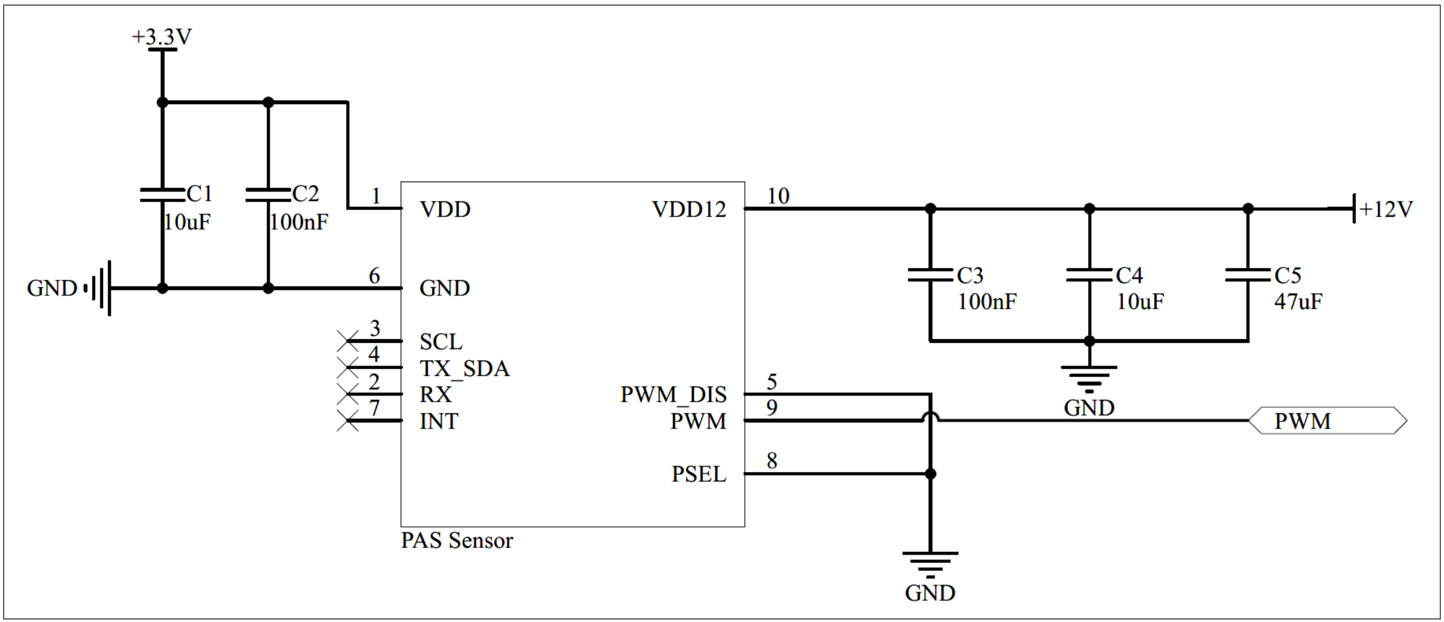


**Figure 9** **Application circuit example for PWM**

With this configuration, the device will start in continuous mode of operation with sampling time of 1 meas/min.

## 4.4 Functional description

This section describes the operation of the sensor while measuring $CO_2$ concentrations. At any moment, the device can be in one out of two different states: active and inactive. At active state, the CPU controlling the device is operating and can perform tasks, such as: running a measurement sequence, serving an interrupt, and so on. When the device has no specific task to perform, it goes to an inactive state. A transition from active to inactive state may occur at the end of a measurement sequence. Several events can wake up the device: the reception of a message on the serial communication interface, a falling edge on pin **PWM_DIS**, the internal generation of a measurement request in continuous measurement mode.

### 4.4.1 Operating modes

The operating mode can be programmed via the serial communication interface by using the bit field **MEAS_CFG.OP_MODE**.

The sensor module supports three operating modes:

- **Idle mode:** The device does not perform any $CO_2$ concentration measurement. The device remains inactive until it becomes active shortly to serve interrupts before going back to an inactive state
- **Continuous mode:** In this mode, the device periodically triggers a $CO_2$ concentration measurement sequence. Once a measurement sequence is completed, the device goes back to an inactive state and wakes up automatically for the next measurement sequence. The measurement period is programmable from 5 s to 4095 s
- **Single-shot mode:** In this mode, the device triggers a single measurement sequence. At the end of the measurement sequence, the device goes back automatically to idle mode

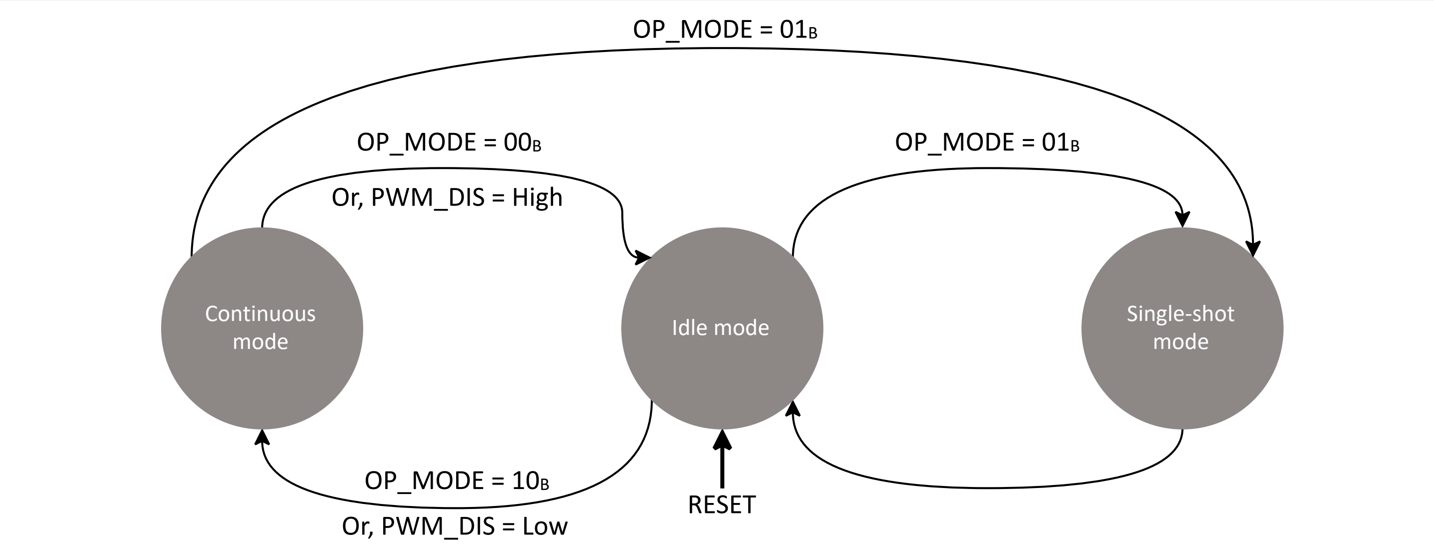


**Figure 10 Operating mode transition**

### 4.4.2 Data post-processing

Once the $CO_2$ concentration data has been acquired, several post-processing schemes can be applied to utilize different functionality.

#### 4.4.2.1 Pressure compensation

The $CO_2$ concentration value acquired by the sensor is dependent on the external atmospheric pressure. To compensate for this effect, the application system can provide the value of the atmospheric pressure by writing into the specific registers, that is, **PRES_REF_H** and **PRES_REF_L**. At the end of a measurement sequence, the device reads the pressure value and applies for compensation on the $CO_2$ concentration value before storing it into the result registers.

#### 4.4.2.2 Automatic baseline offset correction

To correct slow drifts caused by aging during operation, the device supports automatic baseline offset compensation. Every week of operation, the device computes an offset to correct the baseline of the device. The device must be in contact with the reference concentration (for example, fresh air at 400 ppm of $CO_2$ concentration) at least 30 minutes per operating week to make sure proper baseline compensation. The device supports different configurations for compensation. The ABOC set point may only be set between 350 and 1500 ppm.

#### 4.4.2.3 Forced compensation

Forced compensation provides a means to speed up the offset compensation process. Before forced compensation is enabled, the device shall be physically exposed to the reference $CO_2$ concentration. The device will use the next three measurements to calculate the compensation offset. The user shall ensure constant exposure to the reference $CO_2$ concentration during that time. It is recommended to operate at one measurement per 10 seconds while implementing the forced compensation scheme. When three measurement sequences are completed, the device automatically reconfigures itself with the newly computed offset applied to the subsequent $CO_2$ concentration measurement results. The forced compensation offset can be stored to the non-volatile memory by using the corresponding command (SENS_RST = 0xCF).

### 4.4.2.4 Alarm threshold

The device can be configured via interrupt to perform an alarm threshold check each time a new $CO_2$ concentration data is acquired. At the end of each measurement sequence, the computed $CO_2$ value (after all applicable offset compensations) is compared to the concatenated value in **ALARM_TH_H** and **ALARM_TH_L**. In case of a threshold violation, the sticky bit **MEAS_STS.ALARM** is set. This also sets pin **INT** to active level due to configuration as alarm. Bit **MEAS_STS.ALARM** is cleared by reading register **MEAS_STS.ALARM_CLR**.

## 4.5 Monitoring mechanism as advanced functionality

The device supports several mechanisms to monitor the correct operation of the sensor.

**Table 11 Functionality description**

| Mechanism | Description |
|---|---|
| Sensor ready status | After each power-on reset, bit **SENS_STS.SEN_RDY** is set to confirm that the sensor has initialized correctly |
| Scratchpad register | To check the integrity of the communication layer of the serial communication interface, register **SCRATCH_PAD** can be used. This register can use this memory field to write any value and verify that the data received by the device is correct.<br>It can also be used to verify that a soft reset has been executed, using the following sequence:<br>**1.** The user writes a non-default value to register **SCRATCH_PAD**<br>**2.** The user reads back register **SCRATCH_PAD** to verify the writ commend has been correctly executed<br>**3.** The user writes register **SENS_RST** to trigger a soft reset<br>**4.** The user reads register **SCRATCH_PAD** to verify that it has been reset to its default value |
| VDD12V verification | At power-up and the beginning of each measurement sequence, the device automatically measures the voltage at **VDD12**. If the measured voltage exceeds the specified operating range of the device, bit **SENS_STS.ORVS** is set. The measurement sequence is, however, completed normally. Bit **SENS_STS.ORVS** can be cleared by setting bit **SENS_STS.ORVS_CLR** |
| Internal temperature verification | At the beginning of each measurement sequence, the device automatically measures its internal temperature. If the measured temperature exceeds the specified operating ranged of the device, sticky bit **SENS_STS.ORTMP** is set. The measurement sequence is, however, completed normally. Bit **SENS_STS.ORTMP** can be cleared by setting bit **SENS_STS.ORTMP_CLR** |

# 5 Register map

## 5.1 Register map access method

The registers that can be accessed by the user's application via the communication interfaces are covered here. Registers need to be addressed byte-wise.

**Table 12 Bit access terminology**

| Mode | Symbol | Description |
|---|---|---|
| Read/Write | rw | This bit or bitfield can be written or read |
| Read | r | This bit or bitfield is read-only |
| Write | w | This bit or bitfield is write-only (read as $0_H$) |
| Read/Write hardware or firmware affected | rwh | As rw, but bit or bitfield can also be modified by hardware or firmware |
| Read hardware or firmware affected | rh | As r, but bit or bitfield can also be modified by hardware or firmware |
| Sticky | s | Bits with this attribute are "sticky" in one direction. If their reset value is overwritten once they can be switched again into their reset state only by a reset operation. Software and internal logic (except reset-like functions) cannot switch this type of bit into its reset state by writing directly to the register. The sticky attribute can be combined with other functions (for example, "rh") |
| Reserved/not implemented | 0 | Bitfields named "0" indicate functions not implemented. They have the following behavior:<br>• Reading these bitfields returns $0_H$<br>• Writing these bitfields has no effect<br>These bitfields are reserved. When writing, software should always set such bitfields to $0_H$ to preserve compatibility with future products |
| Reserved/not defined | Res | Certain bitfields or bit combinations in a bitfield can be marked as "Reserved", indicating that the behavior of the device is undefined for that combination of bits. Setting the register to such an undefined value may lead to unpredictable results. When writing, the software must always set such bitfields to legal values |

## 5.2 Register map bitfields

**Table 13 Register map**

| Name | Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
|---|---|---|---|---|---|---|---|---|---|---|
| **PROD_ID** | **0x00** | PROD | | | REV | | | | | 0x4F<br>0x60* |
| **SENS_STS** | **0x01** | SEN_RDY | PWM_DIS_ST | ORTMP | ORVS | ICCER | ORTMP_CLR | ORVS_CLR | ICCER_CLR | 0xC0 |
| **MEAS_RATE_H** | **0x02** | 0 | | | | VAL | | | | 0x00 |
| **MEAS_RATE_L** | **0x03** | VAL | | | | | | | | 0x3C |
| **MEAS_CFG** | **0x04** | Reserved | | PWM_OUTEN | PWM_MODE | BOC_CFG | | OP_MODE | | 0x24 |
| **CO2PPM_H** | **0x05** | VAL | | | | | | | | 0x00 |
| **CO2PPM_L** | **0x06** | VAL | | | | | | | | 0x00 |
| **MEAS_STS** | **0x07** | 0 | | Reserved | DRDY | INT_STS | ALARM | INT_STS_CLR | ALARM_CLR | 0x00 |
| **INT_CFG** | **0x08** | 0 | | | INT_TYP | INT_FUNC | | | ALARM_TYP | 0x11 |
| **ALARM_TH_H** | **0x09** | VAL | | | | | | | | 0x00 |
| **ALARM_TH_L** | **0x0A** | VAL | | | | | | | | 0x00 |
| **PRES_REF_H** | **0x0B** | VAL | | | | | | | | 0x03 |
| **PRES_REF_L** | **0x0C** | VAL | | | | | | | | 0xF7 |
| **CALIB_REF_H** | **0x0D** | VAL | | | | | | | | 0x01 |
| **CALIB_REF_L** | **0x0E** | VAL | | | | | | | | 0x90 |
| **SCRATCH_PAD** | **0x0F** | VAL | | | | | | | | 0x00 |
| **SENS_RST** | **0x10** | SRTRG | | | | | | | | 0x00 |

***Note***:
- *Registers with addresses 0x11 to 0x14 are reserved and must not be accessed. Any read or write operation to these registers will result in a communication error.*
- *Registers with addresses 0x15 to 0xFF are reserved and must not be accessed. Any read or write operation to these registers will result in a non-acknowledge error.*

## 5.3 Product and revision ID register (PROD_ID)

This register displays the device's product and version ID. Write accesses to this register are ignored.

| | | |
|---|---|---|
| PROD_ID | **Address:** | $0x00_H$ |
| Product and revision ID register | **Reset value:** | $0x4F/0x60_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **PROD** | | | **REV** | | | | |
| r | | | r | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| PROD | 7:5 | r | **Product ID**<br>This bitfield indicates the product type.<br>$001_B$: Reserved<br>$010_B$: PASCO2V01<br>$011_B$: PASCO2V15 |
| REV | 4:0 | r | **Revision ID**<br>This bitfield indicates the product and firmware revision.<br>$0001_B$: Revision 1.<br>$0010_B$: Revision 2.<br>$0011_B$: Revision 3.<br>... |

## 5.4 Sensor status register (SENS_STS)

This register displays and controls the status of the sensor. Write accesses to the read-only bits of this register are ignored.

| | | |
|---|---|---|
| SENS_STS | **Address:** | $0x01_H$ |
| Sensor status register | **Reset value:** | $0xC0_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **SEN_RDY** | **PWM_DIS_ST** | **ORTMP** | **ORVS** | **ICCER** | **ORTMP_CLR** | **ORVS_CLR** | **ICCER_CLR** |
| rh | rh | rhs | rhs | rhs | w | w | w |

| Field | Bits | Type | Description |
|---|---|---|---|
| SEN_RDY | 7 | rh | **Sensor ready bit**<br>This bit indicates if the initialization of the sensor after power-on reset has been performed correctly.<br>$0_B$: The sensor has not been initialized correctly.<br>$1_B$: The sensor has been initialized correctly. |

**(table continues...)**

**(continued)**

| Field | Bits | Type | Description |
|---|---|---|---|
| PWM_DIS_ST | 6 | rh | **PWM_DIS pin status**<br>This bit indicates the level read at pin **PWM_DIS**.<br>$0_B$: A low level is read at pin **PWM_DIS**.<br>$1_B$: A high level is read at pin **PWM_DIS**.<br>***Note**: This bit is updated at every transition at pin **PWM_DIS**.* |
| ORTMP | 5 | rhs | **Out-of-range temperature error bit (sticky bit)**<br>This bit indicates if a condition where the temperature has been outside the specified valid range has been detected.<br>$0_B$: No error has occurred.<br>$1_B$: An error has occurred.<br>This bit is cleared by setting **SENS_STS.ORTMP_CLR**. |
| ORVS | 4 | rhs | **Out-of-range VDD12V error bit (sticky bit)**<br>This bit indicates if a condition where VDD12V has been outside the specified valid range has been detected.<br>$0_B$: No error has occurred.<br>$1_B$: An error has occurred.<br>This bit is cleared by setting bit **SENS_STS.ORVS_CLR**. |
| ICCER | 3 | rhs | **Communication error notification bit (sticky bit)**<br>This bit indicates if a non-valid command has been received by the serial communication interface.<br>$0_B$: No invalid command received.<br>$1_B$: An invalid command has been received.<br>This bit is cleared by setting **SENS_STS.ICCER_CLR**. |
| ORTMP_CLR | 2 | w | **Out-of-range temperature error clear bit**<br>Writing this bit with $1_B$ clears the sticky bit **SENS_STS.ORTMP**.<br>This bit is read back as $0_B$. |
| ORVS_CLR | 1 | w | **Out-of-range VDD12V error clear bit**<br>Writing this bit with $1_B$ clears the sticky bit **SENS_STS.ORVS**.<br>This bit is read back as $0_B$. |
| ICCER_CLR | 0 | w | **Communication error clear bit**<br>Writing this bit with $1_B$ clears the sticky bit **SENS_STS.ICCER**.<br>This bit is read back as $0_B$. |

## 5.5 Measurement period configuration registers (MEAS_RATE_H)

Registers **MEAS_RATE_H** and **MEAS_RATE_L** define the measurement period used in continuous mode. The concatenation of **MEAS_RATE_H** (MSB) and **MEAS_RATE_L** (LSB) define the period. The concatenated value is coded as a two's complement signed short integer (1 bit = 1 s).

Values above $0FFF_H$ are treated as being equal to $FFF_H$ (4095 s). Values below $0005_H$ are treated as being equal to $0005_H$ (5 s).

Writing a non-valid value to this field generates a communication error (bit **SENS_STS.ICCER** set).

***Note**: When writing to **MEAS_RATE_H** and **MEAS_RATE_L**, the new value is not immediately considered by the device. It is internally latched at the next transition from idle to continuous mode.*

| MEAS_RATE_H | **Address:** | $0x02_H$ |
|---|---|---|
| Measurement period configuration registers | **Reset value:** | $0x00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **0** | | | | **VAL** | | | |
| rw | | | | rwh | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| 0 | 7:4 | rw | **Reserved**<br>This bitfield shall be written with $0_H$. |
| VAL | 3:0 | rwh | **MSB of the measurement period in continuous mode**<br>The concatenation of this value with bitfield **MEAS_RATE_L** defines the measurement period in continuous mode.<br>***Note**: Values above $0F_H$ reserved. Writing a non-valid value to this field generates a communication error (bit **SENS_STS.ICCER** set) and sets the bitfield to $0F_H$.* |

## 5.6 Measurement period configuration registers (MEAS_RATE_L)

Registers **MEAS_RATE_H** and **MEAS_RATE_L** define the measurement period used in continuous mode. The concatenation of **MEAS_RATE_H** (MSB) and **MEAS_RATE_L** (LSB) define the period. The concatenated value is coded as a two's complement signed short integer (1 bit = 1 s).

Values above $0FFF_H$ are treated as being equal to $FFF_H$ (4095 s). Values below $0005_H$ are treated as being equal to $0005_H$ (5 s).

Writing a non-valid value to this field generates a communication error (bit **SENS_STS.ICCER** set).

***Note**: When writing to **MEAS_RATE_H** and **MEAS_RATE_L**, the new value is not immediately considered by the device. It is internally latched at the next transition from idle to continuous mode.*

| MEAS_RATE_L | **Address:** | $0x03_H$ |
|---|---|---|
| Measurement period configuration registers | **Reset value:** | $0x3C_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **VAL** | | | | | | | |
| rwh | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| VAL | 7:0 | rwh | **LSB of the measurement period in continuous mode**<br>The concatenation of this value with bitfield **MEAS_RATE_H.VAL** defines the measurement period in continuous mode.<br>***Note**: Values $00_H$ to $04_H$ are reserved. Writing a non-valid value to this field generates a communication error (bit **SENS_STS.ICCER** set) and sets the bitfield to $05_H$.* |

## 5.7 Measurement mode configuration register (MEAS_CFG)

This register defines the operation settings of the device.

| | | |
|---|---|---|
| MEAS_CFG | **Address:** | $0x04_H$ |
| Measurement mode configuration register | **Reset value:** | $0x24_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **Res** | | **PWM_OUTEN** | **PWM_MODE** | **BOC_CFG** | | **OP_MODE** | |
| rwh | | rwh | rw | rwh | | rwh | |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 7:6 | rwh | **Reserved**<br>This bitfield shall be written with $00_B$. |
| PWM_OUTEN | 5 | rwh | **PWM output software enable bit**<br>$0_B$: **PWM** output is disabled by software.<br>$1_B$: **PWM** output is enabled by software.<br>***Notes**:*<br>***1.** The actual state of pin **PWM** depends on both **MEAS_CFG.PWM_OUTEN** and pin **PWM_DIS**.*<br>***2.** This bit is automatically set at a high to low transition at pin **PWM_DIS**.* |
| PWM_MODE | 4 | rw | **PWM mode configuration**<br>$0_B$: PWM single-pulse mode.<br>$1_B$: PWM pulse-train mode. |

**(table continues...)**

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| BOC_CFG | 3:2 | rwh | **Baseline offset compensation configuration**<br>$00_B$: Automatic baseline offset compensation (ABOC) disabled.<br>$01_B$: ABOC enabled. The offset is periodically updated at each BOC computation.<br>***Note**: With firmware version 2.18 an extended ABOC functionality has been introduced, including support for single shot mode.*<br>$10_B$: Forced compensation.<br>***Note**: After the forced compensation is done, device automatically reconfigures itself into ABOC (**MEAS_CFG.BOC_CFG** = $01_B$).*<br>$11_B$: Reserved. |
| OP_MODE | 1:0 | rwh | **Sensor operating mode**<br>$00_B$: Idle mode.<br>$01_B$: Single-shot mode enabled. Writing $01_B$ to this field triggers a single measurement sequence. This field is reset by firmware automatically.<br>$10_B$: Continuous mode enabled.<br>$11_B$: Reserved (as $00_B$). |

## 5.8 $CO_2$ concentration result register (CO2PPM_H)

Registers **CO2PPM_H** and **CO2PPM_L** are used to display the result of the last $CO_2$ concentration measurement. The concatenation of **CO2PPM_H** (MSB) and **CO2PPM_L** (LSB) define the $CO_2$ concentration value. The concatenated $CO_2$ concentration value is coded as a two's complement signed short integer (1 bit = 1 ppm). This field is updated at the end of each measurement sequence.

Reading register **CO2PPM_L** clears bit **MEAS_STS.DRDY**.

When reading the $CO_2$ concentration value, the user shall first read registers **CO2PPM_H** and then **CO2PPM_L**.

| | | |
|---|---|---|
| CO2PPM_H | **Address:** | $0x05_H$ |
| $CO_2$ concentration result register | **Reset value:** | $0x00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **VAL** | | | | | | | |
| rh | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| VAL | 7:0 | rh | **MSB of the $CO_2$ concentration value**<br>The concatenation of this value with bitfield **CO2PPM_L.VAL** gives the $CO_2$ concentration value. |

## 5.9 $CO_2$ concentration result register (CO2PPM_L)

Registers **CO2PPM_H** and **CO2PPM_L** are used to display the result of the last $CO_2$ concentration measurement. The concatenation of **CO2PPM_H** (MSB) and **CO2PPM_L** (LSB) define the $CO_2$ concentration value. The concatenated $CO_2$ concentration value is coded as a two's complement signed short integer (1 bit = 1 ppm). This field is updated at the end of each measurement sequence.

Reading register **CO2PPM_L** clears bit **MEAS_STS.DRDY**.

When reading the $CO_2$ concentration value, the user shall first read registers **CO2PPM_H** and then **CO2PPM_L**.

| | | |
|---|---|---|
| CO2PPM_L | **Address:** | $0x06_H$ |
| $CO_2$ concentration result register | **Reset value:** | $0x00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **VAL** | | | | | | | |
| rh | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| VAL | 7:0 | rh | **LSB of the $CO_2$ concentration value**<br>The concatenation of this value with bitfield **CO2PPM_H.VAL** gives the $CO_2$ concentration value.<br>Reading this bitfield clears bit **MEAS_STS.DRDY**. |

## 5.10 Measurement status register (MEAS_STS)

This register displays the status information of the sensor. Write accesses to the read-only bits of this register are ignored.

| | | |
|---|---|---|
| MEAS_STS | **Address:** | $0x07_H$ |
| Measurement status register | **Reset value:** | $0x00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **0** | | **Res** | **DRDY** | **INT_STS** | **ALARM** | **INT_STS_CLR** | **ALARM_CLR** |
| rw | | rh | rhs | rhs | rhs | w | w |

| Field | Bits | Type | Description |
|---|---|---|---|
| 0 | 7:6 | rw | **Reserved**<br>This bitfield is read as $00_B$. |
| Res | 5 | rh | **Reserved**<br>This bit is reserved. |
| DRDY | 4 | rhs | **Data ready bit (sticky bit)**<br>This bit indicates if new data are available in register **CO2PPM_H** and **CO2PPM_L**.<br>$0_B$: No new data are available.<br>$1_B$: Unread data are available. This bit is set at the end of every measurement sequence.<br>This bit is cleared by reading **CO2PPM_L**. |

**(table continues...)**

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| INT_STS | 3 | rhs | **INT pin status bit**<br>This bit indicates if pin **INT** has been latched to active state (in case of alarm or data ready).<br>$0_B$: Pin **INT** has not been latched to active state.<br>$1_B$: Pin **INT** has been latched to active state. This bit is set at the end of every measurement sequence in case of a latching condition.<br>This bit is cleared by setting bit **MEAS_STS.INT_STS_CLR**. |
| ALARM | 2 | rhs | **Alarm notification (sticky bit)**<br>This bit indicates if a threshold violation occurred.<br>$0_B$: No violation occurred.<br>$1_B$: Violation occurred. This bit is set at the end of every measurement sequence in case of violation.<br>This bit is cleared by setting bit **MEAS_STS.ALARM_CLR**. |
| INT_STS_CLR | 1 | w | **INT pin status clear bit**<br>Writing this bit with $1_B$ clears the sticky bit **MEAS_STS.INT_STS** and forces pin **INT** to inactive level.<br>This bit is read back as $0_B$. |
| ALARM_CLR | 0 | w | **Alarm notification clear bit**<br>Writing this bit with $1_B$ clears the sticky bit **MEAS_STS.ALARM**.<br>This bit is read back as $0_B$. |

## 5.11 Interrupt pin configuration register (INT_CFG)

This register defines the configuration of pin **INT**.

INT_CFG **Address:** $0x08_H$

Interrupt pin configuration register **Reset value:** $0x11_H$

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **0** | | | **INT_TYP** | **INT_FUNC** | | | **ALARM_TYP** |
| rw | | | rw | rw | | | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| 0 | 7:5 | rw | **Reserved**<br>This bitfield shall be written with $00_B$. |
| INT_TYP | 4 | rw | **Pin INT electrical configuration**<br>$0_B$: Pin **INT** is configured as push-pull and low active.<br>$1_B$: Pin **INT** is configured as push-pull and high active.<br>***Note**: Writing this bitfield forces pin **INT** to inactive state.* |

(table continues...)

**(continued)**

| Field | Bits | Type | Description |
|---|---|---|---|
| INT_FUNC | 3:1 | rw | **Pin INT function configuration**<br>$000_B$: Pin **INT** is inactive.<br>$001_B$: Pin **INT** is configured as alarm threshold violation notification pin.<br>$010_B$: Pin **INT** is configured as data ready notification pin.<br>$011_B$: Pin **INT** is configured as sensor busy notification pin.<br>$100_B$: Pin **INT** is configured as early measurement start notification pin (this function only is available in continuous mode with **MEAS_CFG.OP_MODE** = $10_B$, otherwise the pin is inactive).<br>$101_B$: Reserved<br>…<br>$111_B$: Reserved |
| ALARM_TYP | 0 | rw | **Alarm type configuration bit**<br>This bitfield defines if an alarm is issued in case of lower or higher threshold violation.<br>$0_B$: Crossing down – the concatenated value of register **ALARM_TH_H** and **ALARM_TH_L** is defined as a lower threshold register.<br>$1_B$: Crossing up – the concatenated value of register **ALARM_TH_H** and **ALARM_TH_L** is defined as a higher threshold register. |

## 5.12 Alarm threshold register (ALARM_TH_H)

Registers **ALARM_TH_H** and **ALARM_TH_L** define the value used as a threshold for the alarm violation. The concatenation of **ALARM_TH_H** (MSB) and **ALARM_TH_L** (LSB) define the threshold value that shall be considered by the device. The concatenated alarm threshold value is coded as a 2's complement signed short integer (1 bit = 1 ppm).

| | | |
|---|---|---|
| ALARM_TH_H | **Address:** | $0x09_H$ |
| Alarm threshold register | **Reset value:** | $0x00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **VAL** | | | | | | | |
| rw | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| VAL | 7:0 | rw | **MSB of the alarm threshold**<br>The concatenation of this value with bitfield **ALARM_TH_L.VAL** defines the threshold value. |

## 5.13 Alarm threshold register (ALARM_TH_L)

Registers **ALARM_TH_H** and **ALARM_TH_L** define the value used as a threshold for the alarm violation. The concatenation of **ALARM_TH_H** (MSB) and **ALARM_TH_L** (LSB) define the threshold value that shall be considered by the device. The concatenated alarm threshold value is coded as a 2's complement signed short integer (1 bit = 1 ppm).

| | | |
|---|---|---|
| ALARM_TH_L | **Address:** | $0x0A_H$ |
| Alarm threshold register | **Reset value:** | $0x00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **VAL** | | | | | | | |
| rw | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| VAL | 7:0 | rw | **LSB of the alarm threshold**<br>The concatenation of this value with bitfield **ALARM_TH_H.VAL** defines the threshold value. |

## 5.14 Pressure compensation registers (PRES_REF_H)

Registers **PRES_REF_L** and **PRES_REF_H** are used to capture the atmospheric pressure to be compensated. The concatenation of **PRES_REF_H** (MSB) and **PRES_REF_L** (LSB) define the pressure value that shall be considered by the device. The concatenated pressure value is coded as an unsigned short integer (1 bit = 1 hPa). Since even small variations of the external pressure may lead to significant changes in the output provided by the sensor, it must be ensured that a coherent value is available for the sensor. For that purpose, **PRES_REF_H** and **PRES_REF_L** are associated with two internal shadow registers from which the device reads the pressure value to be used by the internal firmware. When writing to **PRES_REF_L**, the complete 16-bit pressure value is loaded into the shadow registers. When writing to **PRES_REF_H**, the shadow registers are not updated. Therefore, to update the pressure value, the user has to write first **PRES_REF_H** and then **PRES_REF_L**.

Pressure compensation is de facto deactivated if the default value is not updated.

For correct operation, the user shall ensure that pressure value programmed is within the specified pressure operating range of the device. The valid range of operation is 750 hPa to 1150 hPa.

Values below 750 hPa will be treated as 750 hPa (register automatically updated). Similarly, values above 1150 hPa will be treated at 1150 hPa (register automatically updated). If a value outside this range is written, bit **SENS_STS.ICCER** is set.

| | | |
|---|---|---|
| PRES_REF_H | **Address:** | $0x0B_H$ |
| Pressure compensation registers | **Reset value:** | $0x03_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **VAL** | | | | | | | |
| rwh | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| VAL | 7:0 | rwh | **MSB of the pressure compensation value**<br>The concatenation of this value with bitfield **PRESS_REF_L.VAL** gives the pressure compensation value. |

## 5.15 Pressure compensation registers (PRES_REF_L)

Registers **PRES_REF_L** and **PRES_REF_H** are used to capture the atmospheric pressure to be compensated. The concatenation of **PRES_REF_H** (MSB) and **PRES_REF_L** (LSB) define the pressure value that shall be considered by the device. The concatenated pressure value is coded as an unsigned short integer (1 bit = 1 hPa). Since even small variations of the external pressure may lead to significant changes in the output provided by the sensor, it must be ensured that a coherent value is available for the sensor. For that purpose, **PRES_REF_H** and **PRES_REF_L** are associated with two internal shadow registers from which the device reads the pressure value to be used by the internal firmware. When writing to **PRES_REF_L**, the complete 16-bit pressure value is loaded into the shadow registers. When writing to **PRES_REF_H**, the shadow registers are not updated. Therefore, to update the pressure value, the user has to write first **PRES_REF_H** and then **PRES_REF_L**.

Pressure compensation is de facto deactivated if the default value is not updated.

For correct operation, the user shall ensure that pressure value programmed is within the specified pressure operating range of the device. The valid range of operation is 750 hPa to 1150 hPa.

Values below 750 hPa will be treated as 750 hPa (register automatically updated). Similarly, values above 1150 hPa will be treated at 1150 hPa (register automatically updated). If a value outside this range is written, bit **SENS_STS.ICCER** is set.

| | | |
|---|---|---|
| PRES_REF_L | **Address:** | $0x0C_H$ |
| Pressure compensation registers | **Reset value:** | $0xF7_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **VAL** | | | | | | | |
| rwh | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| VAL | 7:0 | rwh | **LSB of the pressure compensation value**<br>The concatenation of this value with bitfield **PRESS_REF_H.VAL** gives the pressure compensation value. |

## 5.16 Automatic baseline offset compensation reference (CALIB_REF_H)

Registers **CALIB_REF_H** and **CALIB_REF_L** define the reference value used for the ABOC and the force calibration. The concatenation of **CALIB_REF_H** (MSB) and **CALIB_REF_L** (LSB) define the reference value. The concatenated offset value is coded as a two's complement signed short integer (1 bit = 1 ppm).

Values must be comprised between 350 ppm and 1500 ppm. Values below 350 ppm will be treated as 350 ppm (register automatically updated). Similarly, values above 1500 ppm will be treated at 1500 ppm (register automatically updated). If a value outside this range is written, bit **SENS_STS.ICCER** is set.

| | | |
|---|---|---|
| CALIB_REF_H | **Address:** | $0x0D_H$ |
| Automatic baseline offset compensation reference | **Reset value:** | $0x01_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **VAL** | | | | | | | |
| rwh | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| VAL | 7:0 | rwh | **MSB of the ABOC**<br>The concatenation of this value with bitfield **CALIB_REF_L.VAL** gives the currently used reference value. |

## 5.17 Automatic baseline offset compensation reference (CALIB_REF_L)

Registers **CALIB_REF_H** and **CALIB_REF_L** define the reference value used for the ABOC and the force calibration. The concatenation of **CALIB_REF_H** (MSB) and **CALIB_REF_L** (LSB) define the reference value. The concatenated offset value is coded as a two’s complement signed short integer (1 bit = 1 ppm).

Values must be comprised between 350 ppm and 1500 ppm. Values below 350 ppm will be treated as 350 ppm (register automatically updated). Similarly, values above 1500 ppm will be treated at 1500 ppm (register automatically updated). If a value outside this range is written, bit **SENS_STS.ICCER** is set.

| | | |
|---|---|---|
| CALIB_REF_L | **Address:** | $0x0E_H$ |
| Automatic baseline offset compensation reference | **Reset value:** | $0x90_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **VAL** | | | | | | | |
| rwh | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| VAL | 7:0 | rwh | **LSB of the ABOC**<br>The concatenation of this value with bitfield **CALIB_REF_H.VAL** gives the currently used reference value. |

## 5.18 Scratch pad register (SCRATCH_PAD)

This register provides a readable and writable address space for data integrity test during runtime. This register is not associated with a specific hardware functionality.

| | | |
|---|---|---|
| SCRATCH_PAD | **Address:** | $0x0F_H$ |
| Scratch pad register | **Reset value:** | $0x00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **VAL** | | | | | | | |
| rw | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| VAL | 7:0 | rw | **Read/Write value**<br>This bit field is “don’t care” for the device. |

## 5.19 Soft reset register (SENS_RST)

This register is used to trigger a soft reset.
In case an invalid command is received, bit **SENS_STS.ICCER** is set.

| | | |
|---|---|---|
| SENS_RST | **Address:** | $0x10_H$ |
| Soft reset register | **Reset value:** | $0x00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **SRTRG** | | | | | | | |
| w | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| SRTRG | 7:0 | w | **Soft reset trigger**<br>Writing $A3_H$ to this field triggers a soft reset event.<br>Writing $BC_H$ to this field resets the ABOC context.<br>Writing $CD_H$ to this field disables the advanced VDD compensation feature.<br>Writing $CF_H$ to this field saves the force calibration offset immediately in the internal non-volatile memory.<br>Writing $DF_H$ to this field disables the Stepwise Reactive IIR Filter.<br>Writing $FC_H$ to this field resets the forced compensation correction factor.<br>Writing $FE_H$ to this field enables the Stepwise Reactive IIR Filter (by default enabled).<br>Other values are reserved. Writing a non-valid value to this field generates a communication error (bit **SENS_STS.ICCER** set).<br>This bit is read back as $00_H$. |

# 6 Assembly instruction

XENSIV™ PAS CO2 module is classified as moisture-sensitivity level 3 (MSL 3). The maximum reflow temperature during board assembly must not exceed 245°C according to IPC/JEDEC J-STD-020E. As shown in the Figure 11, pad 1 to 14 need to be soldered. Pad 1 to 10 need to be assembled as per functionality (Table 1). Pad 11 and 13 need to be connected to the GND. Pad 12 and 14 are not internally connected but must be soldered to maintain mechanical stability. Pad 12 and 14 can be left open or connected to GND. Non-marked smaller pads should be kept open.

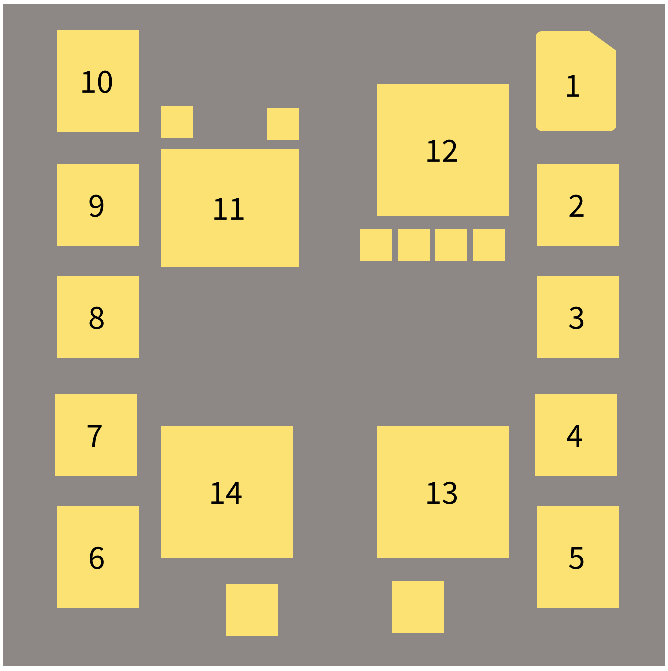


**Figure 11 XENSIV™ PASCO2V01 pads need to be connected to an application board**

***Notes:***

1. *One-time reflow is permitted and after assembly rework is not recommended*
2. *Vapor phase soldering may damage the sensor irreversibly*

For the customer, the allocated floor time (out of bag) is 168 hours (at ≤30°C and 60% r.H.) according to IPC/JEDEC J-STD-020. If floor time exceeds, then the parts (out of moisture barrier bag) need to be baked according to the following table:

**Table 14 Baking condition of the XENSIV™ PASCO2V01**

| Package condition | Bake temperature | Bake time | Condition |
|---|---|---|---|
| Sensors outside of tape | 125°C | 24 hours | r.H. < 5% |
| Sensors within the tape | 40°C | 8 days | r.H. < 5% |

# 7 Package dimensions and footprint

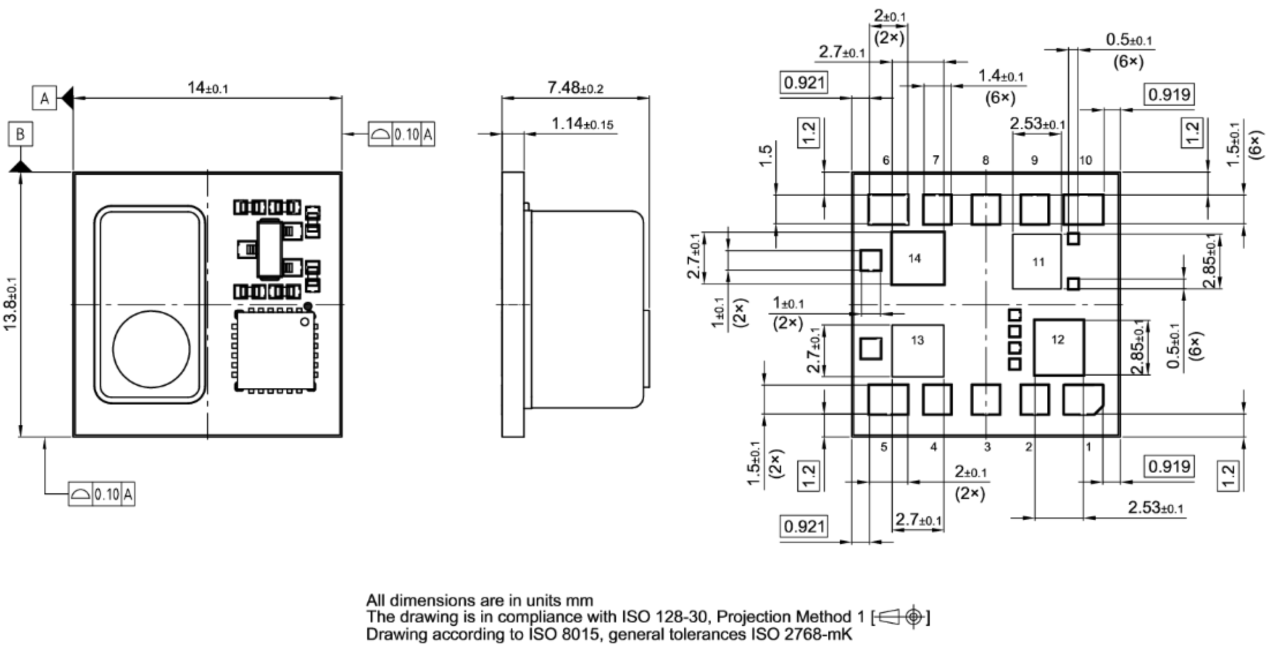


**Figure 12** **Package outline (top, side, and bottom view of LG-MLGA-14-1)**

# 8 Packing for shipment

The device will be shipped in tape and reel. Each tape and reel consist of 300 parts.

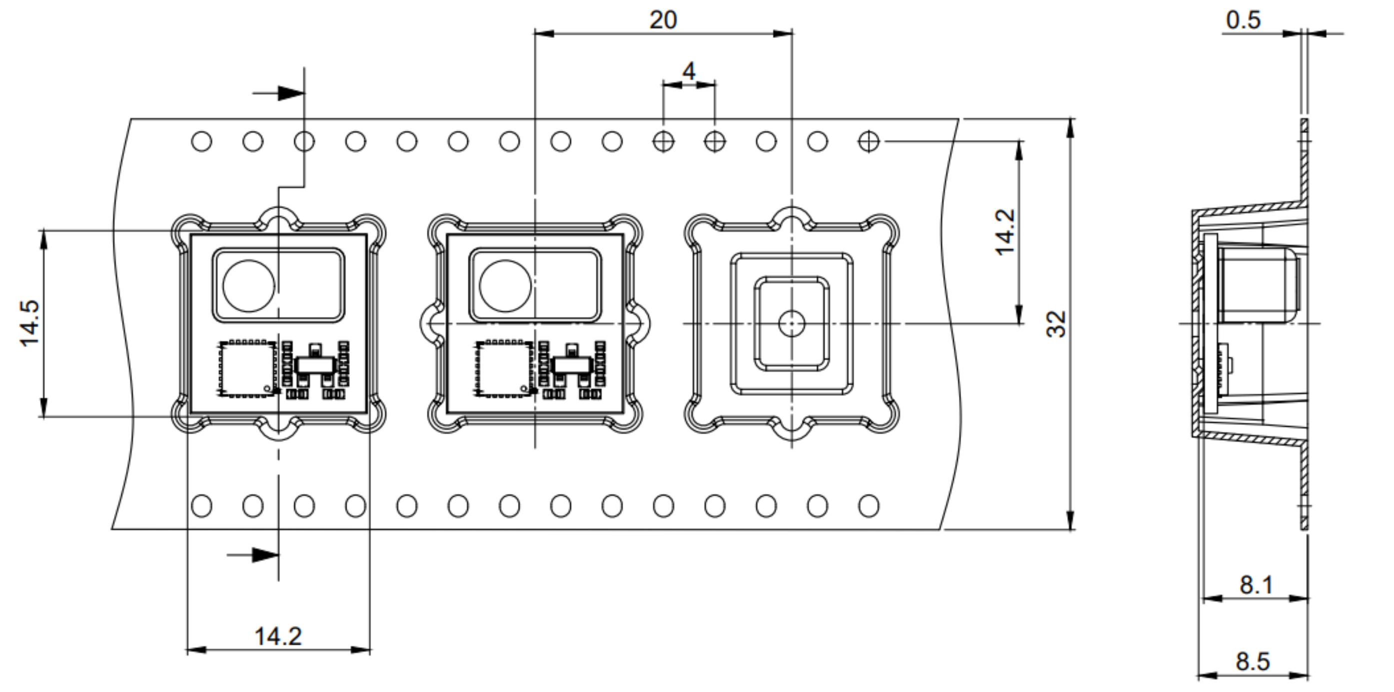


**Figure 13 Tape and reel packing of XENSIV™ PAS CO2**

## Revision history

| Document revision | Date | Description of changes |
|---|---|---|
| 1.0 | 2022-01-17 | Initial release |
| 1.1 | 2022-06-13 | Updated Storage condition, assembly instruction and minor cosmetic changes |
| 1.2 | 2022-09-21 | Storage during transportation, resolved ambiguity before paragraph 4.1.5, updated the baking time in assembly instruction and minor cosmetic changes |
| 1.3 | 2022-11-21 | Correction made in Storage condition section (non-evacuated instead of evacuated dry-pack). Note on typical sampling rate and sensor performance added.<br>Parameter resolution added |
| 1.4 | 2024-03-06 | Halogen-free and RoHS symbol and storage time added/updated |
| 1.5 | 2024-04-09 | New OPN and SP# |
| 1.6 | 2024-08-26 | Typ. Accuracy spec for high CO2 concentration introduced, features list updated, footnote on uncertainty of calibration gas mixtures added |
| 1.7 | 2024-11-27 | Added Sections 5 to 8<br>Updated datasheet template |

**Trademarks**

All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2024-11-27**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**



**Do you have a question about any aspect of this document?**

**Email: erratum@infineon.com**

**Document reference**
**IFX-cmd1726744151864**