Combinatorial PAL10H8 Series

10H8, 12H6, 14H4, 16H2
16C1
10L8, 12L6, 14L4, 16L2

Features/Benefits

- Combinatorial architectures
- Active high or active low options
- Security fuse

Ordering Information

PAL10H8 C N STD

- PROGRAMMABLE ARRAY LOGIC
- NUMBER OF ARRAY INPUTS
- OUTPUT TYPE
  - H = Active High Combinatorial
  - L = Active Low Combinatorial
  - C = Complementary Combinatorial
- NUMBER OF OUTPUTS
- OPERATING CONDITIONS
  - C = Commercial
- PACKAGE
  - N = Plastic DIP
  - J = Ceramic DIP
  - NL = Plastic Leaded Chip Carrier
  - SG = Small-Outline Gull-wing
- PROCESSING
  - STD = Standard
  - XXXX = Other

	INPUTS	OUTPUTS	POLARITY	t_{PD} (ns)	I_{CC} (mA)
PAL10H8	10	8	HIGH	35	90
PAL12H6	12	6	HIGH	35	90
PAL14H4	14	4	HIGH	35	90
PAL16H2	16	2	HIGH	35	90
PAL16C1	16	2	BOTH	40	90
PAL10L8	10	8	LOW	35	90
PAL12L6	12	6	LOW	35	90
PAL14L4	14	4	LOW	35	90
PAL16L2	16	2	LOW	35	90

Description

The PAL10H8 Series is made up of nine combinatorial 20-pin PAL devices. They implement simple combinatorial logic, with no feedback. Each has sixteen product terms total, divided among the outputs, with two to sixteen product terms per output.

Polarity

Both active high and active low versions are available for each architecture. The 16C1 offers both polarities of its single output.

Performance

The standard series has a propagation delay (tpd) of 35 nanoseconds (ns), except for the 16C1 at 40 ns. Standard supply current is 90 milliamps (mA).

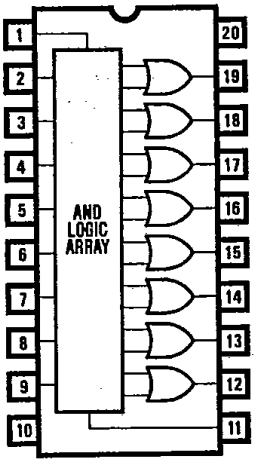
Packages

The commercial PAL10H8 Series is available in the plastic DIP (N), ceramic DIP (J), plastic leaded chip carrier (NL), and small outline (SG) packages.

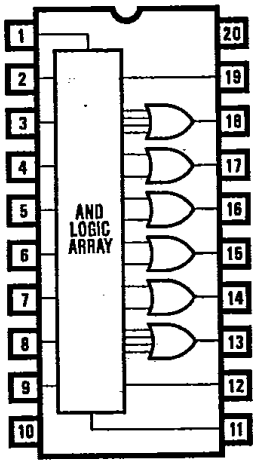
10285A
JANUARY 1988

DIP/SO Pinouts

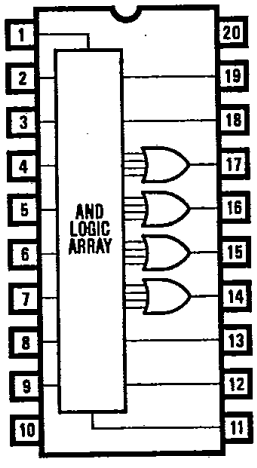
10H8



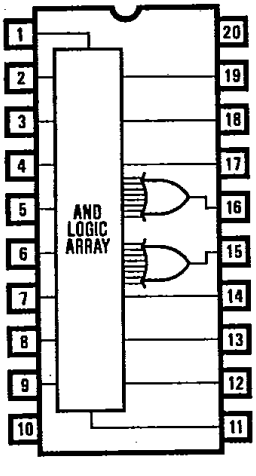
12H6



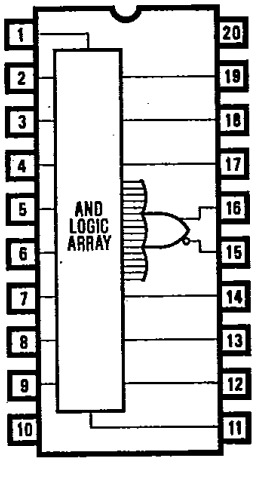
14H4



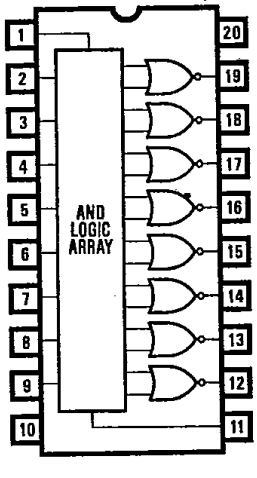
16H2



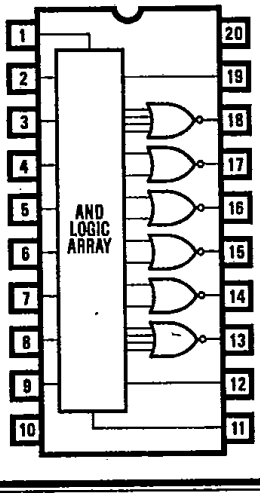
16C1



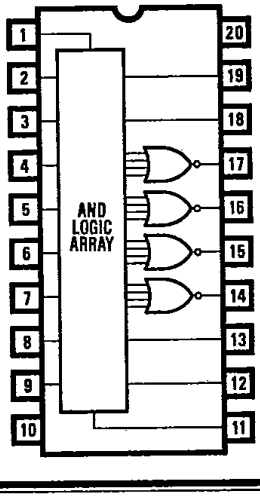
10L8



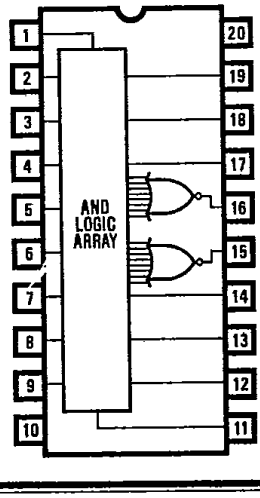
12L6



14L4



16L2



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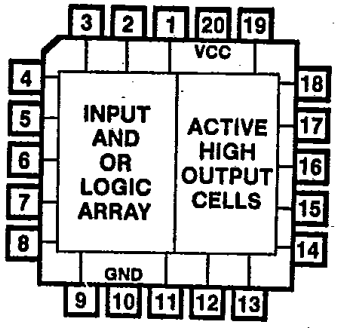
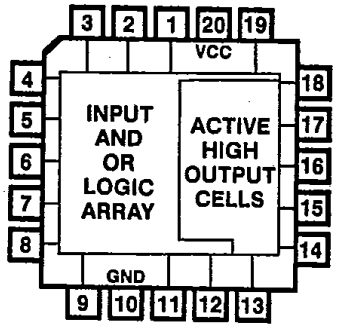
PLCC Pinouts

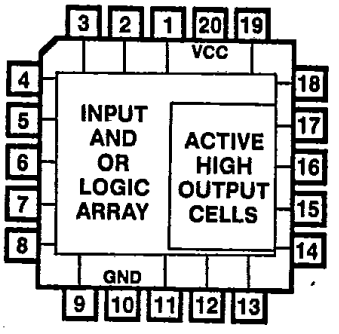
10H8



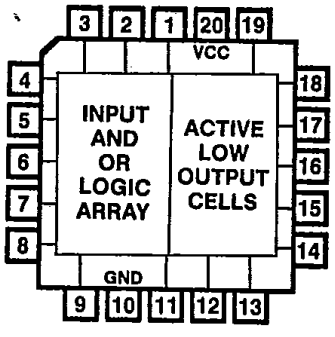
12H6



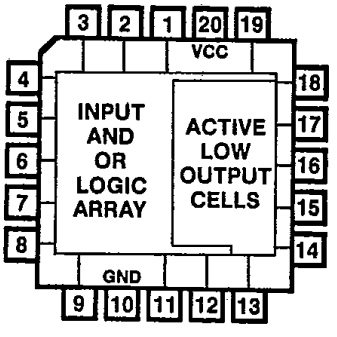
14H4



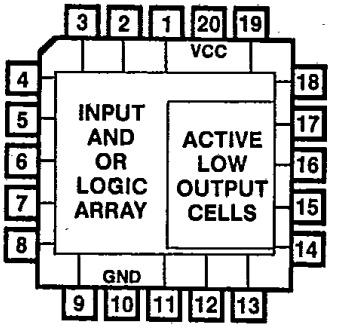
10L8



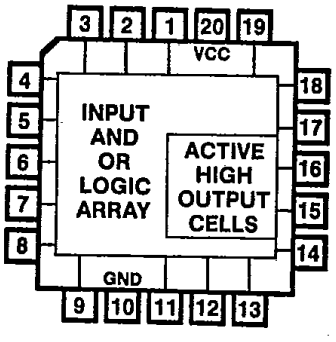
12L6



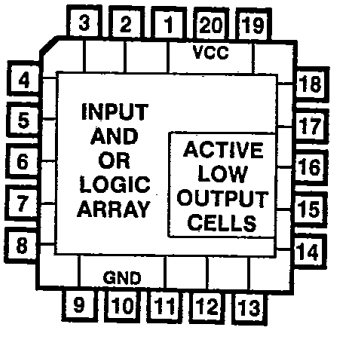
14L4



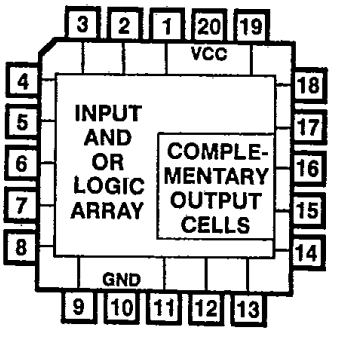
16H2



16L2



16C1



Package Drawings

(refer to PAL Device Package Outlines, page 3-179)

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7.0 V	−0.5 V to 12.0 V
Input voltage	−1.5 V to 5.5 V	−1.0 V to 22.0 V
Off-state output voltage	5.5 V	12.0 V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
T_A	Operating free-air temperature	0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage					0.8	V
V_{IH}[1]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2 mA	2.4	2.8		V
I_{OS}[2]	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			55	90	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output	Except 16C1	R_1 = 560 Ω, R_2 = 1.1 kΩ		25	35	ns
		16C1			25	40	

1. These are absolute values with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

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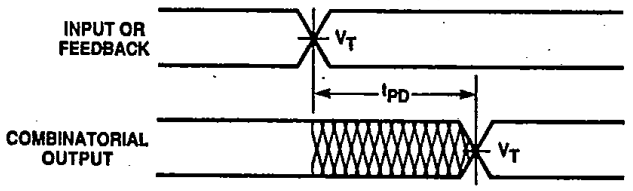
Switching Waveforms



Combinatorial Output

Notes:
1. VT = 1.5 V.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2-5 ns typical.

Switching Test Load

(refer to page 5-164)

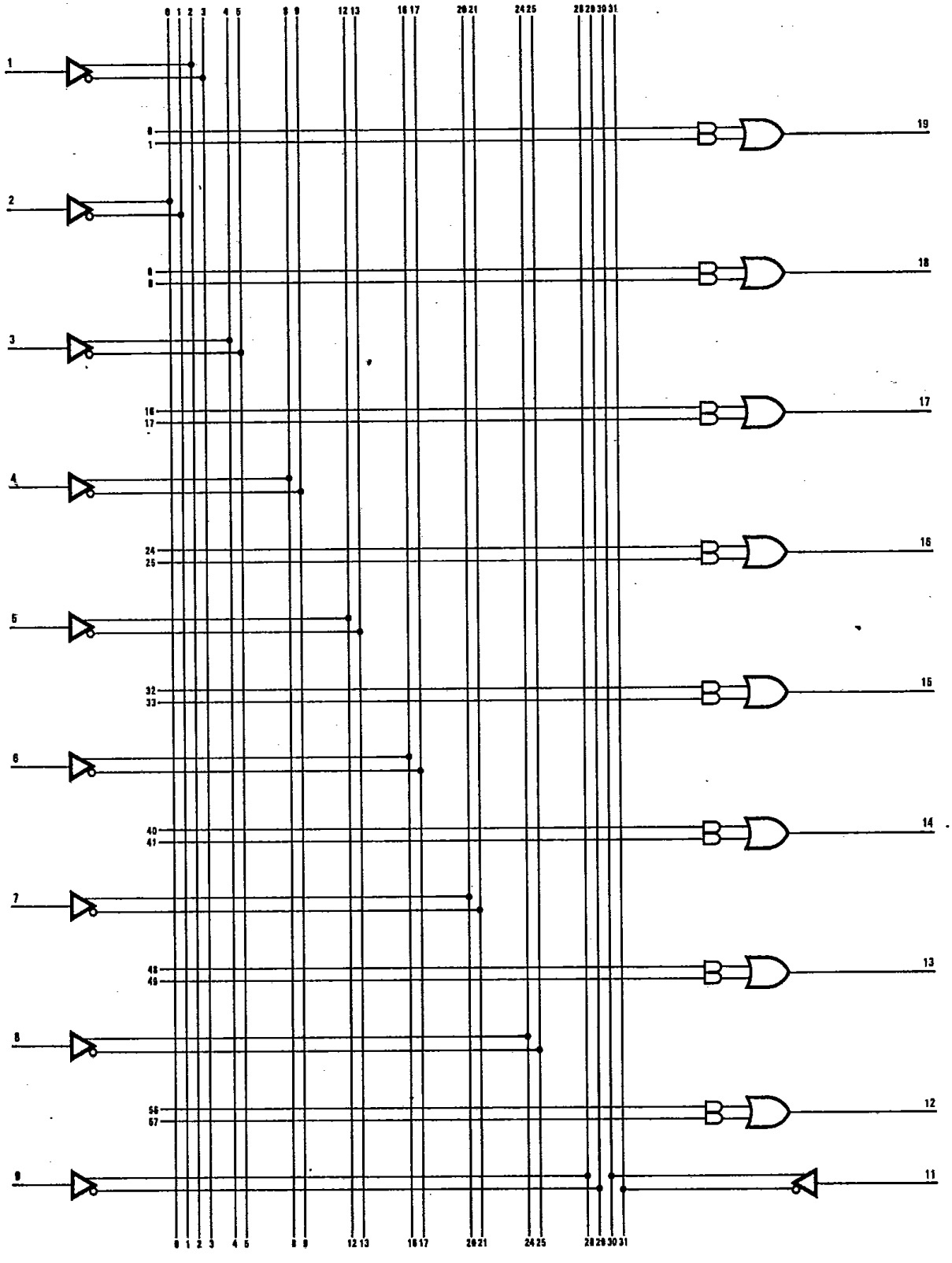
Programmers/Development Systems

(refer to Programmer Reference Guide, page 3-81)

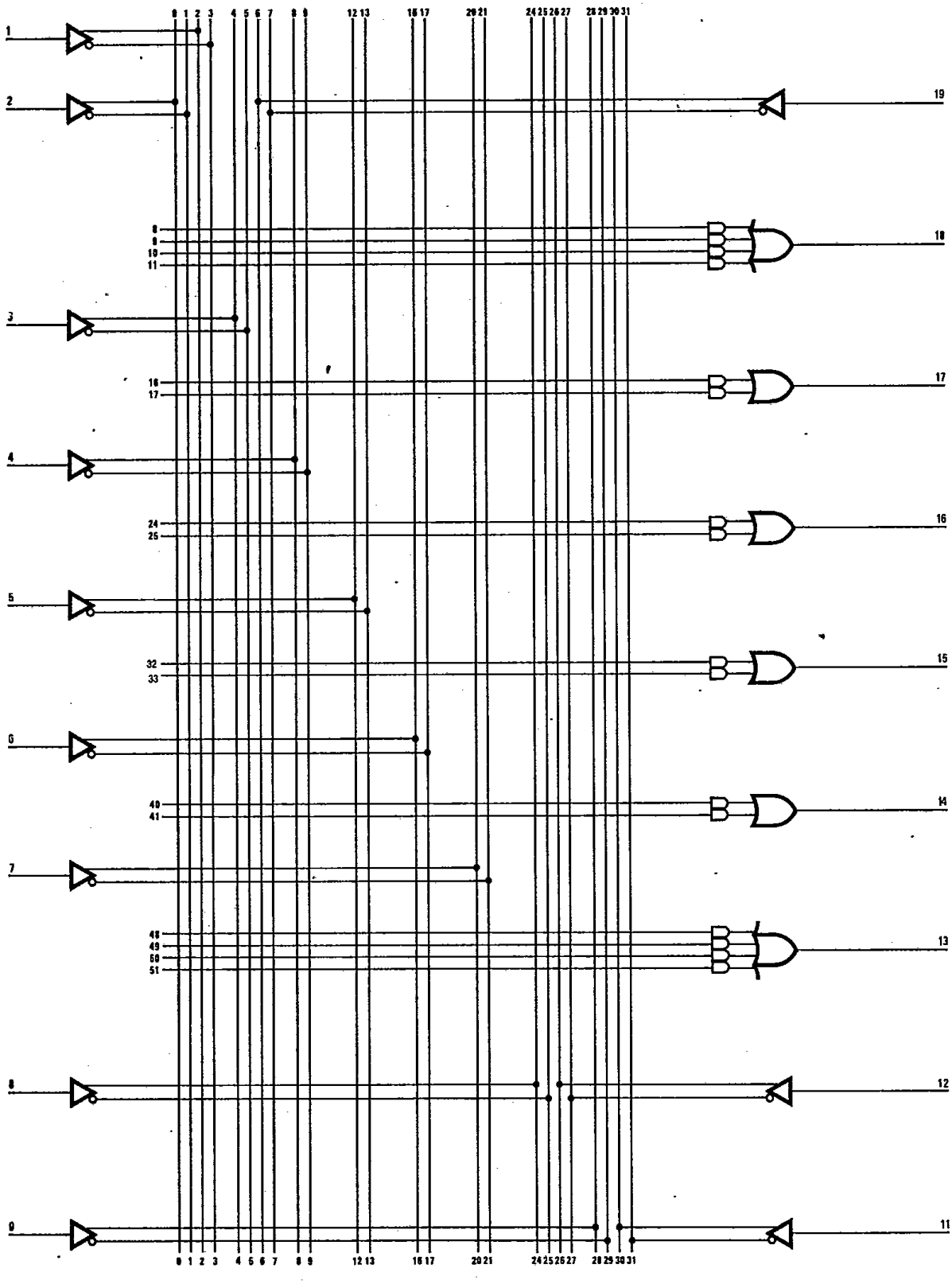
Schematic of Inputs and Outputs

(refer to page 5-164)

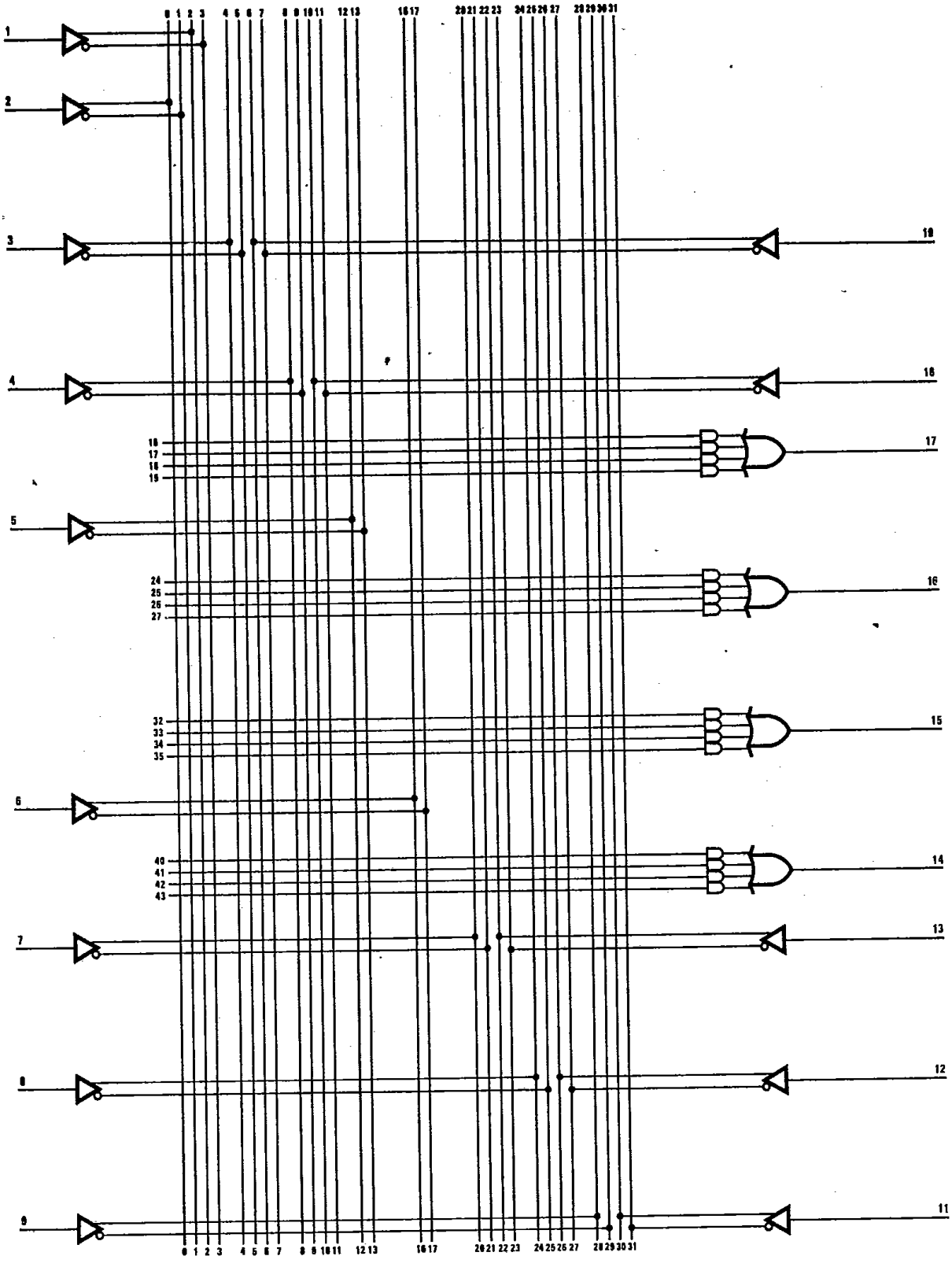
Logic Diagram **10H8** T-46-13-47



Logic Diagram **12H6**



Logic Diagram **14H4** T-46-13-47



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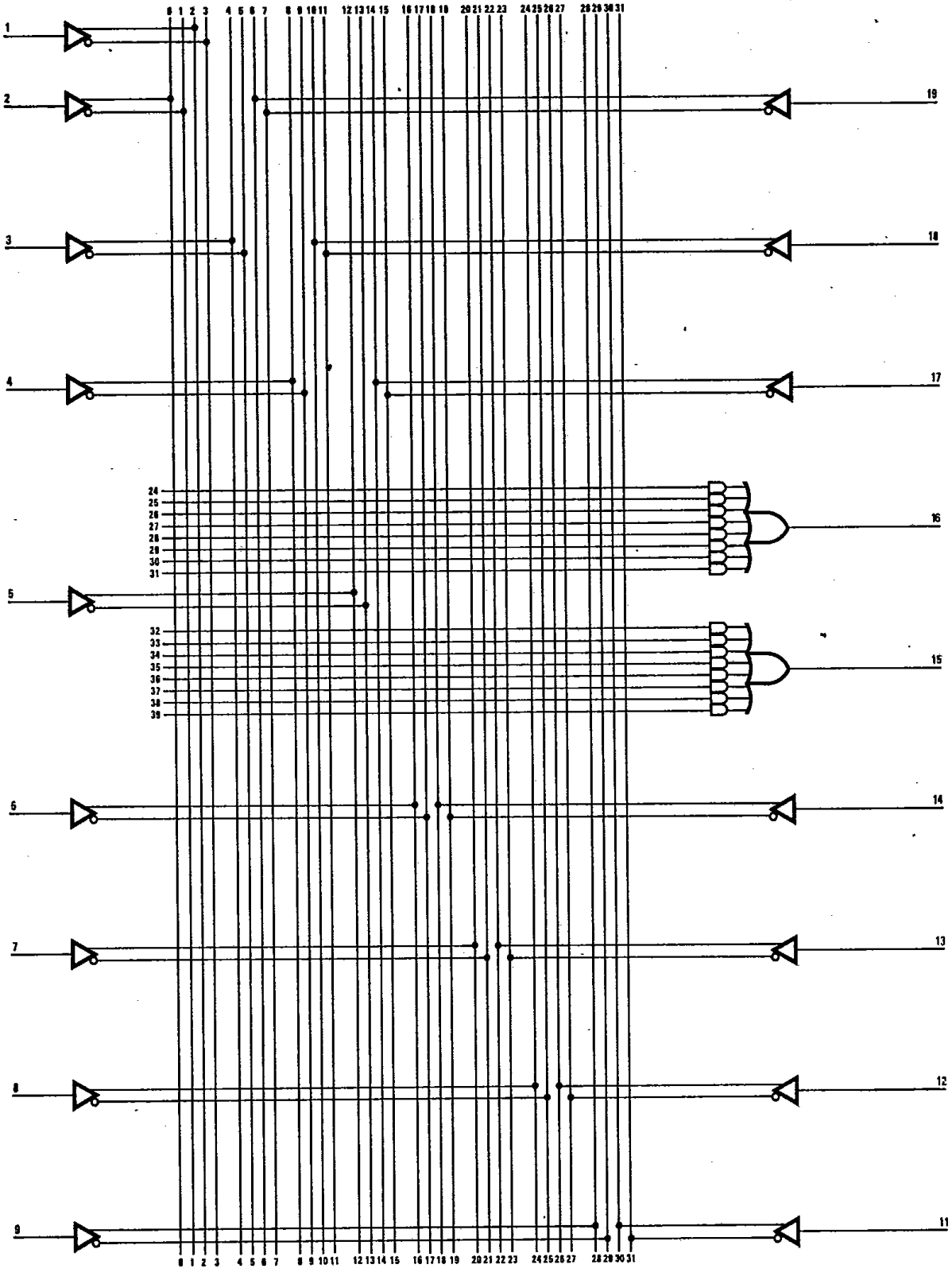
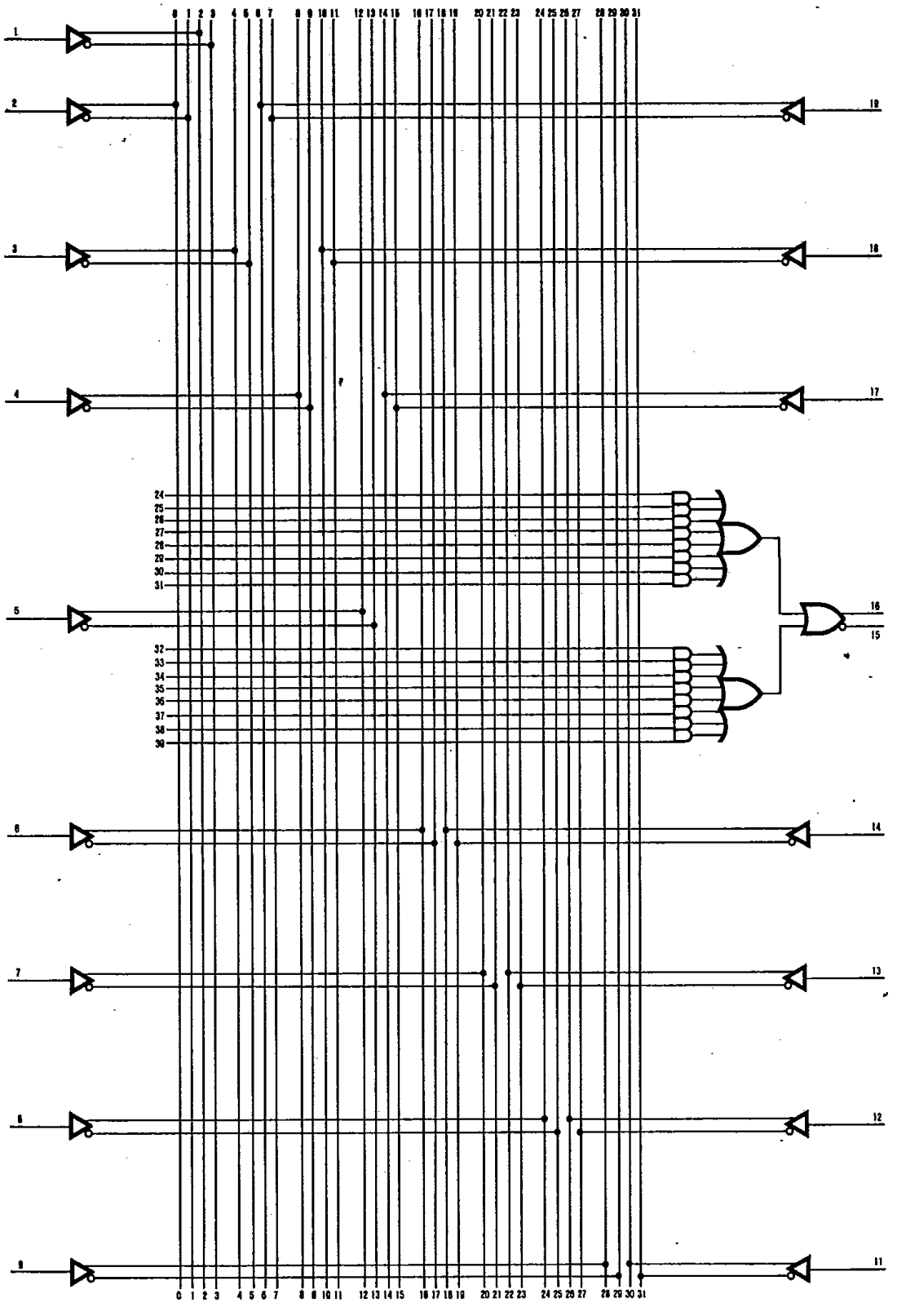
Logic Diagram **16H2**

T-46-13-47



Logic Diagram

16C1



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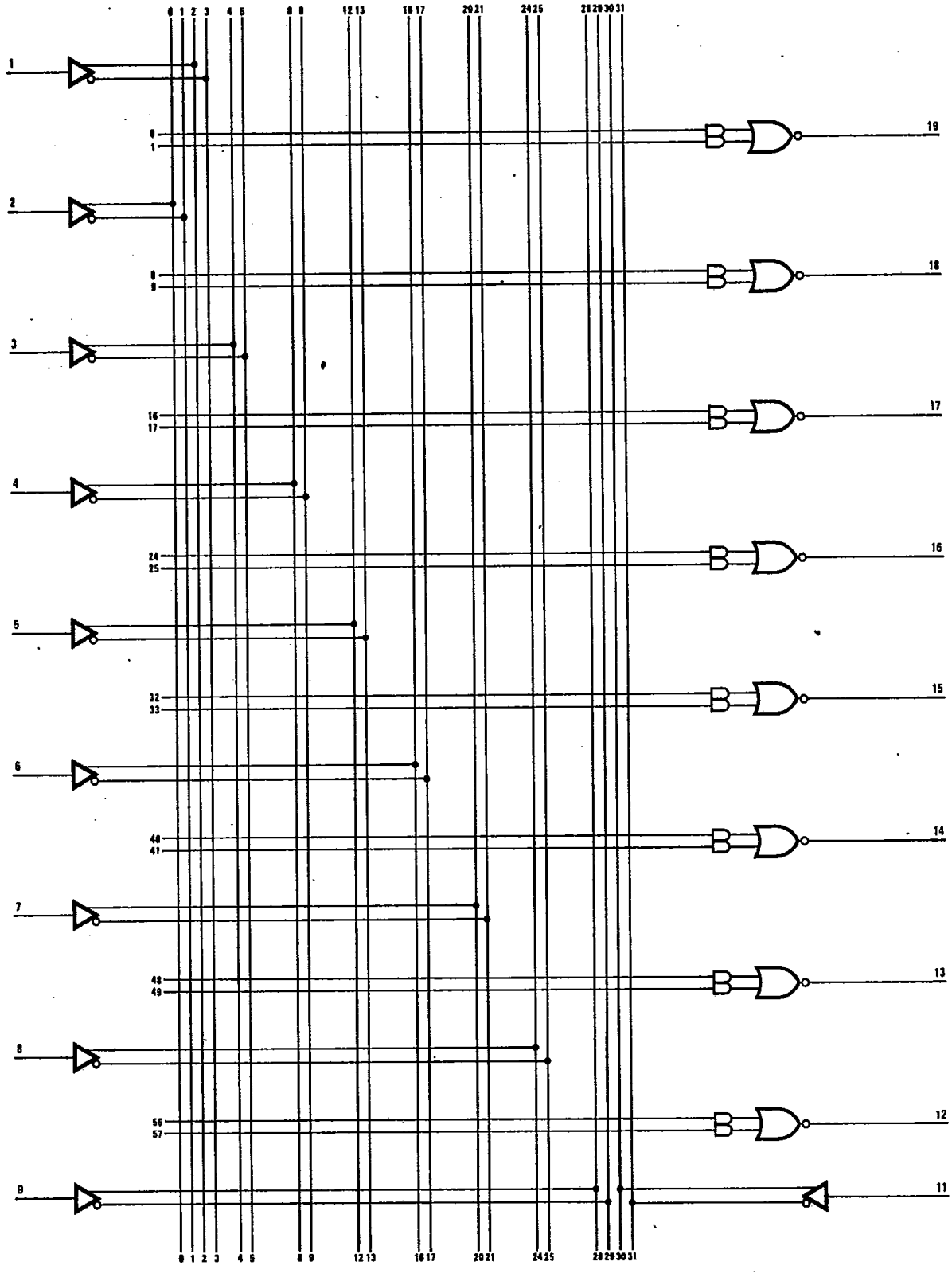
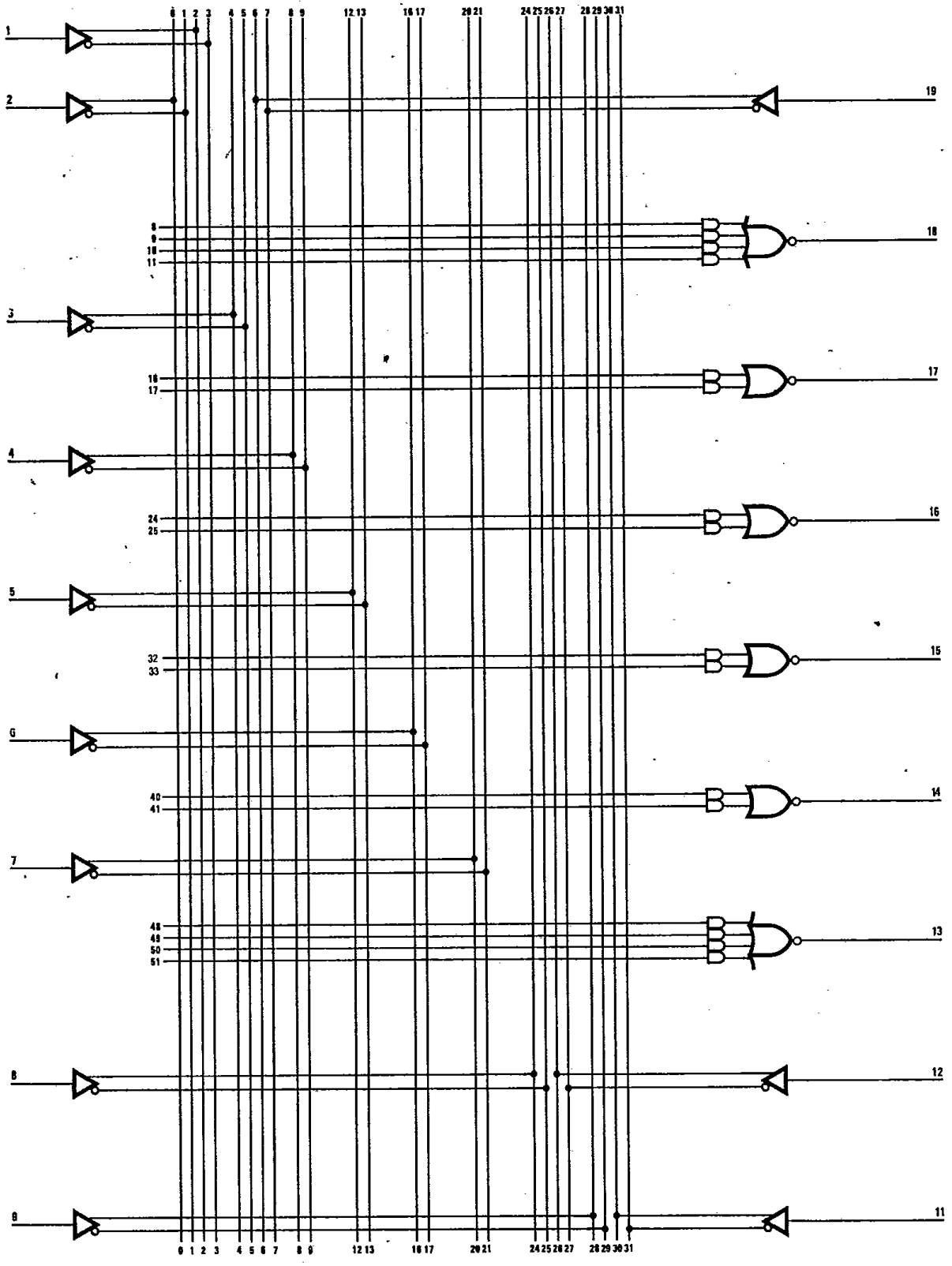
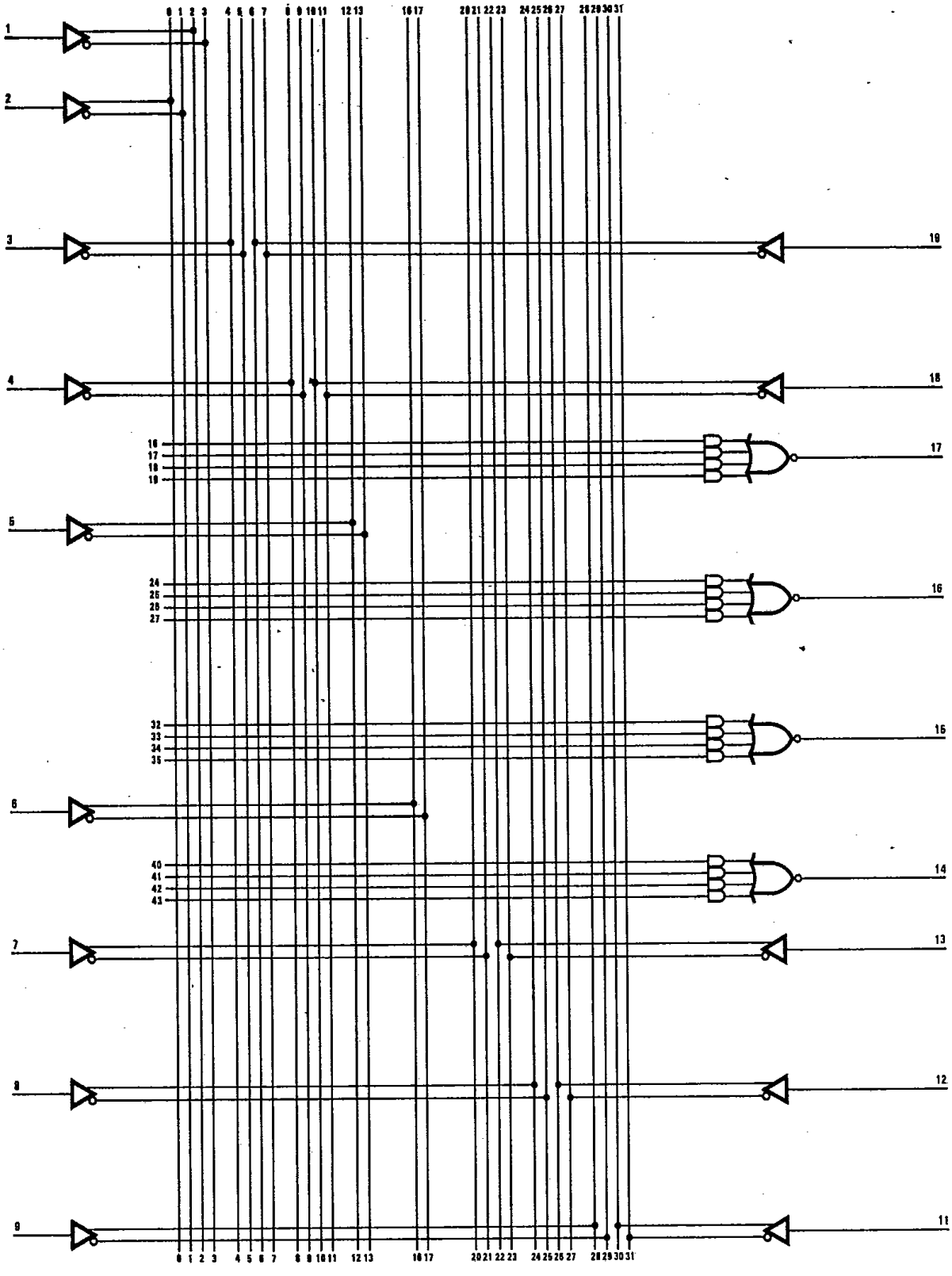
Logic Diagram **10L8** T-46-13-47



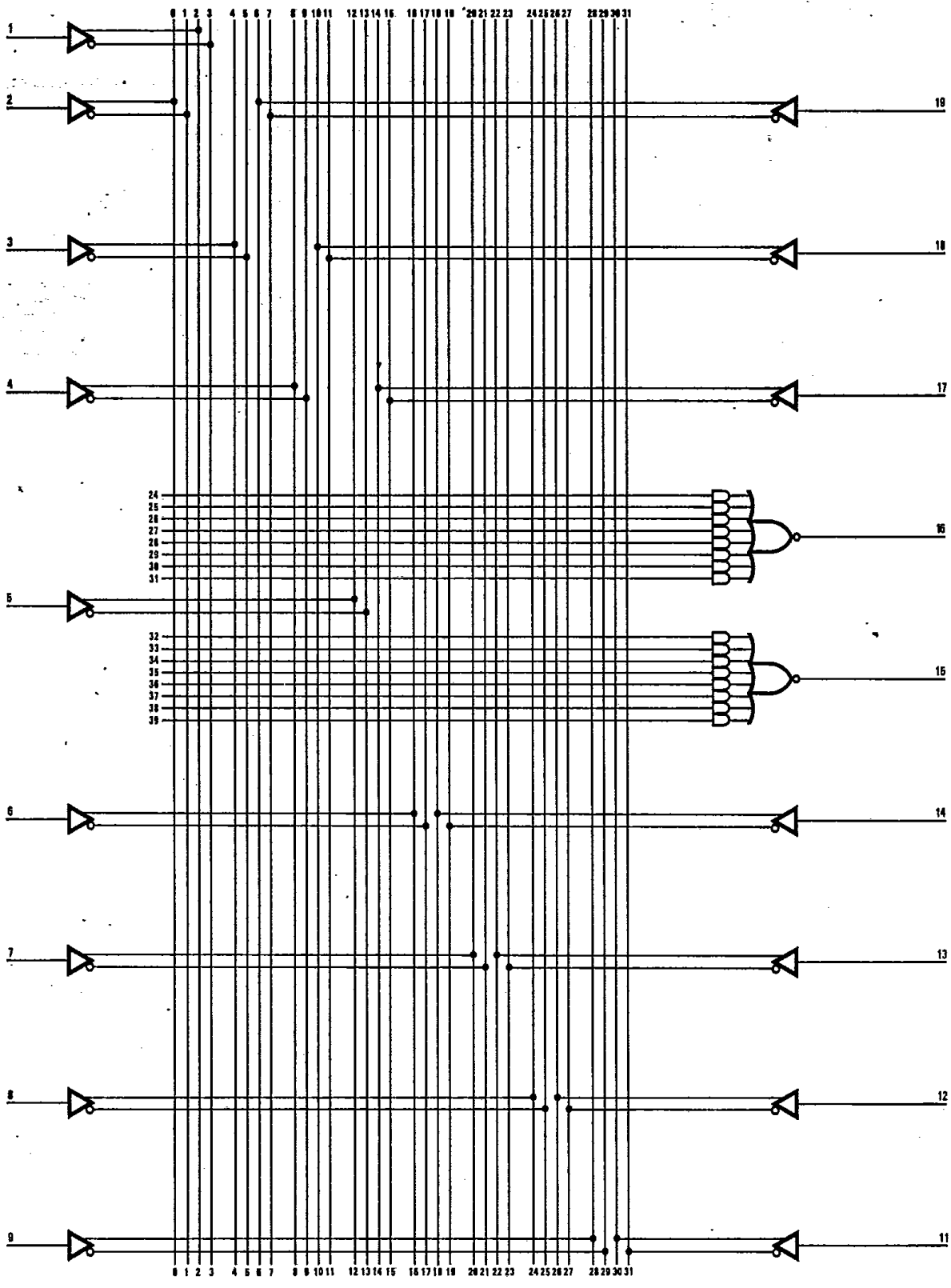
Logic Diagram **12L6** T-46-13-47



Logic Diagram **14L4** T-46-13-47



Logic Diagram **16L2** T-46-13-47



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