

# PA7140 PEEL™ Array

## Programmable Electrically Erasable Logic Array

### Features

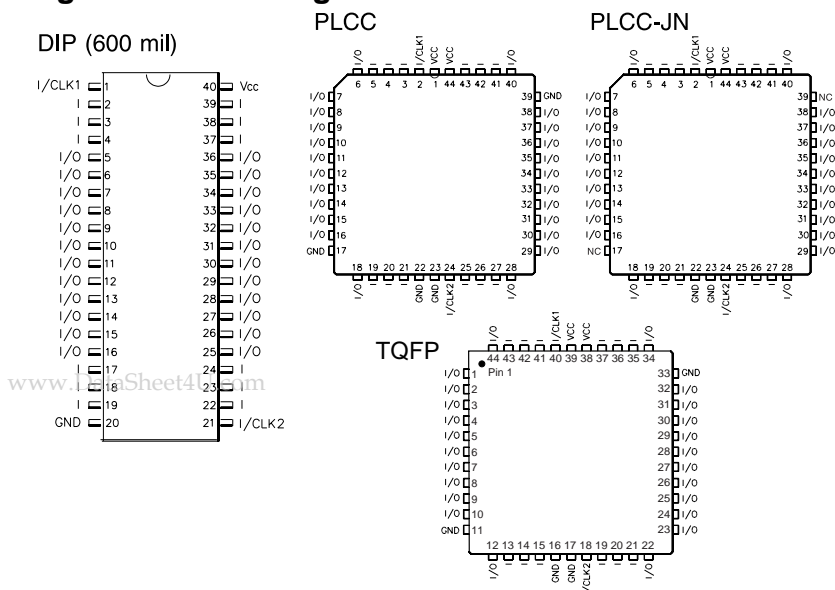
- **Versatile Logic Array Architecture**
  - 24 I/Os, 14 inputs, 60 registers/latches
  - Up to 72 logic cell output functions
  - PLA structure with true product-term sharing
  - Logic functions and registers can be I/O-buried
- **High-Speed Commercial and Industrial Versions**
  - As fast as 13ns/20ns (tpdi/tpdx), 66.6MHz (fMAX)
  - Industrial grade available for 4.5 to 5.5V Vcc and -40 to +85 °C temperatures Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications
  - Integration of multiple PLDs and random logic
  - Buried counters, complex state-machines
  - Comparators, decoders, other wide-gate functions
- **CMOS Electrically Erasable Technology**
  - Reprogrammable in 40-pin DIP, 44-pin PLCC, and TQFP packages
- **Flexible Logic Cell**
  - Up to 3 output functions per logic cell
  - D,T and JK registers with special features
  - Independent or global clocks, resets, presets, clock polarity and output enables
  - Sum-of-products logic for output enables
- **Development and Programmer Support**
  - ICT PLACE Development Software
  - Fitters for ABEL, CUPL and other software
  - Programming support for by ICT PDS-3 and popular third-party programmers

### General Description

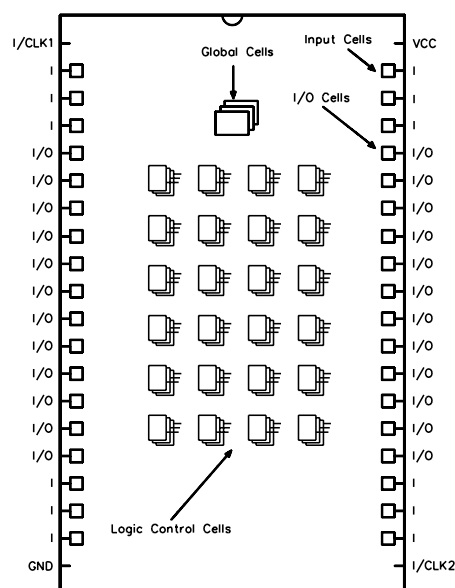
The PA7140 is a member of the Programmable Electrically Erasable Logic (PEEL™) Array family based on ICT's CMOS EEPROM technology. PEEL™ Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and speed needed for today's programmable logic designs. The PA7140 offers a versatile logic array architecture with 24 I/O pins, 14 input pins and 60 registers/latches (24 buried logic cells, 12 input registers/latches, 24 buried I/O registers/latches). Its logic array implements 100 sum-of-products logic functions divided into two groups each serving 12 logic cells. Each group shares half (60) of the 120 product-terms available for logic cells.

The PA7140's logic and I/O cells (LCCs, IOCs) are extremely flexible with up to three output functions per cell (a total of 72 for all 24 logic cells). Cells are configurable as D, T, and JK registers with independent or global clocks, resets, presets, clock polarity, and other features, making the PA7140 suitable for a variety of combinatorial, synchronous and asynchronous logic applications. The PA7140 supports speeds as fast as 13ns/20ns (tpdi/tpdx) and 66.6MHz (fMAX) at moderate power consumption 140mA (100mA typical). Packaging includes 40-pin DIP and 44-pin PLCC (see Figure 1). Development and programming support for the PA7140 is provided by ICT and popular third-party development tool manufacturers.

**Figure 1: Pin Configuration**



**Figure 2: Block Diagram**



This device has been designed and tested for the recommended operating conditions. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

**Table 1. Absolute Maximum Ratings**

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
VI, VO	Voltage Applied to Any Pin	Relative to Ground <sup>1</sup>	-0.5 to VCC + 0.6	V
IO	Output Current	Per pin (IOL, IOH)	±25	mA
TST	Storage Temperature		-65 to + 150	°C
TLT	Lead Temperature	Soldering 10 seconds	+300	°C

**Table 2. Operating Ranges**

Symbol	Parameter	Conditions	Min	Max	Unit
VCC	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	
TA	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
TR	Clock Rise Time	See Note 2		20	ns
TF	Clock Fall Time	See Note 2		20	ns
TRVCC	VCC Rise Time	See Note 2		250	ms

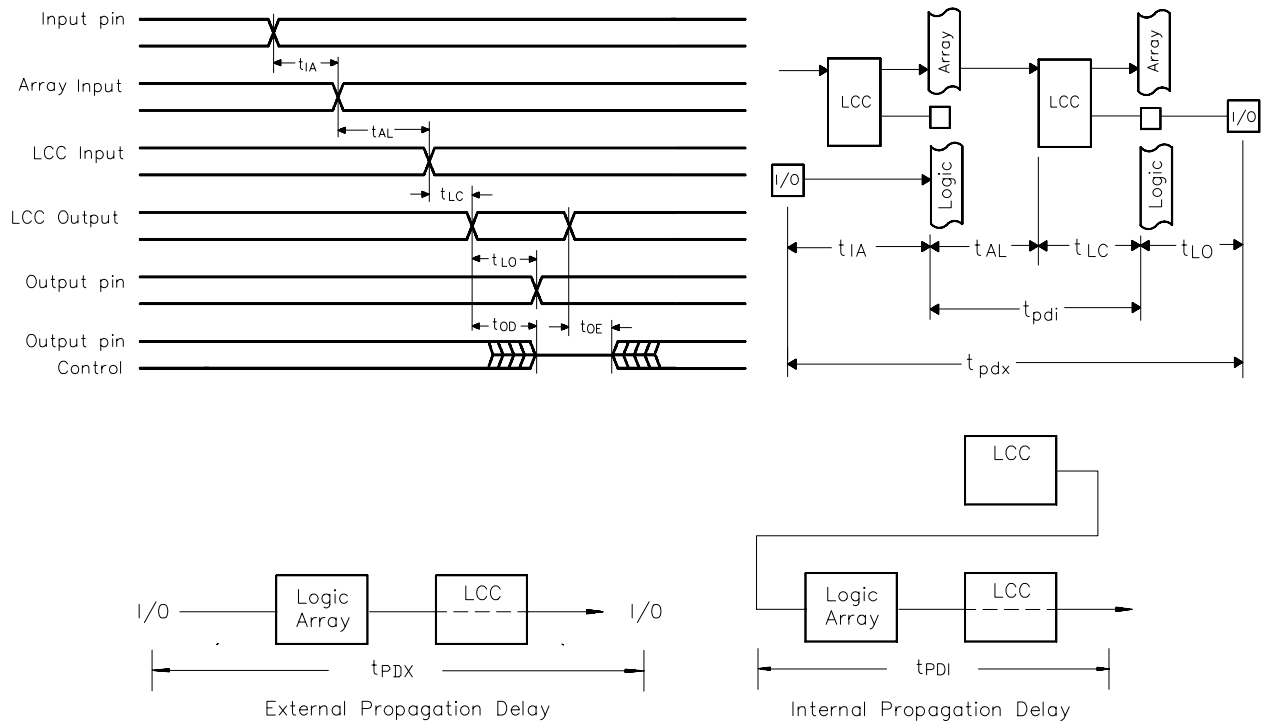
**Table 3. D.C. Electrical Characteristics over the recommended operating conditions**

Symbol	Parameter	Conditions		Min	Max	Unit
VOH	Output HIGH Voltage - TTL	VCC = Min, IOH = -4.0mA		2.4		V
VOHC	Output HIGH Voltage - CMOS	VCC = Min, IOH = -10µA		VCC - 0.3		V
VOL	Output LOW Voltage - TTL	VCC = Min, IOL = 16mA			0.5	V
VOLC	Output LOW Voltage - CMOS	VCC = Min, IOL = -10µA			0.15	V
VIH	Input HIGH Level			2.0	VCC + 0.3	V
VIL	Input LOW Level			-0.3	0.8	V
IIL	Input Leakage Current	VCC = Max, GND ≤ VIN ≤ VCC			±10	µA
IOZ	Output Leakage Current	I/O = High-Z, GND ≤ VO ≤ VCC			±10	µA
ISC	Output Short Circuit Current <sup>4</sup>	VCC = 5V, VO = 0.5V, TA = 25°C		-30	-120	mA
ICC <sup>11</sup>	VCC Current	VIN = 0V or VCC <sup>3,11</sup> f = 25MHz All outputs disabled <sup>4</sup>	-20	100 (typ.) <sup>18</sup>	140	mA
			-25		140	
			I-25		150	
CIN <sup>7</sup>	Input Capacitance <sup>5</sup>	TA = 25°C, VCC = 5.0V @ f = 1 MHz			6	pF
COUT <sup>7</sup>	Output Capacitance <sup>5</sup>				12	pF

**Table 5. A.C Electrical Characteristics Combinatorial** Over the Operating Range

Symbol	Parameter <sup>6,12</sup>	-20		-25 / 1 -25		Unit
		Min	Max	Min	Max	
tPDI	Propagation delay Internal (tAL + tLC)		13		17	ns
tPDX	Propagation delay External (tIA + tAL + tLC + tLO)		20		25	ns
tIA	Input or I/O pin to array input		2		2	ns
tAL	Array input to LCC		12		16	ns
tLC	LCC input to LCC output <sup>10</sup>		1		1	ns
tLO	LCC output to output pin		5		6	ns
tOD, tOE	Output Disable, Enable from LCC output <sup>7</sup>		5		6	ns
tOX	Output Disable, Enable from input pin <sup>7</sup>		20		25	ns

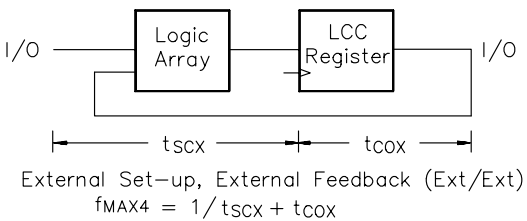
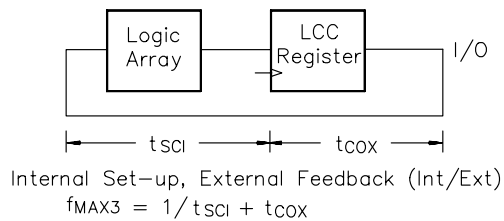
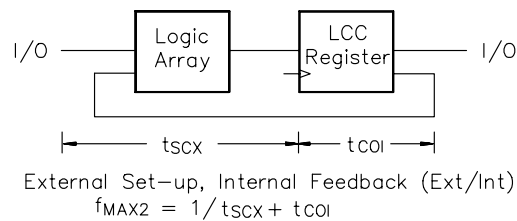
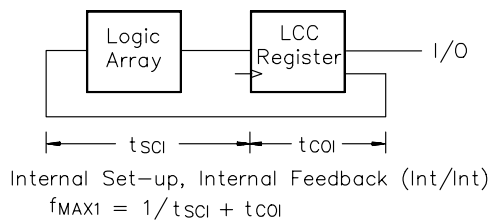
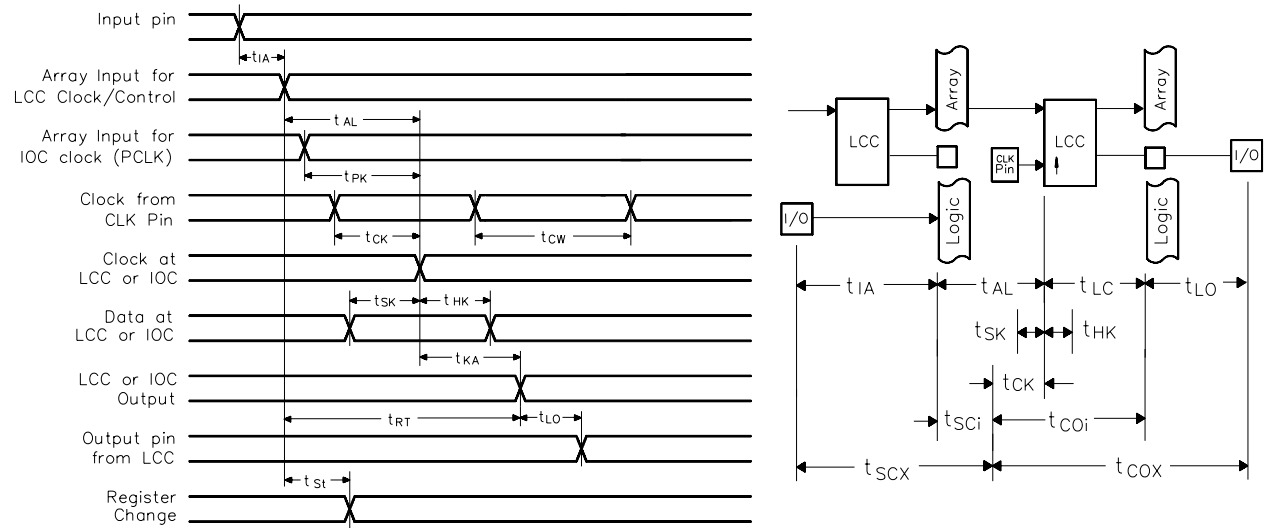
### Combinatorial Timing - Waveforms and Block Diagram



**Table 1. A.C. Electrical Characteristics Sequential** Over the Operating Range

Symbol	Parameter <sup>6,12</sup>	-20		-25 / I-25		Unit
		Min	Max	Min	Max	
tSCI	Internal set-up to system clock <sup>8</sup> - LCC <sup>14</sup> (tAL + tSK + tLC - tCK)	8		11		ns
tSCX	Input <sup>16</sup> (EXT.) set-up to system clock, - LCC (tIA + tSCI)	10		14		ns
tCOI	System-clock to Array Int. - LCC/IOC/INC <sup>14</sup> (tCK + tLC)		7		8	ns
tCOX	System-clock to Output Ext. - LCC (tCOI + tLO)		12		14	ns
tHX	Input hold time from system clock - LCC	0		0		ns
tSK	LCC Input set-up to async. clock <sup>13</sup> - LCC	1		1		ns
tAK	Clock at LCC or IOC - LCC output	1		1		ns
tHK	LCC input hold time from system clock - LCC	4		4		ns
tSI	Input set-up to system clock - IOC/INC <sup>14</sup> (tSK - tCK)	0		0		ns
tHI	Input hold time from system clock - IOC/INC <sup>14</sup> (tSK - tCK)	5		6		ns
tPK	Array input to IOC PCLK clock		9		11	ns
tSPI	Input set-up to PCLK clock <sup>17</sup> - IOC/INC (tSK-tPK-tIA)	0		0		ns
tHPI	Input hold from PCLK clock <sup>17</sup> - IOC/INC (tPK+tIA-tSK)	10		12		ns
tSD	Input set-up to system clock - IOC/INC Sum-D <sup>15</sup> (tIA + tAL + tLC + tSK - tCK)	10		13		ns
tHD	Input hold time from system clock - IOC Sum-D	0		0		ns
tSDP	Input set-up to PCLK clock (tIA + tAL + tLC + tSK - tPK) - IOC Sum-D	7		9		ns
tHDP	Input hold time from PCLK clock - IOC Sum-D	0		0		ns
tCK	System-clock delay to LCC/IOC/INC		6		7	ns
tCW	System-clock low or high pulse width	7		8		ns
fMAX1	Max. system-clock frequency Int/Int 1/(tSCI + tCOI)		66.6		52.6	MHz
fMAX2	Max. system-clock frequency Ext/Int 1/(tSCX + tCOI)		58.8		45.4	MHz
fMAX3	Max. system-clock frequency Int/Ext 1/(tSCI + tCOX)		50.0		40.0	MHz
fMAX4	Max. system-clock frequency Ext/Ext 1/(tSCX + tCOX)		45.4		35.7	MHz
fTGL	Max. system-clock toggle frequency 1/(tCW + tCW)		71.4		62.5	MHz
tPR	LCC presents/reset to LCC output		1		2	ns
tST	Input to Global Cell present/reset (tIA + tAL + tPR)		15		20	ns
tAW	Asynch. preset/reset pulse width	8		8		ns
tRT	Input to LCC Reg-Type (RT)		8		10	ns
tRTV	LCC Reg-Type to LCC output register change		1		2	ns
tRTC	Input to Global Cell register-type change (tRT + tRTV)		9		12	ns
tRW	Asynch. Reg-Type pulse width	10		10		ns
tRESET	Power-on reset time for registers in clear state <sup>2</sup>		5		5	µs

## Sequential Timing - Waveforms and Block Diagram



## Notes

- Minimum DC input is -0.5V, however inputs may under-shoot to -2.0V for periods less than 20ns.
- Test points for Clock and VCC in  $t_R$ ,  $t_{FCL}$ ,  $t_{CH}$ , and  $t_{RESET}$  are referenced at 10% and 90% levels.
- I/O pins are 0V or VCC.
- Test one output at a time for a duration of less than 1 sec.
- Capacitances are tested on a sample basis.
- Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
- $t_{OE}$  is measured from input transition to  $V_{REF} \pm 0.1V$  (See test loads at end of Section 6 for  $V_{REF}$  value).  $t_{OD}$  is measured from input transition to  $V_{OH} - 0.1V$  or  $V_{OL} + 0.1V$ .
- DIP: "System-clock" refers to pin 1/21 high speed clocks. PLCC: "System-clock" refers to pin 2/24 high speed clocks.
- For T or JK registers in toggle (divide by 2) operation only.
- For combinatorial and async-clock to LCC output delay.
- ICC for a typical application: This parameter is tested with the device programmed as a 10-bit D-type counter.
- Test loads are specified in Section 5 of this Data Book.

- "Async. clock" refers to the clock from the Sum term (OR gate).
- The "LCC" term indicates that the timing parameter is applied to the LCC register. The "IOC" term indicates that the timing parameter is applied to the IOC register. The "LCC/IOC" term indicates that the timing parameter is applied to both the LCC and IOC registers. The "LCC/IOC/INC" term indicates that the timing parameter is applied to the LCC, IOC and INC registers.
- This refers to the Sum-D gate routed to the IOC register for an additional buried register
- The term "Input" without any reference to another term refers to an (external) input pin.
- The parameter  $t_{SPI}$  indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of  $(t_{SK} - t_{PK} - t_{IA})$ . This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for  $t_{HPI}$  time, i.e. to wait for the PCLK signal to arrive at the IOC register.
- Typical (typ) ICC is measured at  $T_A = 25^\circ C$ , Freq = 25MHz,  $V_{CC} = 5V$ .

**Table 5. Ordering Information**

Part Number	Speed	Temperature	Package
PA7140P-20	13/20ns	C	P40
PA7140F-20			F44
PA7140J-20			J44
PA7140JN-20			JN44
PA7140P-25	17/25ns	C	P40
PA7140PI-25		I	P40
PA7140F-25	17/25ns	C	F44
PA7140FI-25		I	F44
PA7140J-25	17/25ns	C	J44
PA7140JI-25		I	J44
PA7140JN-25	17/25ns	C	JN44
PA7140JNI-25		I	JN44

**Part Number**
**Device**
**Suffix**
**PA7140J-20**
**Package**

P = Plastic 600mil DIP  
 F= Thin Quad Flat Pack (TQFP)  
 J = Plastic (J) Leaded Chip Carrier  
 JN = Alternate pin-out PLCC

**Speed**

-20 = 13ns/20ns tpd/tpdx  
 -25 = 17ns/25ns tpd/tpdx

**Temperature Range**

(Blank) = Commercial 0 to 70°C  
 I = Industrial -40 to +85°C