



## PA3428

CMOS IC

### 2W STEREO AUDIO AMPLIFIER

#### DESCRIPTION

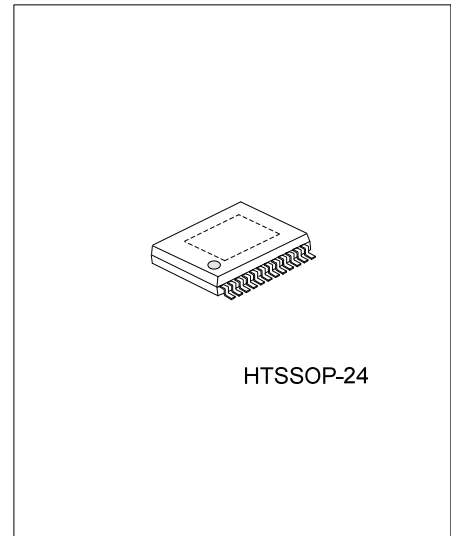
As a stereo audio speaker which is operating on a single 5V supply, the UTC **PA3428** is capable of delivering 2W of output power per channel into 4Ω loads with less than 1% THD+N.

Way of two terminals (GAIN0 and GAIN1) can configured and control the amplifier gain. It also provide gain settings of 2, 6, 12, and 24V/V.

Other features include internal gain control which requires few external components, an active-low shutdown mode input and thermal shutdown protection.

#### FEATURES

- \* Internal Depop circuitry
- \* Output power at 1% THD+N
  - Supply voltage:5V
  - Delivering 2.0W into a 4Ω load
  - Delivering 1.2W into a 8Ω load
- \* Tow mode:
  - Bridge-tied Load (BTL),
  - Single-ended (SE)
- \* Stereo input signal
- \* Fully differential input
- \* Gain control Internally
- \* Differential Input fully



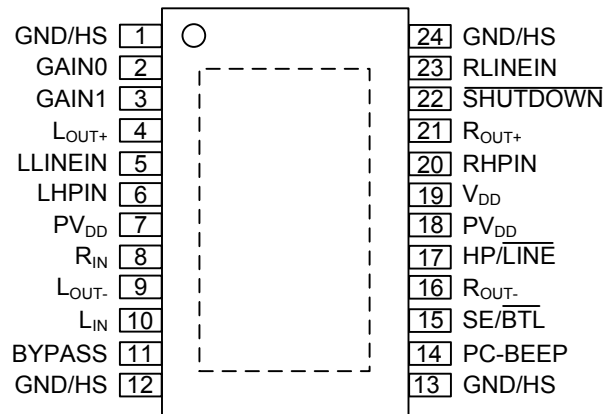
Lead-free: PA3428L  
Halogen-free: PA3428G

#### ORDERING INFORMATION

Ordering Number			Package	Packing
Normal	Lead Free	Halogen Free		
PA3428-N24-R	PA3428L-N24-R	PA3428G-N24-R	TSSOP-24	Tape Reel
PA3428-N24-T	PA3428L-N24-T	PA3428G-N24-T	TSSOP-24	Tube

<p>PA3428L-N24-R</p>	<p>(1) Packing Type (2) Package Type (3) Lead Plating</p>	<p>(1) R: Tape Reel, T: Tube (2) N24: HTSSOP-24 (3) G: Halogen Free, L: Lead Free, Blank: Pb/Sn</p>
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## ■ PIN CONFIGURATION



## ■ PIN DESCRIPTION

PIN NO	PIN NAME	I/O	DESCRIPTION
1,12,13,24	GND/HS		Ground, connected to thermal pad directly.
11	BYPASS		Connected to voltage divider
2	GAIN0	I	For gain control: Bit 0
3	GAIN1	I	For gain control: Bit 1
5	LLINEIN	I	Line input for Left channel, available when pin17 is held low.
6	LPHIN	I	Headphone input Left channel, available when pin17 is held high.
7,18	PV <sub>DD</sub>	I	Supply voltage
8	R <sub>IN</sub>	I	Differential input for Right channel. And for single-ended inputs is also AC ground.
10	L <sub>IN</sub>	I	Differential input for Left channel. And for single-ended inputs is also AC ground.
14	PC-BEEP	I	PC-BEEP mode input. When at least eight continuous > 1-V <sub>PP</sub> square waves is input to this pin, PC-BEEP is enabled.
15	SE/BTL	I	Low for BTL mode, high for SE mode.
17	HP/LINE	I	Input of MUX control. Being high to select the inputs of Pin6, 20, and low to select inputs of PIN 5, 23.
19	V <sub>DD</sub>		Analog V <sub>DD</sub> Supply voltage
20	RHPIN	I	Right channel headphone input, selected when HP/LINE pin is held high.
22	SHUTDOWN	I	in shutdown mode when held low, expect PC-BEEP remains active.
23	RLINEIN	I	Headphone input right channel, available when pin17 is held low.
4	L <sub>OUT+</sub>	O	Positive output for Left channel in BTL mode, positive output in SE mode.
9	L <sub>OUT-</sub>	O	Negative output for Left channel, and high impedance in SE mode.
16	R <sub>OUT-</sub>	O	Negative output for Right channel, and high impedance in SE mode.
21	R <sub>OUT+</sub>	O	Positive output for right channel in BTL mode, positive output in SE mode.

### ■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	6	V
Power Dissipation $T_A \leq 25^\circ\text{C}$	$P_D$	2.7	W
Operating Free-Air Temperature Range	$T_A$	-40~+85	$^\circ\text{C}$
Operating Junction Temperature Range	$T_J$	150	$^\circ\text{C}$
Storage Temperature Range	$T_{STG}$	-65~+150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

### ■ ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DC ELECTRICAL CHARACTERISTICS</b>						
Supply voltage	$V_{DD}$		4.5	5	5.5	V
High-Level Input voltage	$V_{IH}$	SHUTDOWN, SE/BTL, HP/LINE, GAIN0, GAIN1	3.5			V
Low-Level Input voltage	$V_{IL}$	SHUTDOWN, SE/BTL, HP/LINE, GAIN0, GAIN1			1	V
DC Differential Output Voltage	$V_{OUT(DIFF)}$	$V_{DD} = 5V, \text{Gain} = 2V/V$		5	50	mV
Supply Current in Mute Mode	$I_{DD}$	$V_{DD} = 5V, \text{Stereo BTL}$		7.5	13	mA
		$V_{DD} = 5V, \text{Stereo SE}$		4	7	
Supply Current, Shutdown Mode	$I_{DD(SD)}$	$V_{DD} = 5V$		160	300	$\mu\text{A}$
<b>AC ELECTRICAL CHARACTERISTICS</b> $V_{DD} = 5.0V, R_L = 4\Omega$ , unless otherwise specified						
Output Power	$P_{OUT}$	THD = 1%, BTL, $R_L = 4\Omega, G = 2V/V$		2		W
		THD = 1%, BTL, $R_L = 8\Omega, G = 2V/V$		1.25		
		THD = 10%, BTL, $R_L = 4\Omega, G = 2V/V$		2.5		
		THD = 10%, BTL, $R_L = 8\Omega, G = 2V/V$		1.6		
		THD = 0.1%, SE, $R_L = 32\Omega$		85		mW
Total Harmonic Distortion Plus Noise	THD+N	$P_{OUT} = 1.6W, \text{BTL}, R_L = 4\Omega, G = 2V/V$		100		m%
		$P_{OUT} = 1W, \text{BTL}, R_L = 8\Omega, G = 2V/V$		60		
		$P_{OUT} = 75mW, \text{SE}, R_L = 32\Omega$		80		
		$V_I = 1V, \text{BTL}, R_L = 10k\Omega, \text{SE}$		30		
Max Output Power Bandwidth	$B_{OM}$	THD = 5%		15		kHz
Power Supply Ripple Rejection	PSRR	$F = 1\text{kHz}, \text{BTL}, G = 2V/V, C_{BYP} = 1\mu\text{F}$		68		V/V
Channel-to-Channel Output Separation		$F = 1\text{kHz}$		80		V/V
Line/HP Input Separation				80		V/V
BTL Attenuation (SE mode)				85		V/V
Signal-to-Noise Ratio	SNR	$P_{OUT} = 500mW, \text{BTL}, G = 2V/V$		90		V/V
Output Noise Voltage	eN	BTL, $G = 2V/V, A$ Weighted filter		45		$\mu\text{V(rms)}$

Note: Output power is measured at the output terminals of the IC at 1kHz.

## ■ APPLICATION INFORMATION

### Shutdown Mode Operating

INPUT			AMPLIFIER	
HP/LINE	SE/BTL	SHUTDOWN	INPUT	OUTPUT
X	X	L	X	MUTE
L	L	H	LINE	BTL
L	H	H	LINE	SE
H	L	H	HEADPHONE	BTL
H	H	H	HEADPHONE	SE

X: Ignore

L: Low

H: High

### C<sub>i</sub> (Input Capacitor)

The value of C<sub>i</sub> is important to consider as it directly affects the bass performance of the application circuit. When C<sub>i</sub> is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation, its value can be calculate by this equation:

$$C_i = 1 / (2\pi R_i F_c)$$

R<sub>i</sub>: Input Impedance

F<sub>c</sub>: High-pass Filter's Frequency

The low leakage tantalum or ceramic capacitors are suggested to be used as the input coupling capacitors, because of the small leakage current of the input ca-pacitors will cause the dc offset voltage at the input to the amplifier that reduces the operation headroom, especially at the high gain applications. It is important to let the positive side connecting to the higher dc level of the application when using the polarized capacitors.

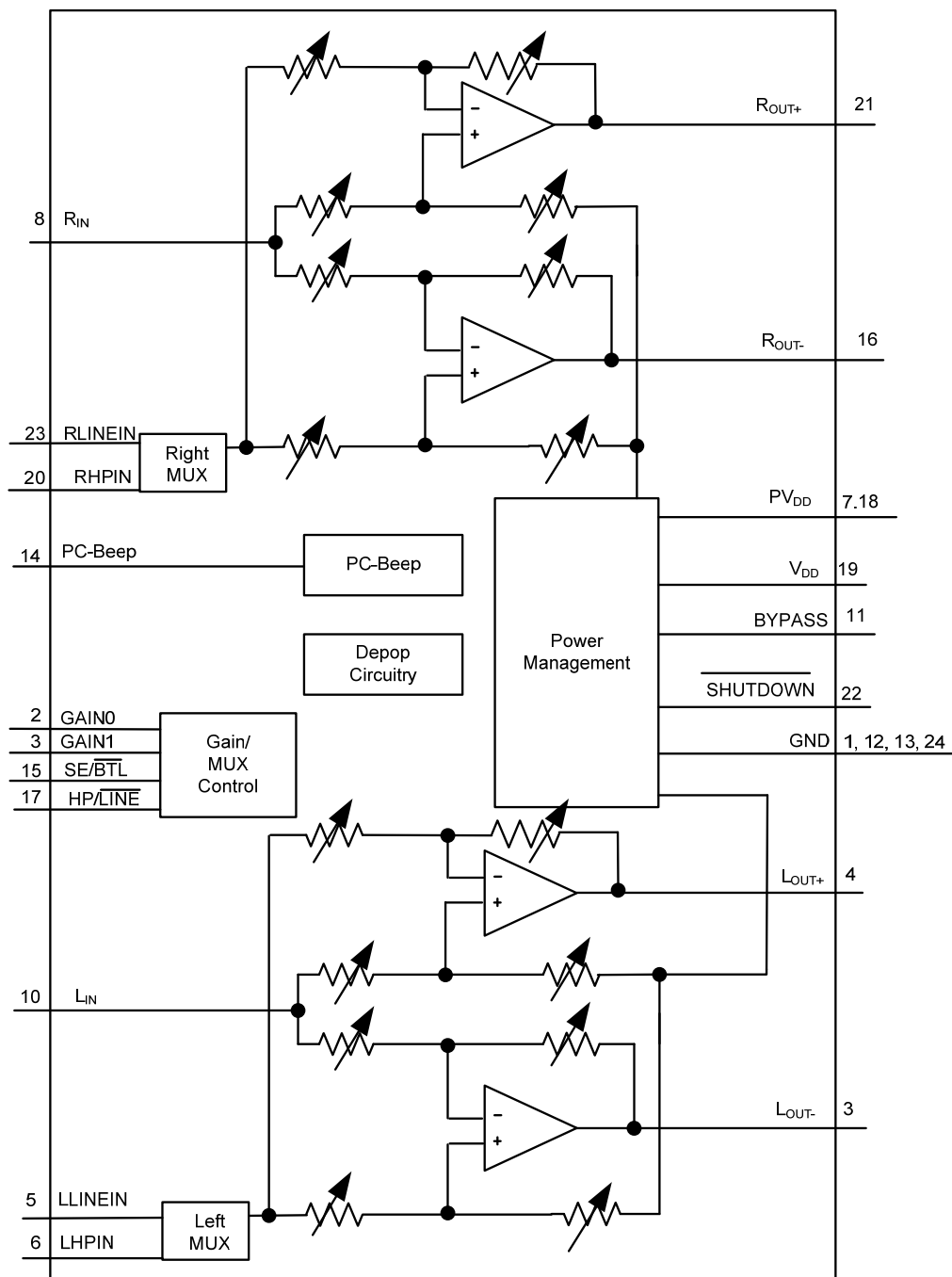
### Gain setting (Vs Gain0, Gain1 and R<sub>i</sub>, SE/BTL)

Gain setting is determined by GAIN0 and GAIN1. The gains listed in the next table are realized by changing the taps on the input resistors inside the amplifier which will cause the internal input impedance(R<sub>i</sub>) to be dependent on the gain setting as we can see listed in the next table.

A <sub>v</sub> (V/V)	GAIN0	GAIN1	SE/BTL	R <sub>i</sub> (kΩ)
2	0	0	0	90
6	0	1	0	45
12	1	0	0	30
24	1	1	0	15
1	X	X	1	

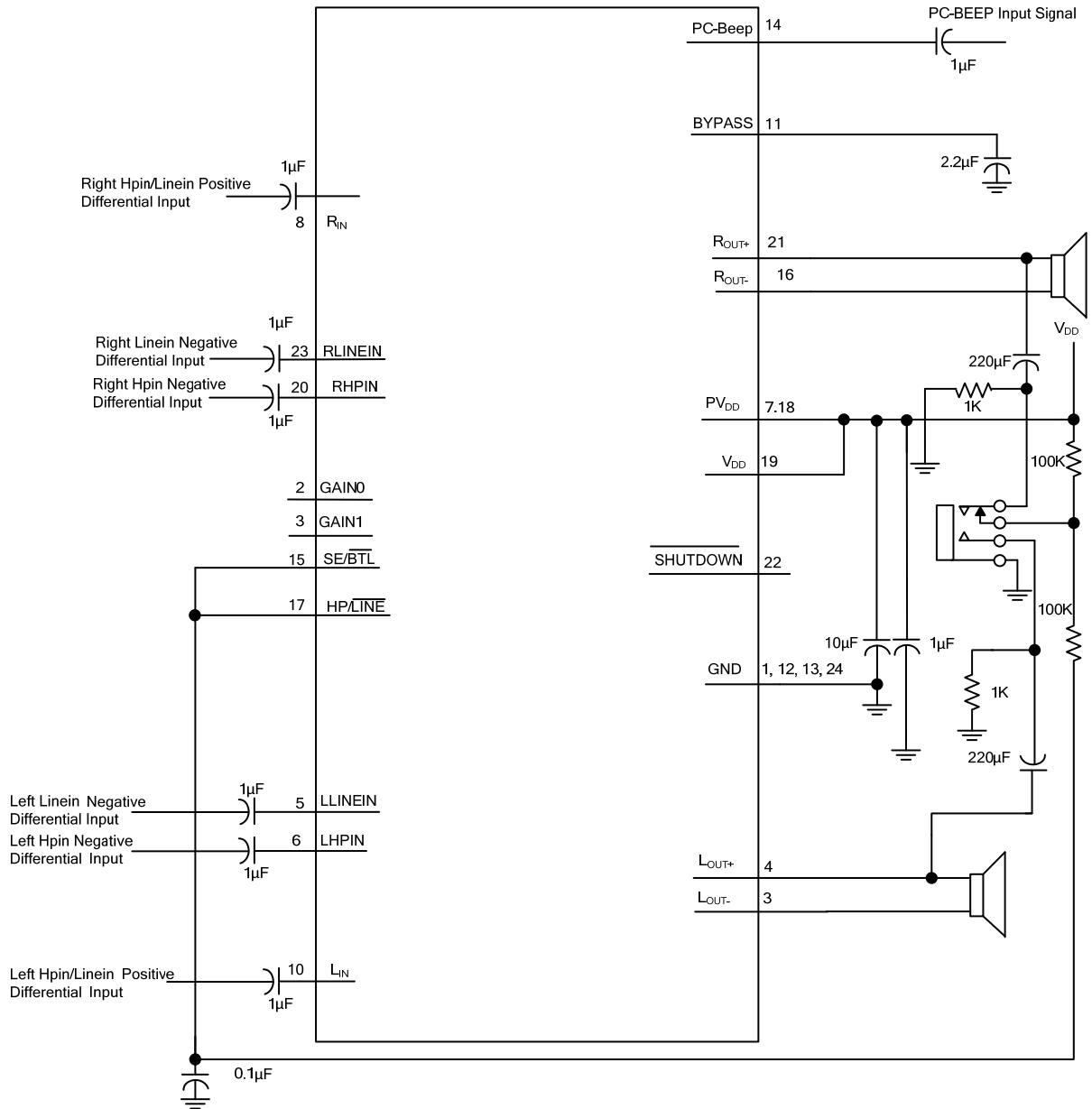
X: Ignore

■ BLOCK



## TYPICAL APPLICATION CIRCUIT

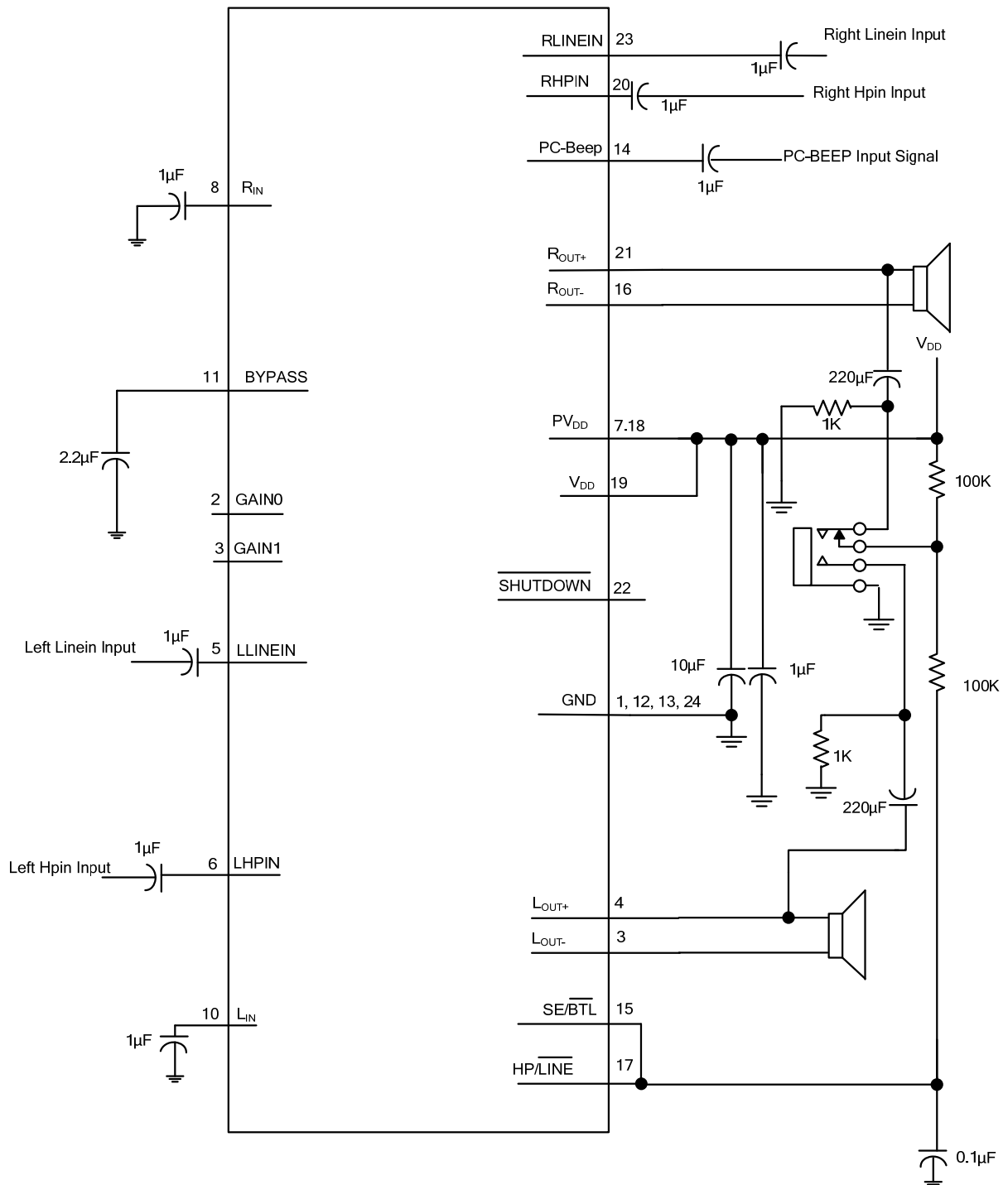
### FOR DIFFERENTIAL INPUTS



Note: A 0.1µF ceramic capacitor must be placed much closely to the IC. For filtering lower frequency noise signals, a larger electrolytic capacitor of 10µF or greater should be placed as close as possible to the audio power amplifier.

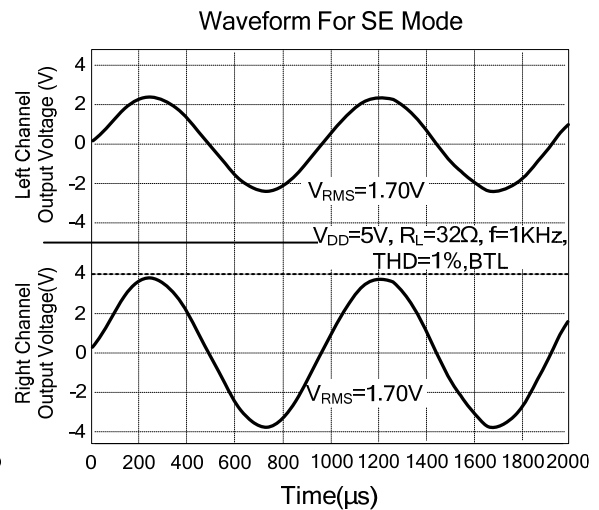
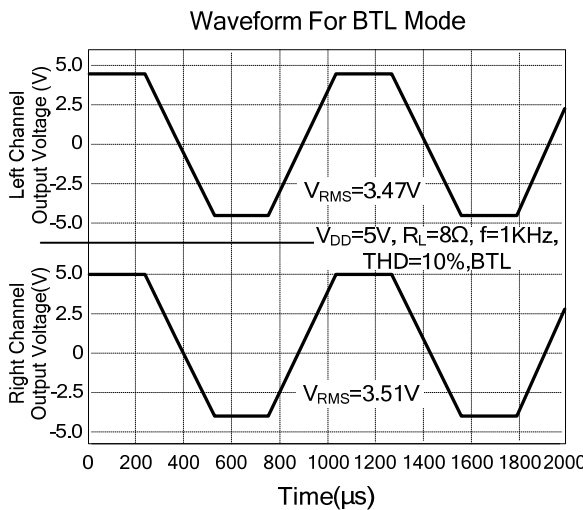
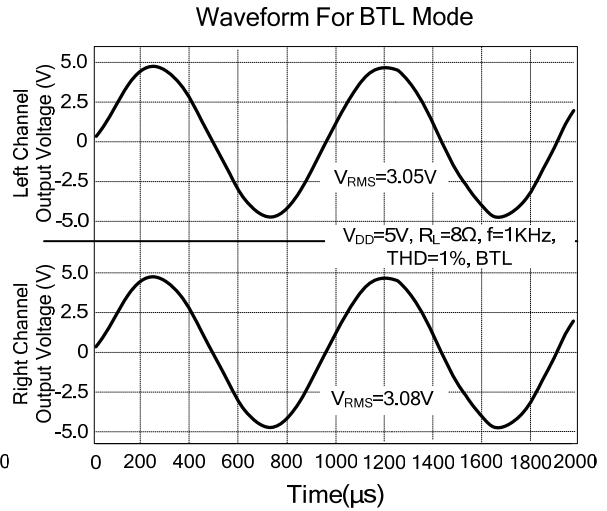
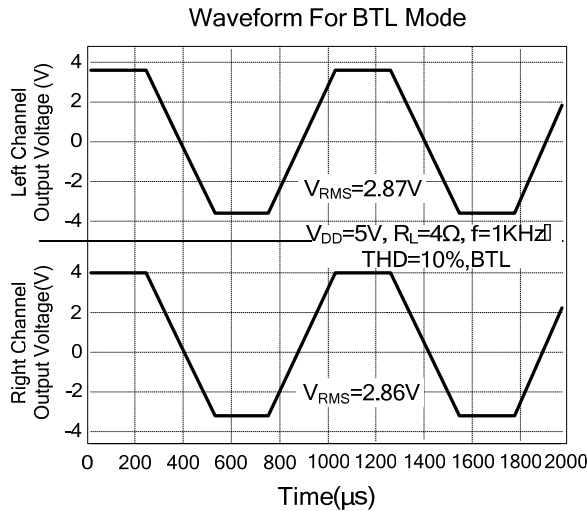
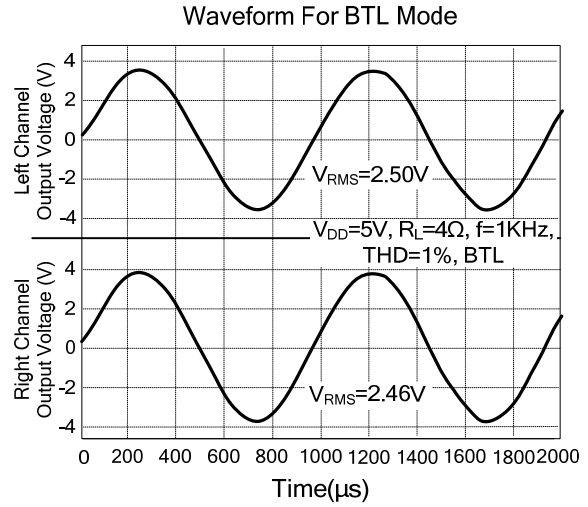
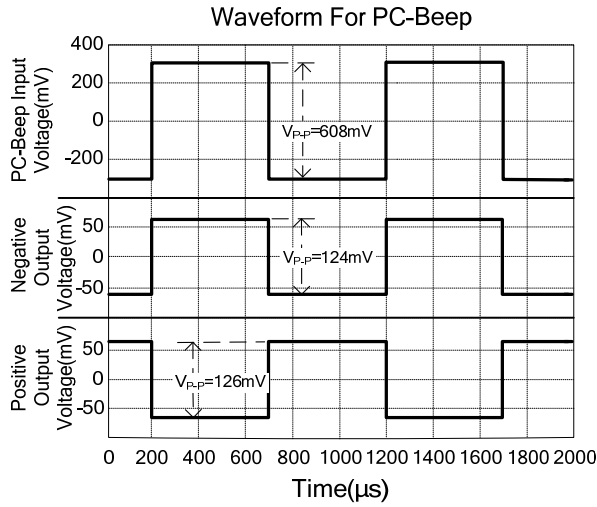
## ■ TYPICAL APPLICATION CIRCUIT(Cont.)

### FOR SINGLE-ENDED INPUTS



Note: 1μF ceramic capacitor should be placed as close as possible to the IC to filter the higher-frequency noise.

■ TYPICAL CHARACTERISTICS





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