

Version : 1.1

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TECHNICAL SPECIFICATION

MODEL NO. : PA064DS1

☐ Customer's Approved

Customer _____

Date _____

By _____

☐ PVI's Confirmation

Approved By _____

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TECHNICAL SPECIFICATION

CONTENTS

NO.	ITEM	PAGE
-	Cover	1
-	Contents	2
1	Application	3
2	Features	3
3	Mechanical Specifications	3
4	Mechanical Drawing of TFT-LCD module	4
5	Input / Output Terminals	5
6	Absolute Maximum Ratings	7
7	Electrical Characteristics	7
8	Power Sequence	20
9	Optical Characteristics	20
10	Handling Cautions	24
11	Reliability	25
12	Indication of Lot Number Label	25
13	Block Diagram	26
14	Packing	27
-	Revision History	28

1. Application

This technical specification applies to 6.4" color TFT-LCD module , PA064DS1. The applications of the panel are car TV , portable DVD , GPS , multimedia applications and others AV system.

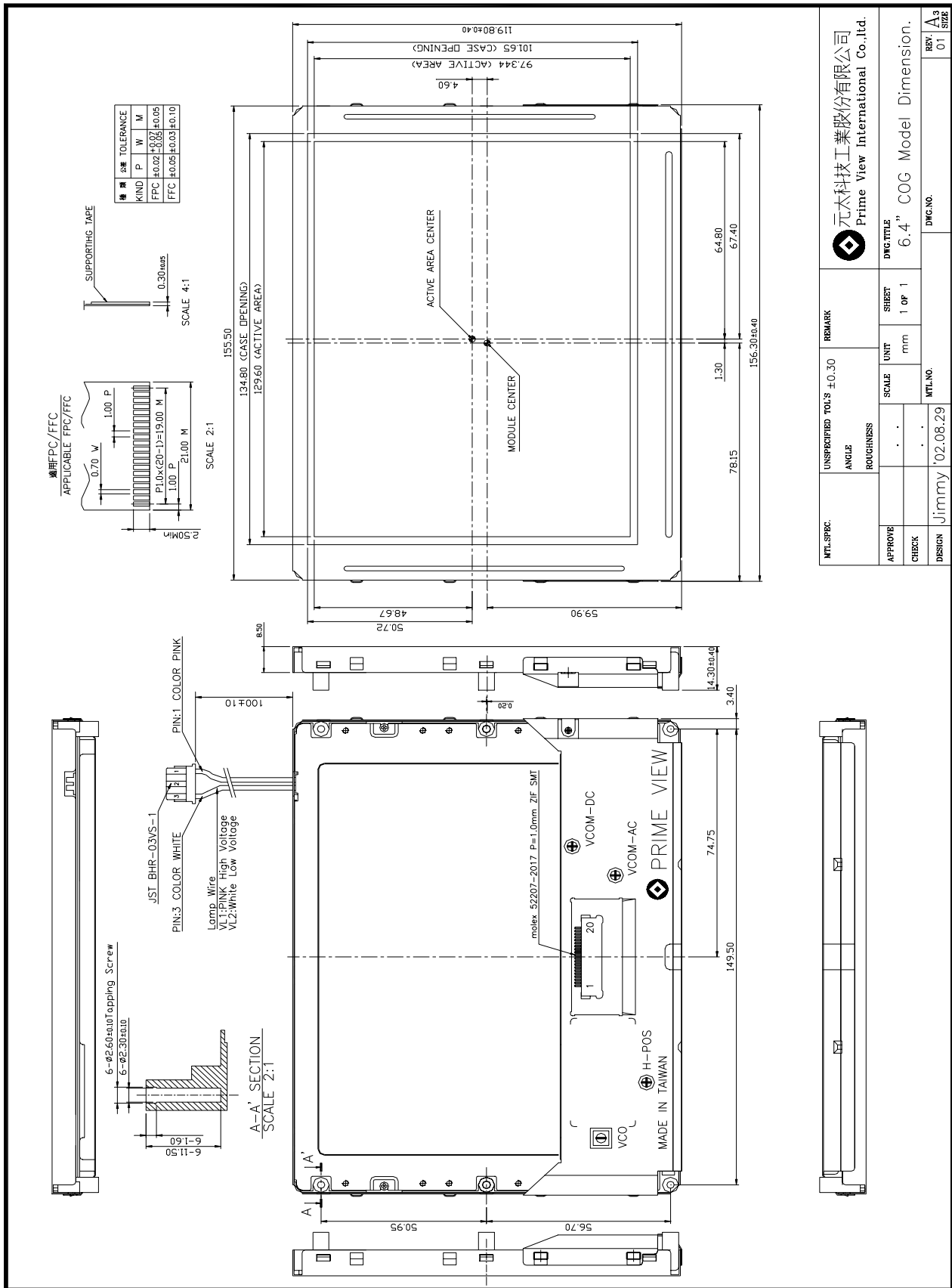
2. Features

- . Compatible with NTSC & PAL system
- . Pixel in stripe configuration
- . Slim and compact
- . High Brightness
- . Image Reversion : Up/Down and Left/Right

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	6.4 (diagonal)	inch
Surface Treatment	Anti-Glare+WV film	
Display Format	960 (H)×234 (V)	dot
Active Area	129.60 (H)×97.34 (V)	mm
Dot Pitch	0.135 (H)×0.416 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	156.3 (W)×119.8 (H)×14.3 (D)(Typ.)	mm
Weight	235±10	g

4. Mechanical Drawing of panel



5. Input / Output Terminals

5-1) TFT-LCD Panel Driving

Pin No	Symbol	I/O	Description	Remark
1	$\overline{\text{HSY}}$	I/O	Horizontal Sync. Input / Output	Note 5-1
2	POLC	O	Video Polarity Alternating Signal	
3	CSY	I	Composite Sync. Signal	Note 5-1
4	V_{GH}	I	Gate on voltage	Note 5-2
5	V_{GL}	I	Gate off voltage	Note 5-3
6	V_{B}	I	Video Input B	
7	V_{R}	I	Video Input R	
8	V_{G}	I	Video Input G	
9	GND	I	GND	
10	V_{DD}	I	Digital power input	Note 5-4
11	V_{CC}	I	Analogue power input for source driver	Note 5-5
12	GND	I	GND	
13	CKC	I	Select Pin for Internal / External Clock Mode	Note 5-1
14	$\overline{\text{VS}}\overline{\text{Y}}$	I/O	Vertical Sync. Input / Output	
15	PSI	I	Synchronize Pulse for Decoder	Note 5-6
16	COMPS	I	Select Pin for Composite Sync. Mode & Sync. Separate Mode	Note 5-1
17	$\overline{\text{VI}}\overline{\text{Y}}$	I	Vertical Sync. Input Pin for Sync. Separate Mode	
18	U/D	I	Up/Down Control for gate driver	Note 5-8
19	R/L	I	Left/Right Control for source driver	Note 5-7
20	NP	I	NTSC / PAL Input	Note 5-9

Note 5-1 : The relation between Pin13 (CKC) and Pin 16 (COMPS) :

Pin13 (CKC)	Pin16 (COMPS)	Pin 1 ($\overline{\text{HSY}}$)	Pin3 (CSY)	Pin14 ($\overline{\text{VS}}\overline{\text{Y}}$)	Pin17 ($\overline{\text{VI}}\overline{\text{Y}}$)
High	High	$\overline{\text{HSY}}$ output	CSY input	$\overline{\text{VS}}\overline{\text{Y}}$ output	NC
High	Low	$\overline{\text{HSY}}$ output	CSY (Hsync.) input	$\overline{\text{VS}}\overline{\text{Y}}$ output	$\overline{\text{VI}}\overline{\text{Y}}$ (Vsync.) input
Low	-	Hsync. input	External clock	Vsync. input	NC

Note 5-1-1 : CKC = High , COMPS = High (Composite sync. mode & Internal clock mode)

- If CKC = 1, COMPS = 1 the phase lock loop (PLL) is adopted in the LCD module (internal clock mode).
- Input sync. is CSY.
- Output sync. are Horizontal Sync ($\overline{\text{HSY}}$, Pin 1) and Vertical Sync ($\overline{\text{VS}}\overline{\text{Y}}$, Pin 14).

Note 5-1-2 : CKC = High , COMPS = Low (Sync. Separate mode & Internal clock mode)

- If CKC = 1, COMPS = 0 the phase lock loop (PLL) is adopted in the LCD module (internal clock mode).
- Input sync. are Horizontal sync. (CSY , Pin3) and Vertical sync. ($\overline{\text{VIY}}$, Pin17).
- Output sync. are Horizontal Sync ($\overline{\text{HSY}}$, Pin 1) and Vertical Sync ($\overline{\text{VSX}}$, Pin 14).

Note 5-1-3 : CKC = Low , COMPS = Don't care (External clock mode)

- If CKC = 0 , the phase lock loop (PLL) is not adopted in the LCD module.
- If CKC = 0 , the external clock input frequency of Pin 3 is 6.4 MHz.
- Input external Vertical Sync ($\overline{\text{VSX}}$, Pin 14) and Horizontal Sync ($\overline{\text{HSY}}$, Pin 1) to synchronize the LCD module.
- The pulse width of external Horizontal Sync input is $4.7\mu\text{s} \pm 2\mu\text{s}$. The pulse width of external Vertical Sync input is 2H~4H.
- The pulse length of external input Vertical Sync of system is $262\text{H} \pm 4\text{H}$.

Note 5-1-4 : If there is any question about CKC = 0 , please contact PVI.

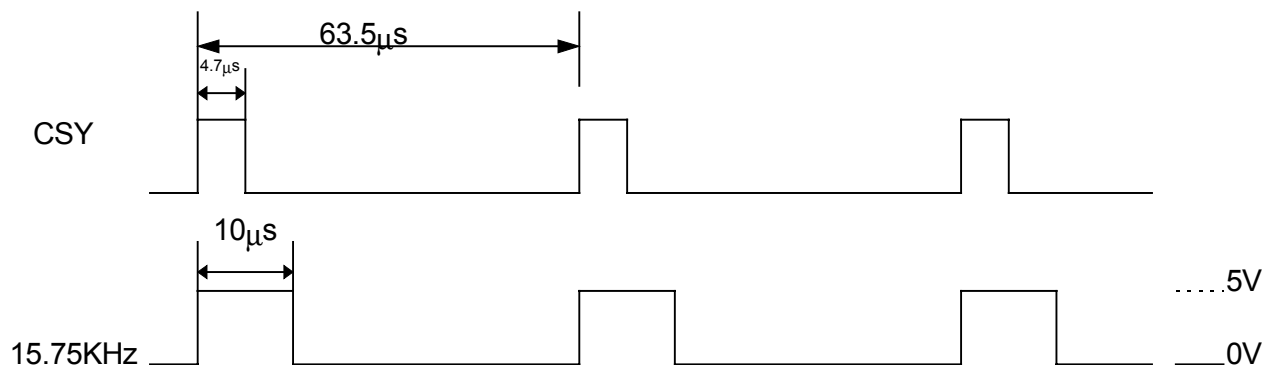
Note 5-2 : V_{GH} TYP. = +17V

Note 5-3 : V_{GL} TYP. = -15V

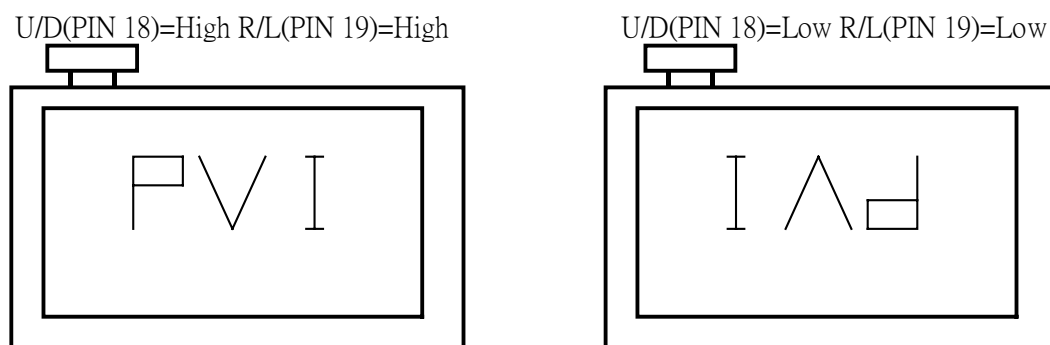
Note 5-4 : V_{DD} TYP. = +5V

Note 5-5 : V_{CC} TYP. = +5V

Note 5-6 : The frequency of PSI is 15.75KHz.



Note 5-7,5-8 : The definitions of U/D & R/L



Note 5-9 : NTSC = Hi (+5V) , PAL = LOW (0V).

6. Absolute Maximum Ratings

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

GND = 0 V , Ta = 25 °C

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage For Source Driver	Analog	V_{CC}	-0.3	+7.0	V	
	Digital	V_{DD}	-0.3	+7.0		
Supply Voltage For Gate Driver	Positive	V_{GH}	-0.3	+45	V	
	Negative	V_{GL}	-23	+0.3	V	
		$V_{GH}-V_{GL}$	+15	+40	V	
Analog input voltage		V_{Video}	-0.3	+7.3	V	Note 6-1
Digital input signals			-0.5	+5.5	V	Note 6-2
Digital output signals			-0.5	+5.5	V	
Storage Temperature			-30	+80	°C	
Operation Temperature			-20	+70	°C	Note 6-3

Notes 6-1 : Analog Input Voltage means V_R, V_G, V_B .

Notes 6-2 : $\overline{HSY}$, POLC , CSY , $\overline{VS_Y}$, CKC , PSI , COMPS , $\overline{VI_Y}$

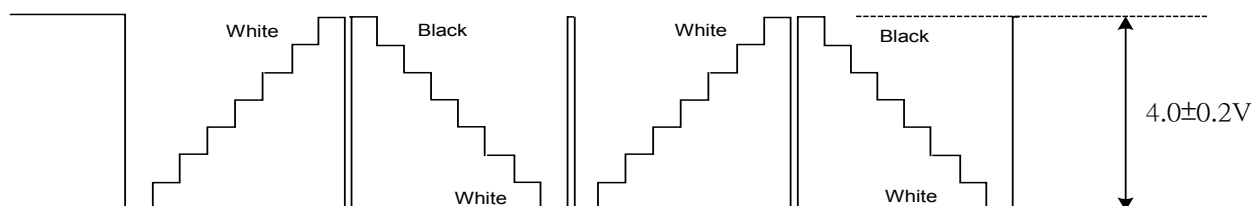
Notes 6-3 : Operating Temperature define that contrast, response time, other display optical character are Ta=+25.

7. Electrical Characteristics

7-1) Operating Condition

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply		V_{CC}	+4.5	+5.0	+5.5	V	
		V_{DD}	+4.5	+5.0	+5.5	V	
		V_{GH}	+15.0	+17.0	+19.0	V	
		V_{GL}	-16.0	-15.0	-14.0	V	DC Component of V_{GL}
Video Signal (V_R, V_G, V_B)		V_{iAC}	-	+4.0	+4.2	V_{P-P}	AC Component Note 7-1
		V_{iDC}	-	+2.5	-	V	DC Component
Digital input voltage	H Level	V_{IH}	+0.7 V_{DD}	-	V_{DD}	V	
	L Level	V_{IL}	-0.3	-	+0.3 V_{DD}	V	
Digital output voltage	H Level	V_{OH}	+0.7 V_{DD}	-	V_{DD}	V	
	L Level	V_{OL}	-0.3	-	+0.3 V_{DD}	V	

Note 7-1 : Both NTSC and PAL system Video Signal input waveform is based on 8 steps gray scale.



7-2) Current Consumption (GND=0V)

Ta= 25 °C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Current for Driver	I _{GH}	V _{GH} =+17V	-	0.07	0.08	mA	
	I _{GL}	V _{GL} =-15V	-	9.81	10.31	mA	V _{GL} center voltage
	I _{CC}	V _{CC} =+5V	-	6.67	7.65	mA	
	I _{DD}	V _{DD} =+5V	-	22.22	24.64	mA	

7-3) Backlight driving & Power Consumption

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
3	VL2	Input terminal (Low voltage side)	Note 7-3

Note 7-3 : Low voltage side of backlight inverter connects with Ground of inverter circuits.

Ta= 25 °C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V _L	450	560	730	Vrms	I _L =6mA
Lamp current	I _L	4	6	8	mA	
Lamp frequency	F _L	40	60	80	KHz	Note 7-4
Kick-off voltage(25°C)	Vs	-	730	840	Vrms	

Note 7-4 : The waveform of lamp driving voltage should be as closed to a perfect SIN wave as possible.

Power Consumption

Ta= 25 °C

Parameter	Symbol	Conditions	TYP.	Unit	Remark
LCD Panel Power Consumption			292.79	mW	Note 7-5
Backlight Lamp Power Consumption			3.36	W	Note 7-6
Total Power Consumption			3.65	W	

Note 7-5 : The power consumption for backlight is not included.

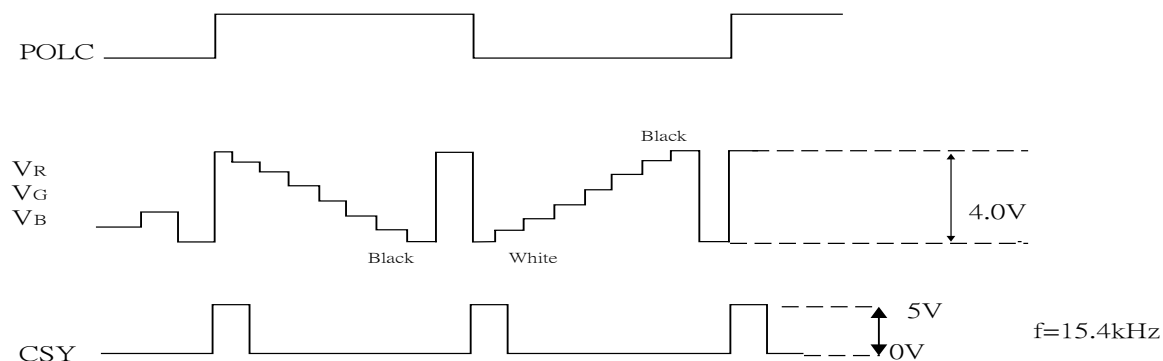
Note 7-6 : Backlight lamp power consumption is calculated by I_L×V_L.

7-4) Input / Output Connector
A) LCD Module Connector

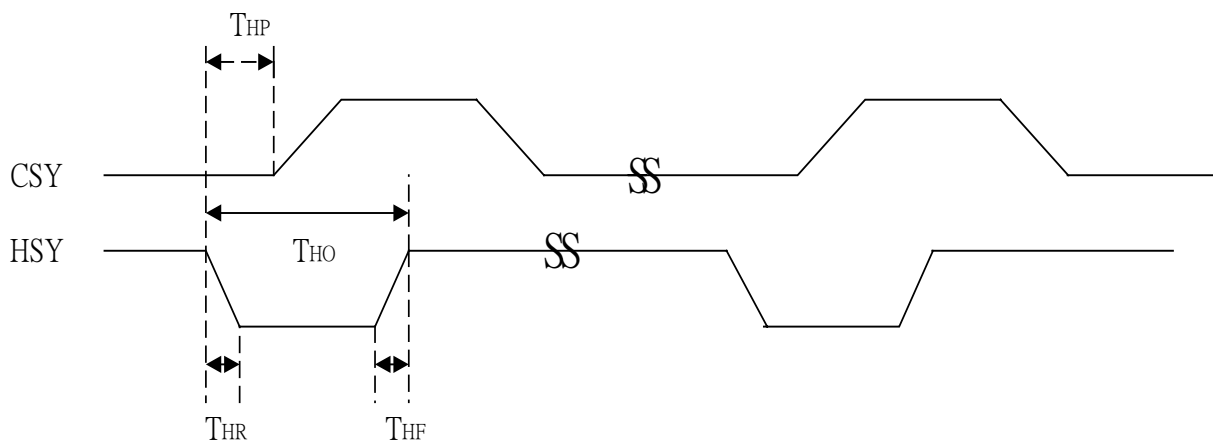
52207-2017 (Molex)
FFC Up Connector,
20 Pins
Pitch : 1.0 mm

B) Backlight Connector

JST BHR-03VS-1
Pin No. : 3
Pitch : 4 mm
Pink : High Voltage
White : Low Voltage

7-5) Input / Output signal timing chart

a) Composite sync. & sync. separate mode's timing

Parameter			Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Horizontal Sync. Output Pulse	Frequency	NTSC	$F_{HO(N)}$	-	15.75	-	KHz	
		PAL	$F_{HO(P)}$	-	15.63	-	KHz	
	Pulse Width		T_{HO}	4.4	4.7	5.0	μs	
	Phase Difference		T_{HP}	0	2	-	μs	
	Rising Time		T_{HR}	-	-	0.05	μs	
	Falling Time		T_{HF}	-	-	0.05	μs	
Vertical Sync. Output Pulse	Frequency	NTSC			$f_h/262.5$			
		PAL			$f_h/312.5$			
	Pulse Width		T_{VO}	-	4H	-	μs	
	Phase Difference	NTSC	$T_{VPO(N)}$	-	1H	-	μs	odd field
		PAL	$T_{VPO(P)}$	-	1H	-	μs	
	Phase Difference	NTSC	$T_{VPE(N)}$	-	1.5H	-	μs	even field
		PAL	$T_{VPE(P)}$	-	0.5H	-	μs	



b) External clock mode's timing

Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Input Clock signal	Frequency	f_{CLI}	5.8	6.4	7.0	MHz	
	Hi pulse width	τ_{WH}	20.0	-	-	ns	
	Lo pulse width	τ_{WL}	20.0	-	-	ns	
	Rising edge time	τ_{rCLI}	-	-	10.0	ns	
	Falling edge time	τ_{fCLI}	-	-	10.0	ns	
Input Horizontal synchronize signal	Frequency	f_{HI}	$f_{CLI} / 430$	$f_{CLI} / 406$	$f_{CLI} / 396$	Hz	
	Pulse width	τ_{HI}	1.0	5.0	9.0	μs	
	Rising edge time	τ_{rHI}	-	-	0.05	μs	
	Falling edge time	τ_{fHI}	-	-	0.05	μs	
Input Vertical Synchronize signal	Frequency	f_{VI}	50	$f_{HI} / 262$	$f_{HI} / 258$	Hz	
	Pulse width	$\tau_{VI(P)}$	1H	3H	5H		
	Rising edge time	τ_{rVI2}	-	-	0.5	μs	
	Falling edge time	τ_{fVI2}	-	-	0.5	μs	
Data set up time		t_{SU1}	25	-	-	ns	
Data hold time		t_{HO1}	25	-	-	ns	
Data set up time		t_{SU2}	1.0	-	-	μs	
Data hold time		t_{HO2}	1.0	-	-	μs	

7-6) Display Time Range

Composite sync. & sync. separate mode

The Both two timing can adjust with H-position

A) When sync. signal of NTSC system is applied.

a) Horizontally

11.35 ~ 61.36 μs .

b) Vertical

22 ~ 255 H

B) When sync. signal of PAL system is applied.

a) Horizontally

11.54 ~ 61.9 μs .

b) Vertical

30 ~ 302 H

c) Odd field : Scan lines 14n+7 14n+13 (n=2,3,4...) are not displayed.

Even field : Scan lines 14n+4 14n+10 (n=2,3,4...) are not displayed.

External clock mode (CKC = " LOW ")

a) Horizontally direction

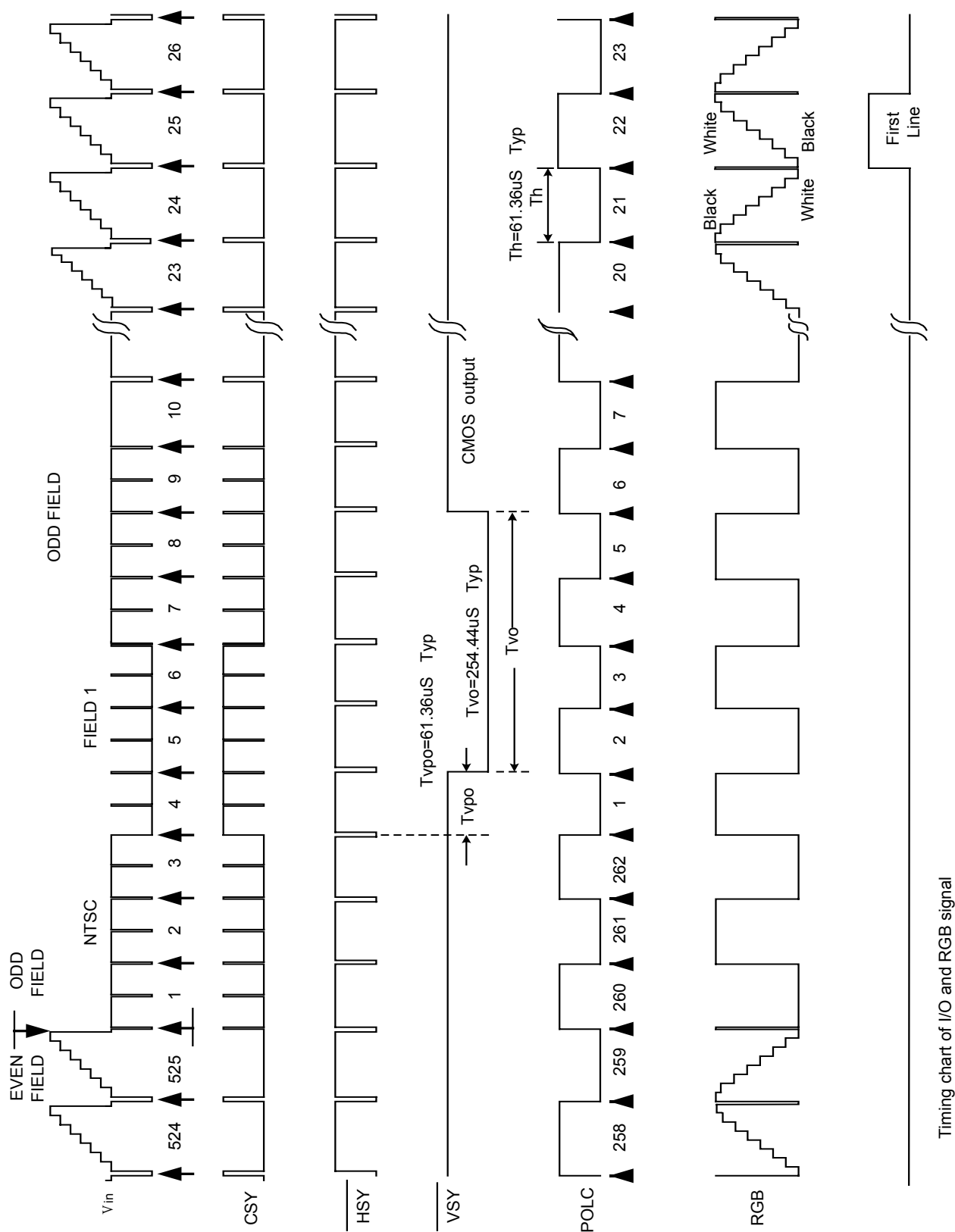
69 ~ 388 CLK from the falling edge of $\overline{HSY}$

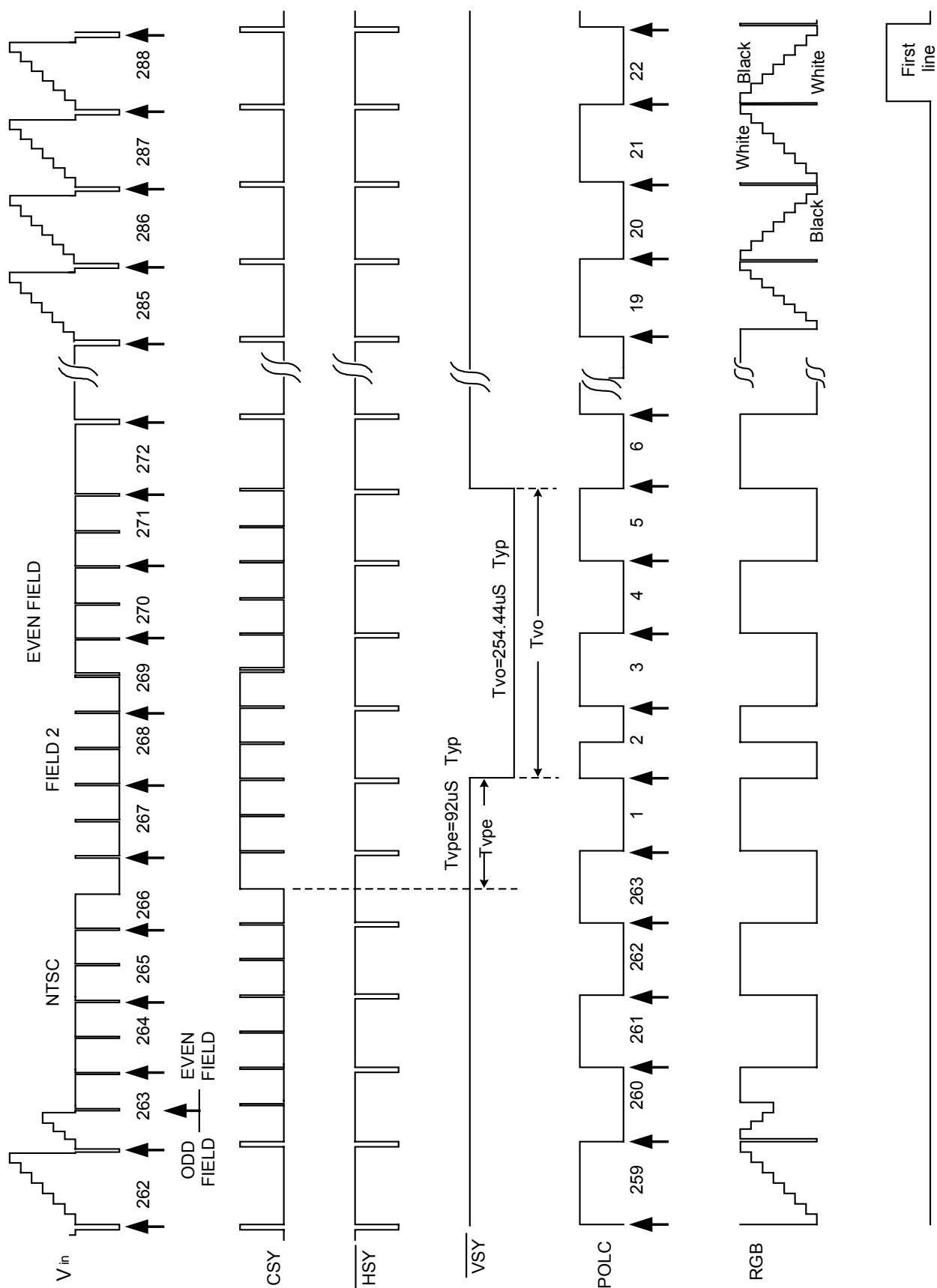
CLK means input external clock. (6.4MHz TYP.)

b) Vertical direction

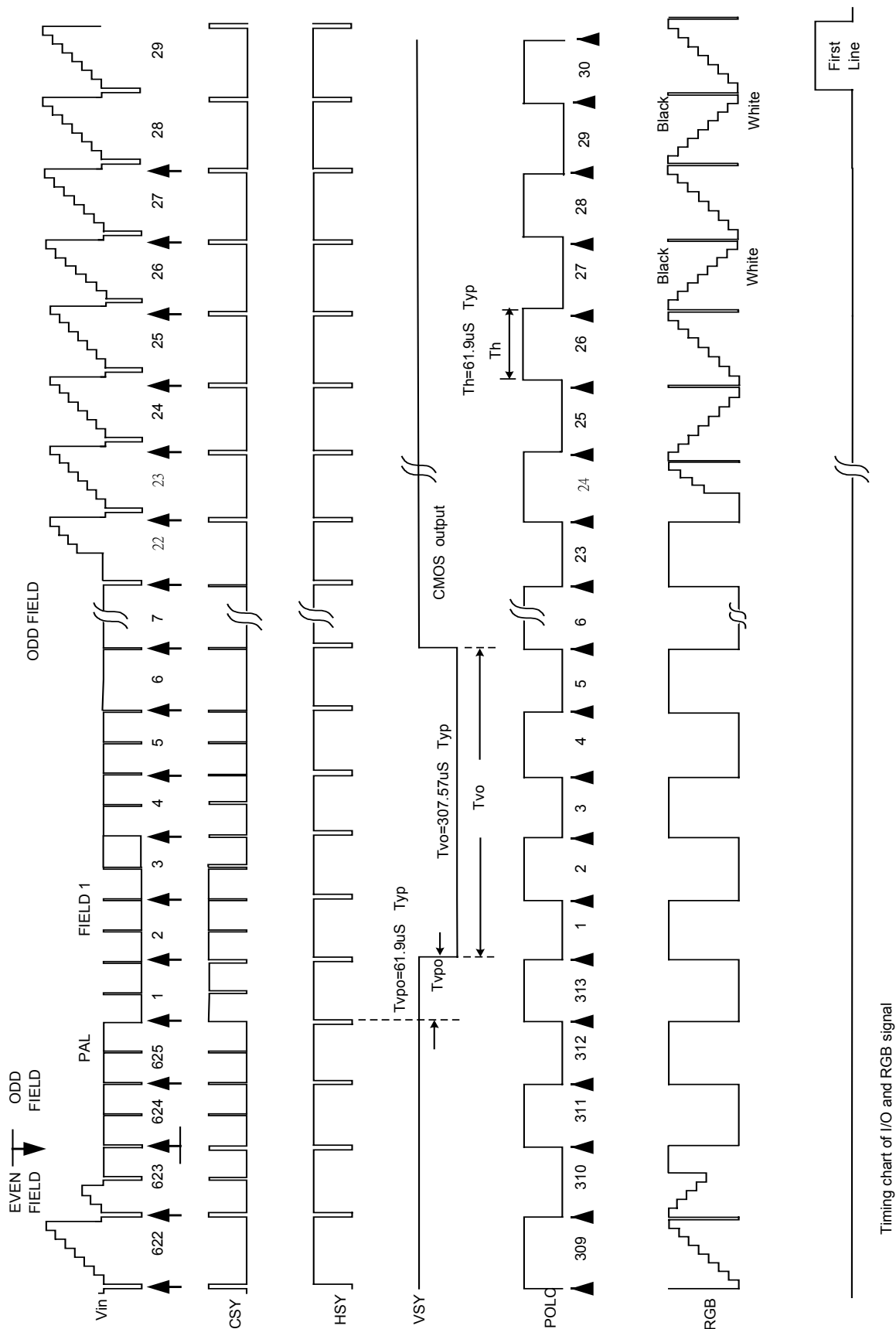
22 ~ 255 H from the falling edge of $\overline{VSY}$

C) NTSC System (Composite sync. mode)

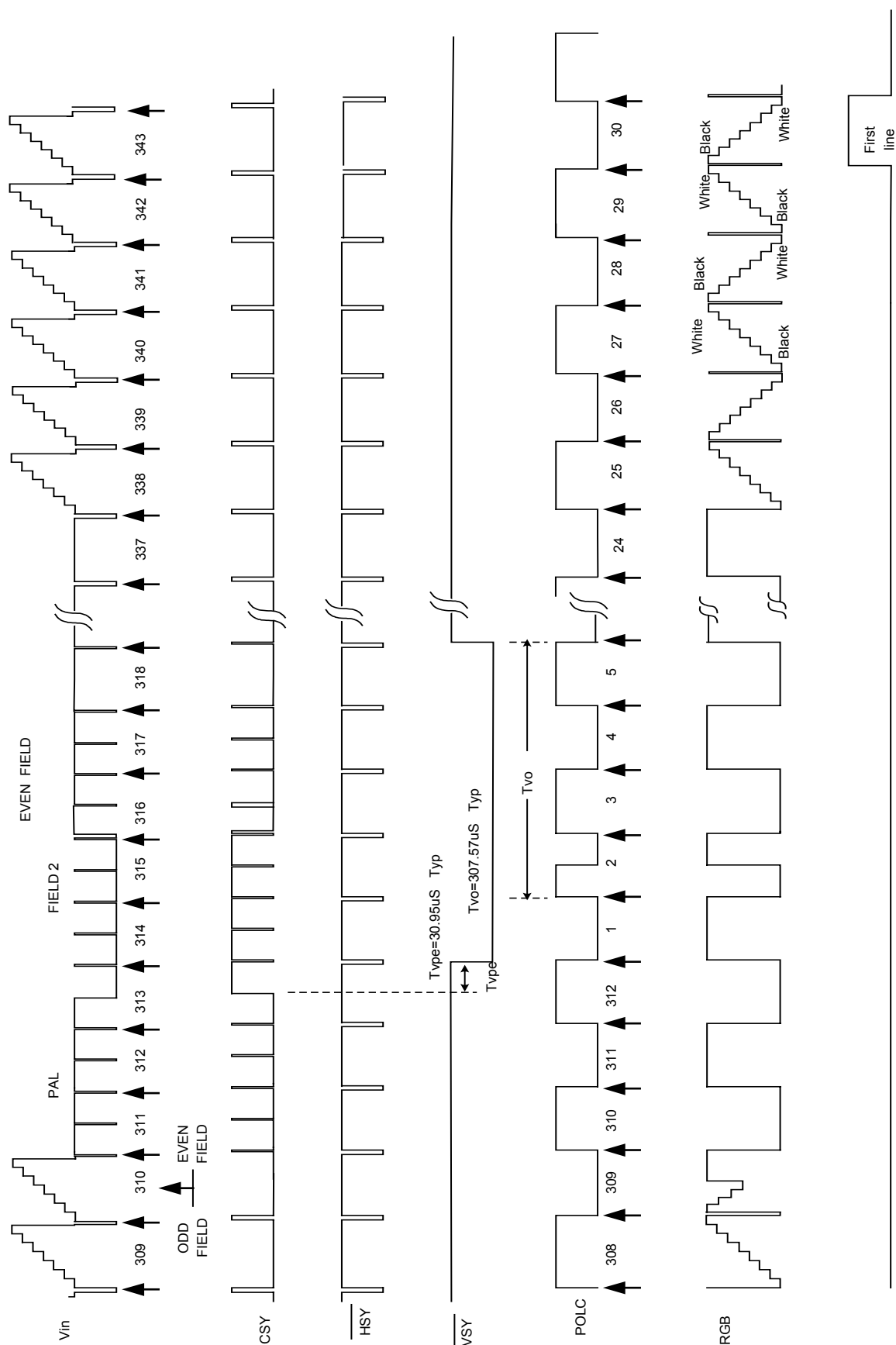




D) PAL System (Composite sync. mode)

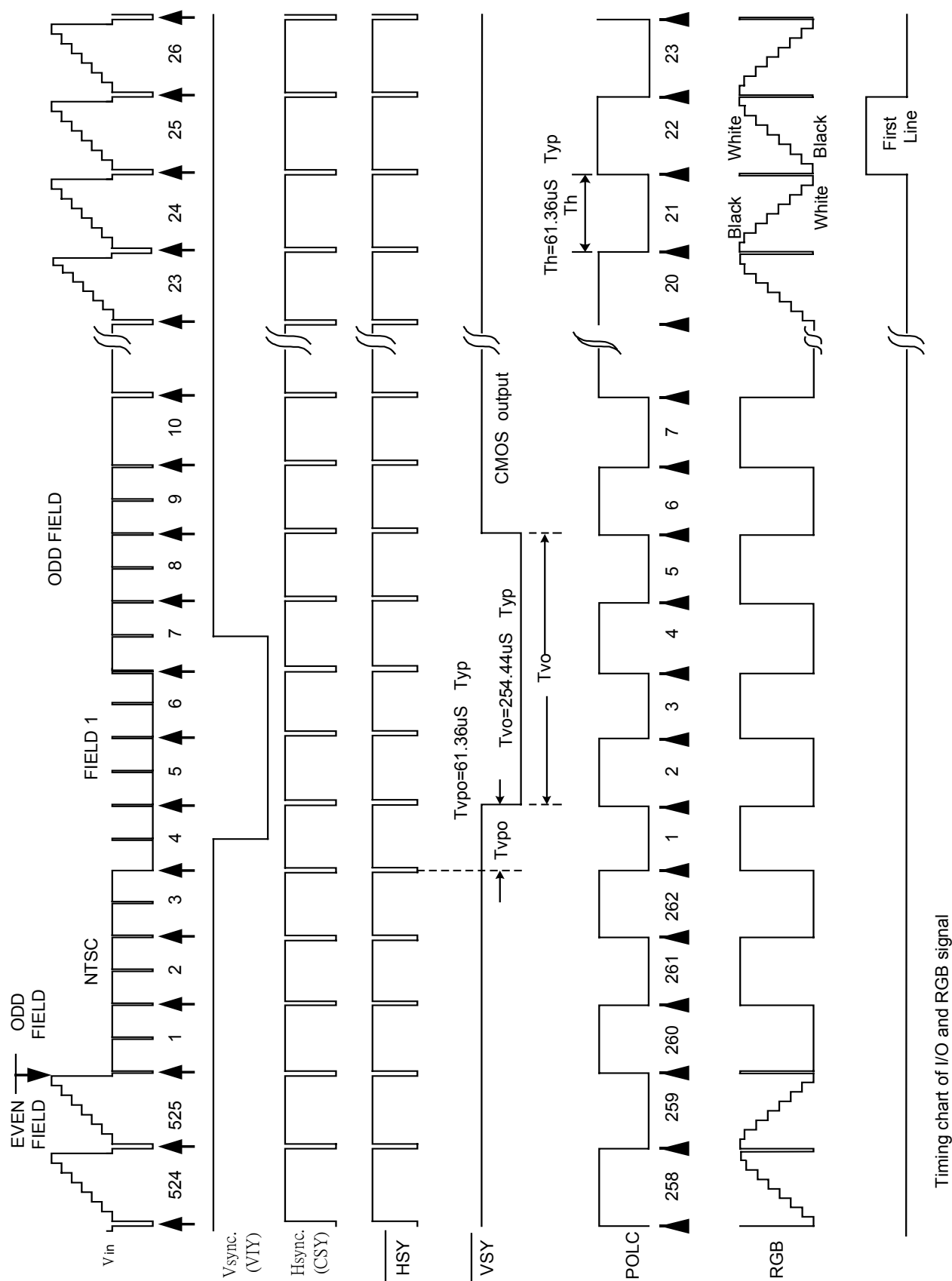


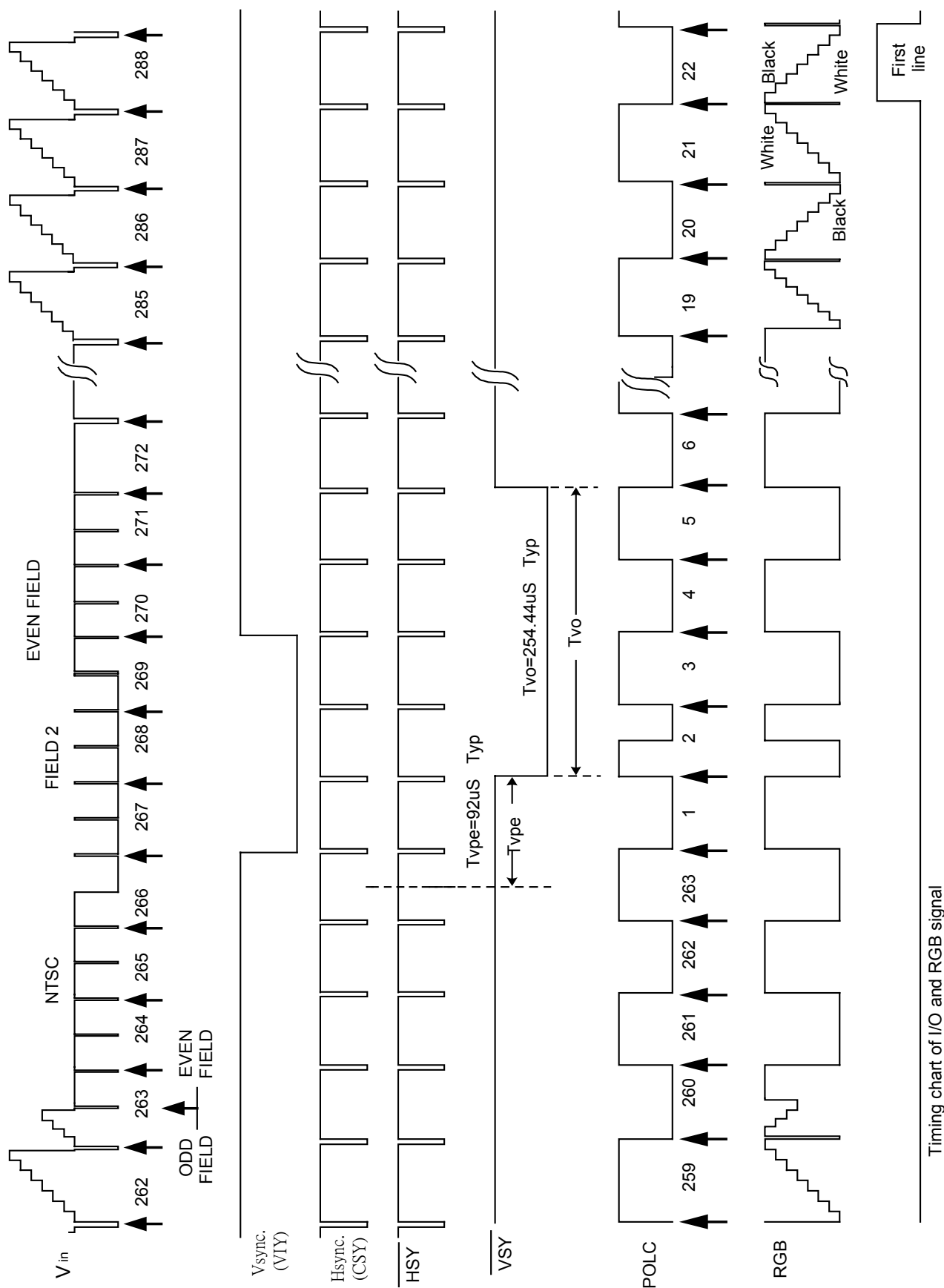
Timing chart of I/O and RGB signal



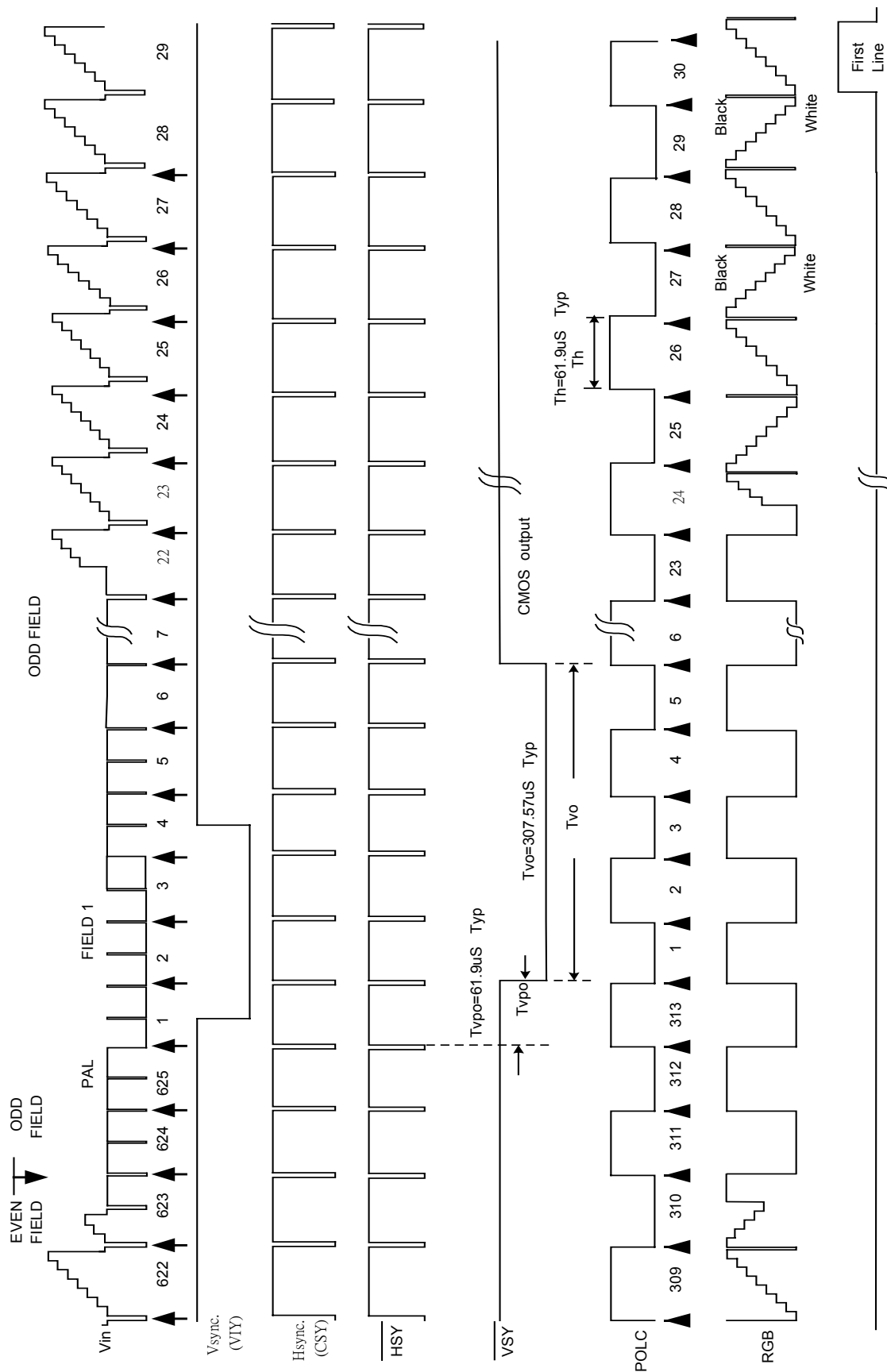
Timing chart of I/O and RGB signal

E) NTSC System (Sync. separate mode)

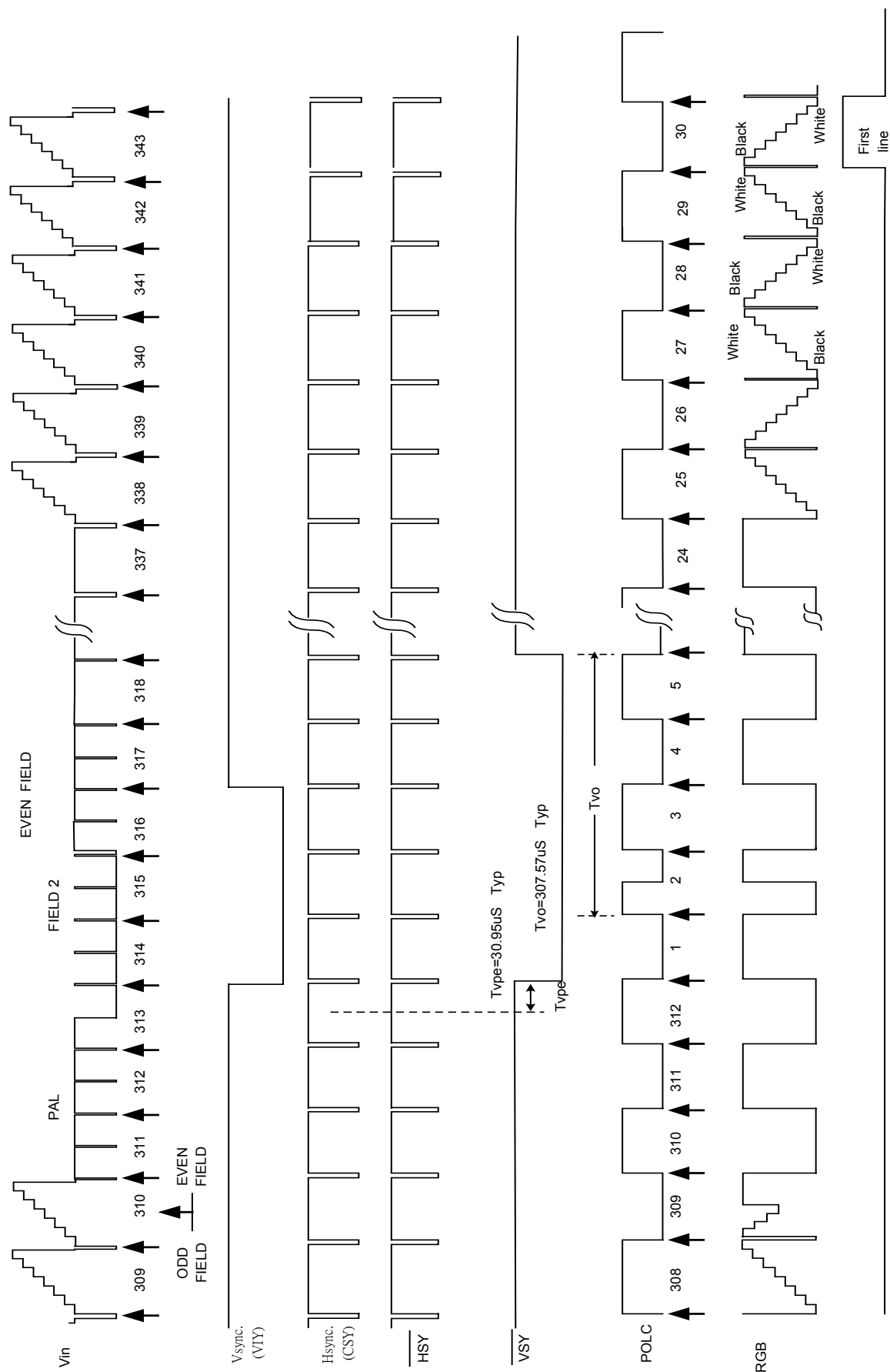




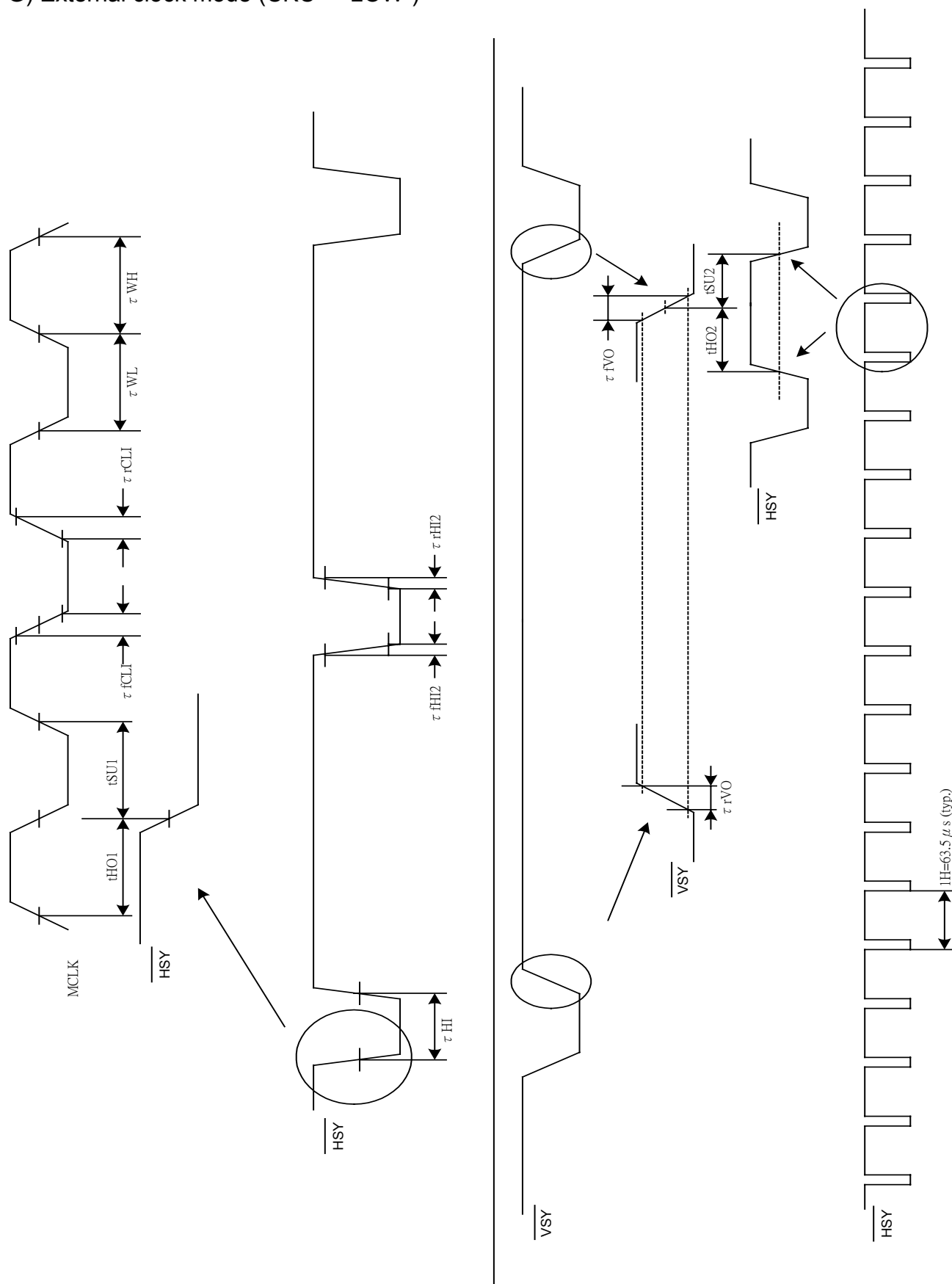
F) PAL System (Sync. separate mode)



Timing chart of I/O and RGB signal

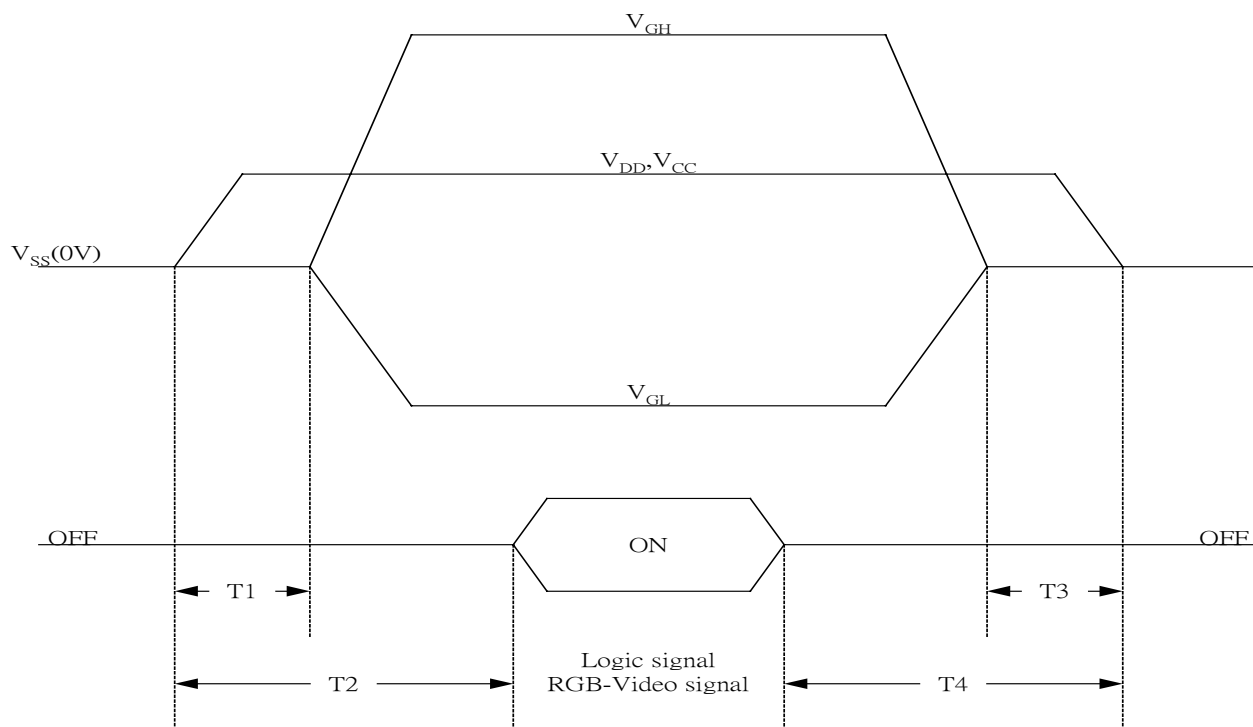


G) External clock mode (CKC = "LOW")



8. Power on Sequence(Voltage source)

The Power on Sequence only effect by V_{CC} , V_{SS} , V_{DD} , V_{GL} and V_{GH} , the others do not care.



$$1) 10\text{ms} \leq T1 < T2$$

$$2) 0\text{ms} < T3 \leq T4 \leq 10\text{ms}$$

9. Optical Characteristics

9-1) Specification

$T_a = 25^\circ\text{C}$

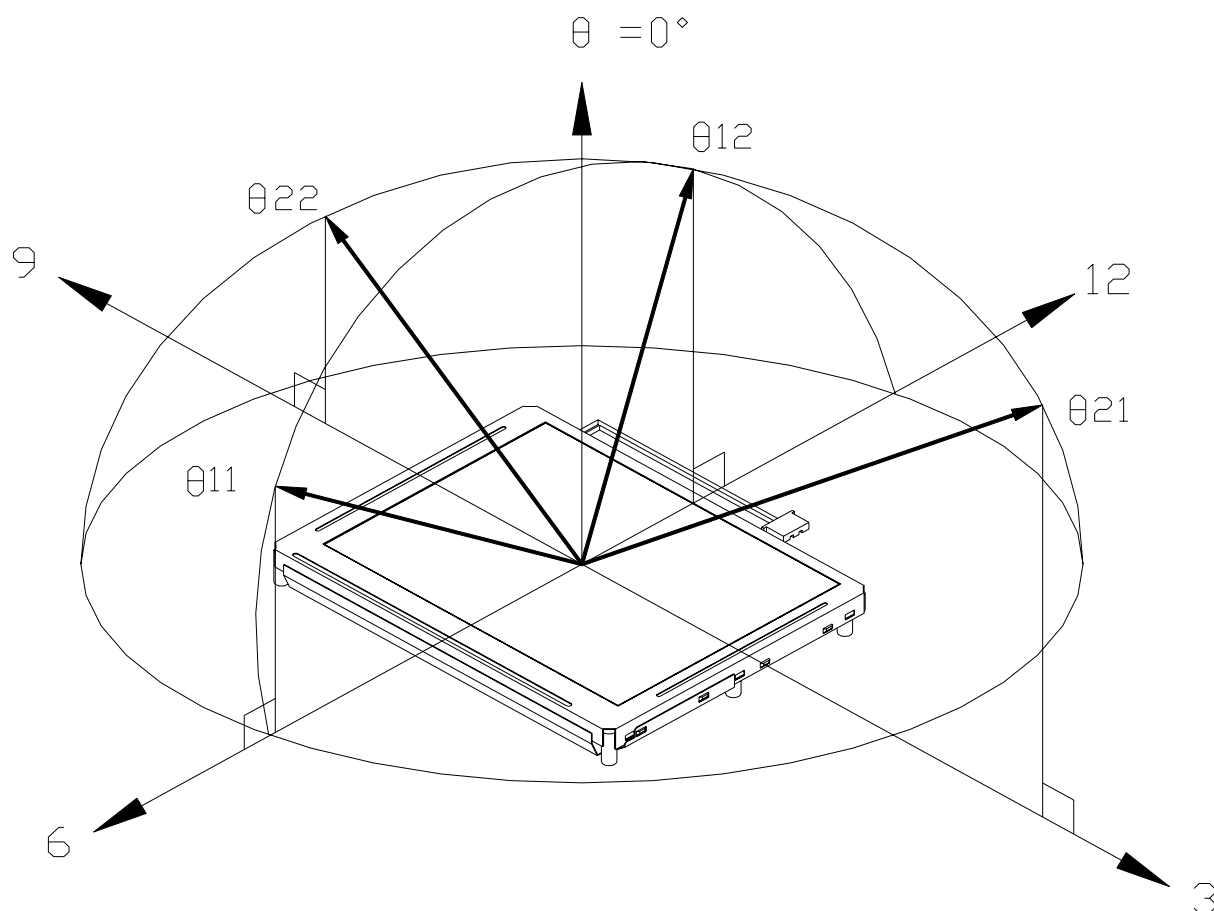
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ_{21}, θ_{22}	$CR \geq 10$	± 55	± 60		deg	Note 9-3
	Vertical	θ_{12} (to 12 o'clock)		35	40		deg	
		θ_{11} (to 6 o'clock)		50	55		deg	
Contrast Ratio		CR	At optimized Viewing angle	110	150			Note 9-1
Response time	Rise	Tr	$\theta = 0^\circ$		15	30	ms	Note 9-4
	Fall	Tf			25	50	ms	
Transmission Ratio		T		9.5	10.0	10.5	%	
Uniformity		U		75	80		%	Note 9-5
Brightness				300	330		cd/m ²	Note 9-2
White Chromaticity		X	$\theta = 0^\circ$	0.270	0.300	0.330		Note 9-2
		Y		0.280	0.310	0.340		
		Tc		6300	7800	9300		
Lamp Life Time		+25°C		10,000			hr	

Note 9-1 : $CR = \frac{\text{Luminance when LCD is White}}{\text{Luminance when LCD is Black}}$

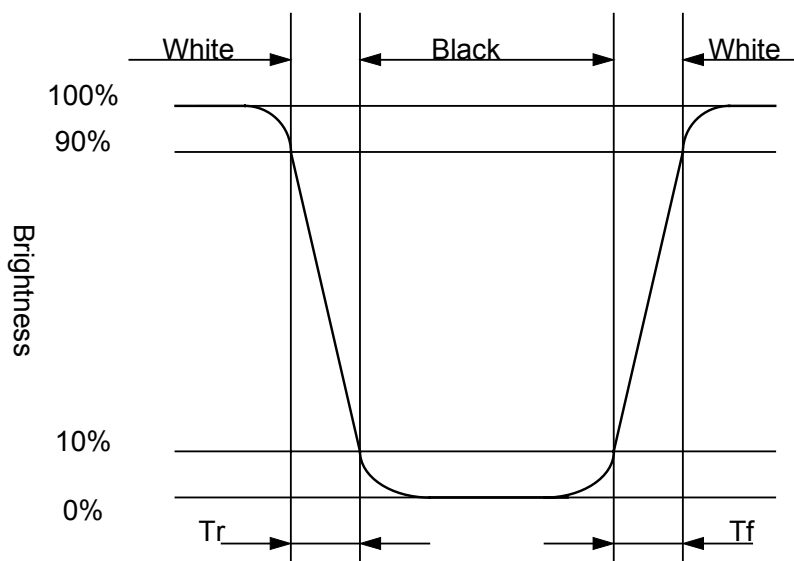
Contrast Ratio is measured in optimum common electrode voltage.
The test configurations of contrast ratio see section 9-2.

Note 9-2 : 1.Topcon BM-7(fast) luminance meter 2.0°field of view is used in the testing (after 20~30 minutes operation).
2.Lamp current : 6 mA
3.Inverter model : TDK-347.

Note 9-3 : The definition of viewing angle diagram



Note 9-4 : The definitions of response time



Note 9-5 : The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

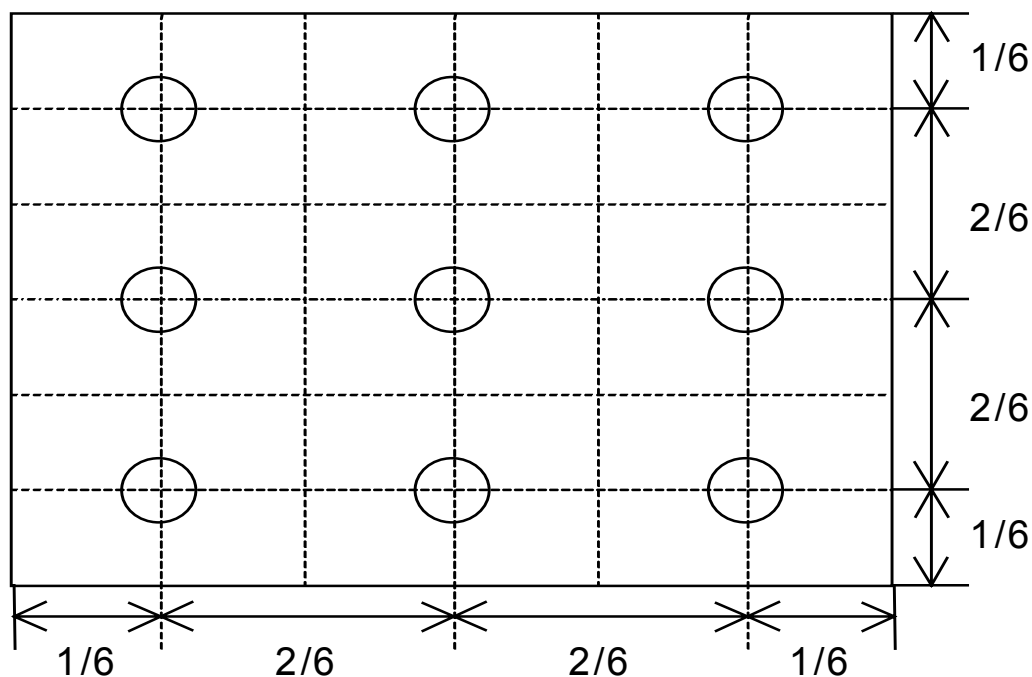
Luminance meter : BM-5A or BM-7 fast (TOPCON)

Measurement distance : 500 mm +/- 50 mm

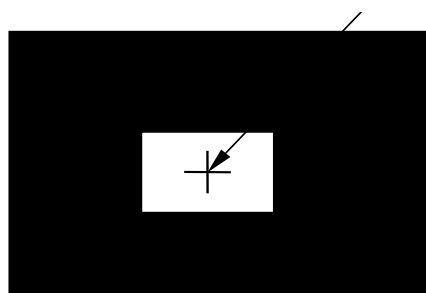
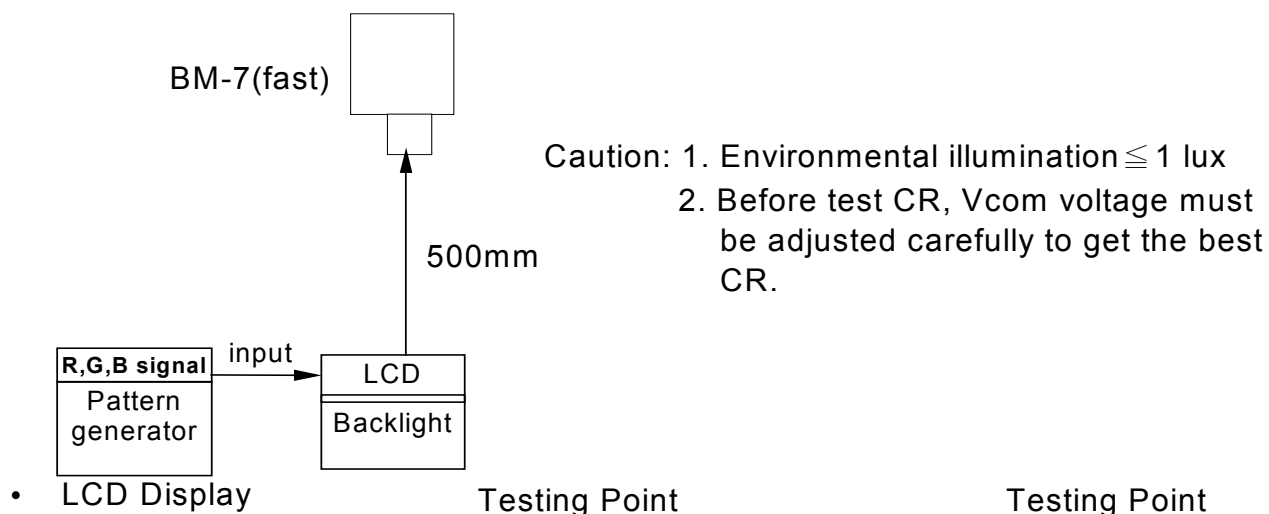
Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

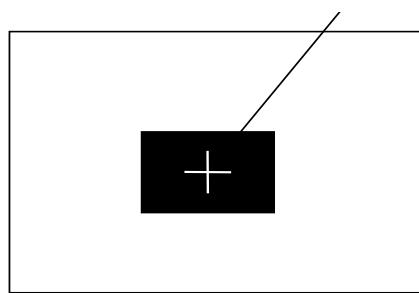
The test pattern is white (Gray Level 63).



9-2) Test Configuration

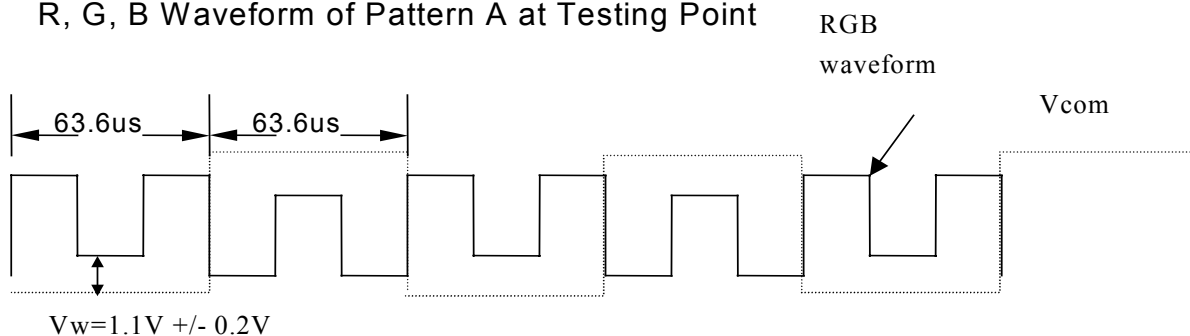


Pattern A

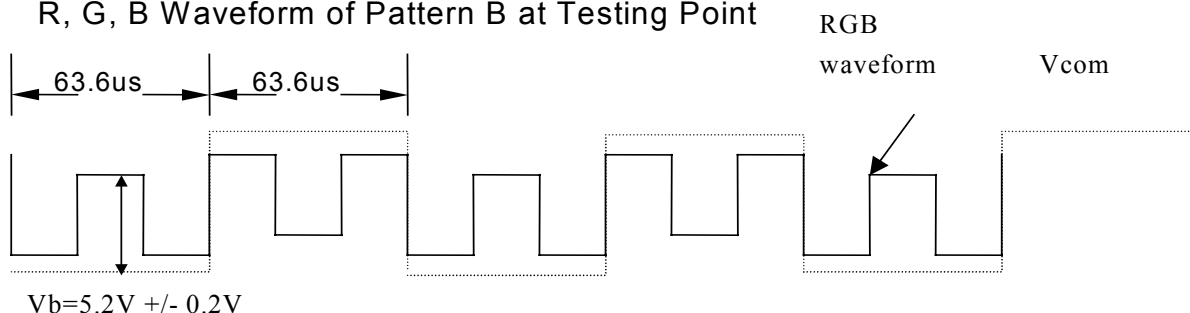


Pattern B

- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



10. Handling Cautions

10-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
 - 1. The noise from the backlight unit will increase.
 - 2. The output from inverter circuit will be unstable.
 - 3. In some cases a part of module will heat.
- c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

10-2) Precautions in mounting

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

10-3) Adjusting module

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

10-4) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many Hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.

10-5) Polarizer mark

The polarizer mark is to describe the direction of wide view angle film how to mach up with the rubbing direction.

11. Reliability

No.	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80°C, 240 hrs
2	Low Temperature Storage Test	Ta = -30°C, 240 hrs
3	High Temperature Operation Test	Ta = +70°C, 240 hrs
4	Low Temperature Operation Test	Ta = -20°C, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60°C, 80%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-25°C → +25°C → +70°C, 200 Cycles 30 min 5min 30 min
7	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz Amplitude : 1.5 mm Sweep time : 11 mins Test Period : 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction: ±X, ±Y, ±Z Cycle: 3 times
9	Electrostatic Discharge Test (non-operating)	150pF, 330Ω Air : ±15KV ; Contact : ±8KV 10 times/point, 9 points/panel face

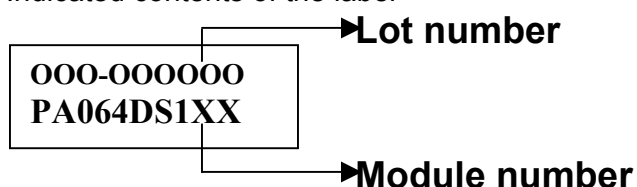
Ta: ambient temperature

[Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

12. Indication of Lot Number Label

a) Indicated contents of the label



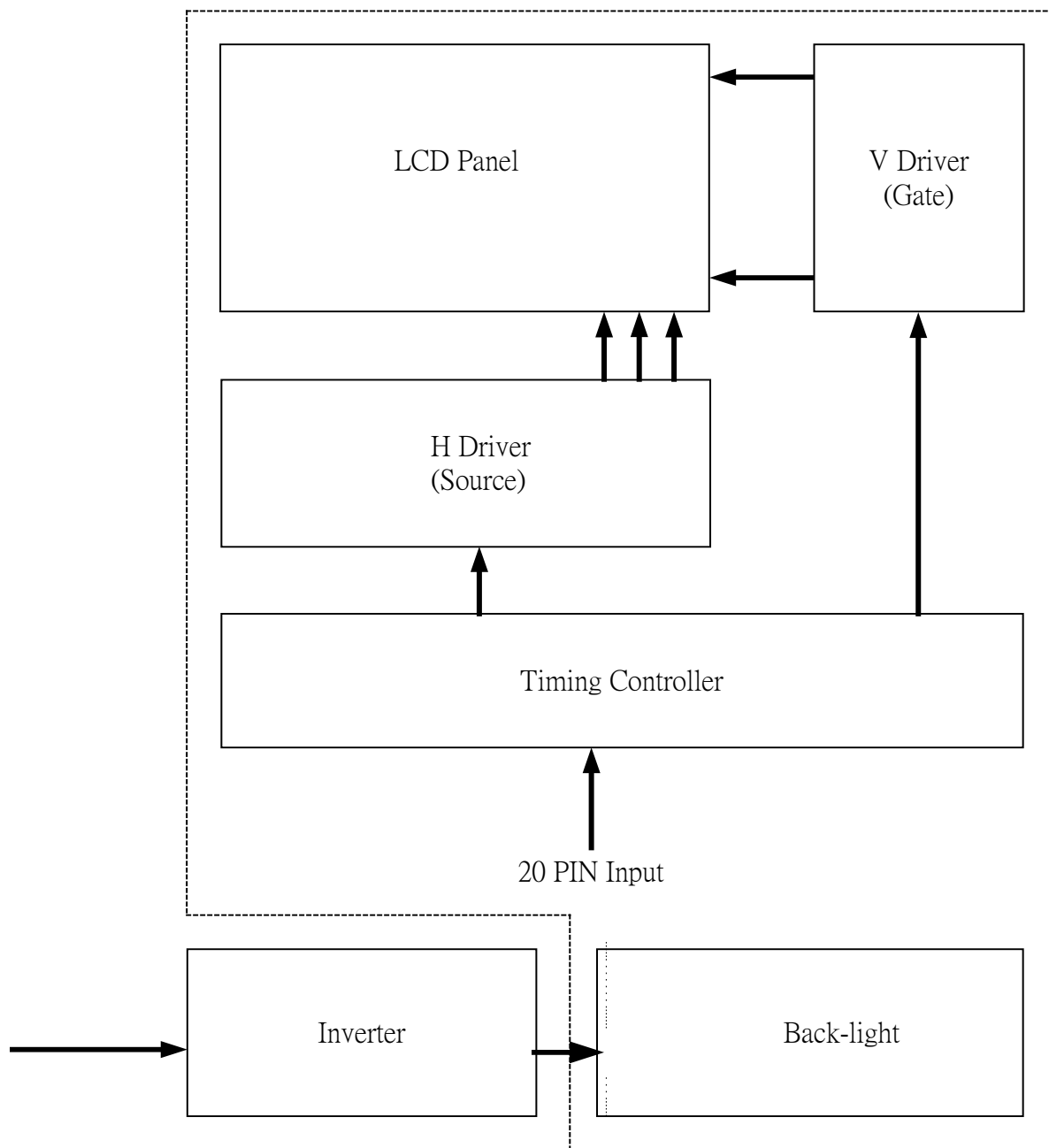
Contents of lot number : SB9—STC OEM product

5th—Production year : 1999⇒9, 2000⇒A, 2001⇒B.....

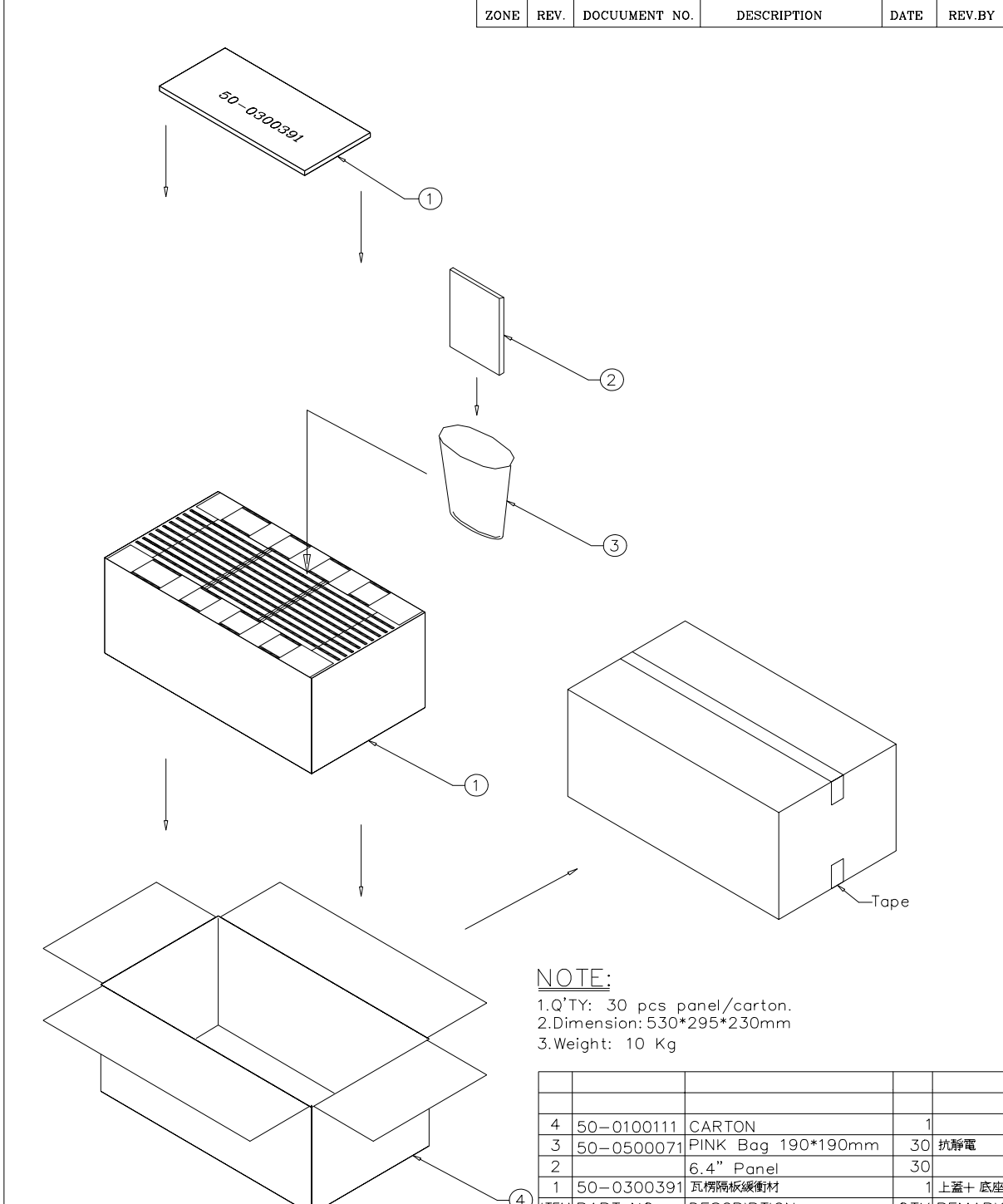
6th—Production month : 1, 2, 3,...,9, A, B, C

7th~10th—Serial numbers : 0001~9999

13. Block Diagram



14. Packing

ZONE	REV.	DOCUMENT NO.	DESCRIPTION	DATE	REV. BY																									
																														
NOTE: 1.Q'TY: 30 pcs panel/carton. 2.Dimension: 530*295*230mm 3.Weight: 10 Kg																														
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th>ITEM</th> <th>PART NO.</th> <th>DESCRIPTION</th> <th>QTY</th> <th>REMARK</th> </tr> <tr> <td>4</td> <td>50-0100111</td> <td>CARTON</td> <td>1</td> <td></td> </tr> <tr> <td>3</td> <td>50-0500071</td> <td>PINK Bag 190*190mm</td> <td>30</td> <td>抗靜電</td> </tr> <tr> <td>2</td> <td></td> <td>6.4" Panel</td> <td>30</td> <td></td> </tr> <tr> <td>1</td> <td>50-0300391</td> <td>瓦楞隔板緩衝材</td> <td>1</td> <td>上蓋+底座</td> </tr> </table>		ITEM	PART NO.	DESCRIPTION	QTY	REMARK	4	50-0100111	CARTON	1		3	50-0500071	PINK Bag 190*190mm	30	抗靜電	2		6.4" Panel	30		1	50-0300391	瓦楞隔板緩衝材	1	上蓋+底座		
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MTL.SPEC.		UNSPECIFIED TOL'S		REMARK																										
		ANGLE																												
		ROUGHNESS																												
APPROVE		SCALE	UNIT	SHEET	DWG.TITLE																									
CHECK				1 OF 1	6.4" Model Packing Draw																									
DRAWN	Jimmy	MTL.NO.	DWG FILE:		REV. 01																									
	'02.10.23				A4 SIZE																									

Revision History

Rev.	Issued Date	Revised Contents
0.1	Sep. 06 , 2002	NEW
1.0	Oct. 29 , 2002	Modify Page 27 : Packing Drawing
1.1	Feb. 27, 2003	Modify Page 8 : Current Consumption (Total consumption changed from 285.53mW to 292.79mW)