DATA SHEET

P87CL881
Low voltage 8-bit microcontroller

Preliminary specification
File under Integrated Circuits, IC20

1997 Dec 12

Philips
Semiconductors

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CONTENTS

1 FEATURES

- Full static 80C51 CPU; enhanced 8-bit architecture with:
  - Minimum 6 cycles per instruction (twice as fast as a standard 80C51 core)
  - Non-page oriented instructions
  - Direct addressing
  - Four 8 byte RAM register banks
  - Stack depth limited only by available internal RAM (maximum 256 bytes)
  - Multiply, divide, subtract and compare instructions.
- Very low current consumption
- Single supply voltage of 1.8 to 3.6 V
- Frequency: 1 MHz to 10 MHz
- Operating temperature: –25 to +70 °C
- 44-pin LQFP package
- Four 8-bit ports (32 I/O lines)
- 63 kbytes OTP program memory
- 256 bytes internal RAM
- 1792 bytes internal AUX-RAM
- External address range: 64 kbytes of ROM and 64 kbytes of RAM
- Amplitude Controlled Oscillator (ACO) suitable for use with a quartz crystal or ceramic resonator
- Improved Power-On/Power-Off Reset circuitry (POR)
- Low Voltage Detection (LVD) with 11 software programmable levels
- 8 interrupts on Port 1, edge or level sensitive triggering selectable via software power-saving use for keyboard control
- Twenty source, twenty vector interrupt structure with two priority levels
- Wake-up from Power-down mode via LVD or external interrupts at Port 1
- Two 16-bit timer/event counters
- Additional 16-bit timer/event counters, with capture, compare and PWM function
- Watchdog Timer
- Full duplex enhanced UART with double buffering
- I^2C-bus interface for serial transfer on two lines, maximum operating frequency 400 kHz.

2 GENERAL DESCRIPTION

The P87CL881 is an 8-bit microcontroller especially suited for pager applications.

The P87CL881 is manufactured in an advanced CMOS technology and is based on single-chip technology.

The device is optimized for low power consumption and has two software selectable features for power reduction: Idle and Power-down modes. In addition, all derivative blocks switch off their clock if they are inactive.

The instruction set of the P87CL881 is based on that of the 8051. The P87CL881 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

This data sheet details the specific properties of the P87CL881; for details of the P87CL881 core and the derivative functions see the *"TELX family"* data sheet and *"8051-Based 8-bit Microcontrollers; Data Handbook IC20"*.

3 ORDERING INFORMATION

TYPE NUMBER(1)	PRODUCT TYPE	PACKAGE		
		NAME	DESCRIPTION	VERSION
P87CL881HDH/000	Blank OTP; note 2	LQFP44	plastic low profile quad flat package; 44 leads; body 10 × 10 × 1.4 mm	SOT389-1
P87CL881HDH/xxx	Pre-programmed OTP			

Notes

1. Please refer to the Order Entry Form (OEF) for this device for the full type number to use when ordering. This type number will also specify the required program and options.
2. No guarantee for OTP retention.

4 BLOCK DIAGRAM

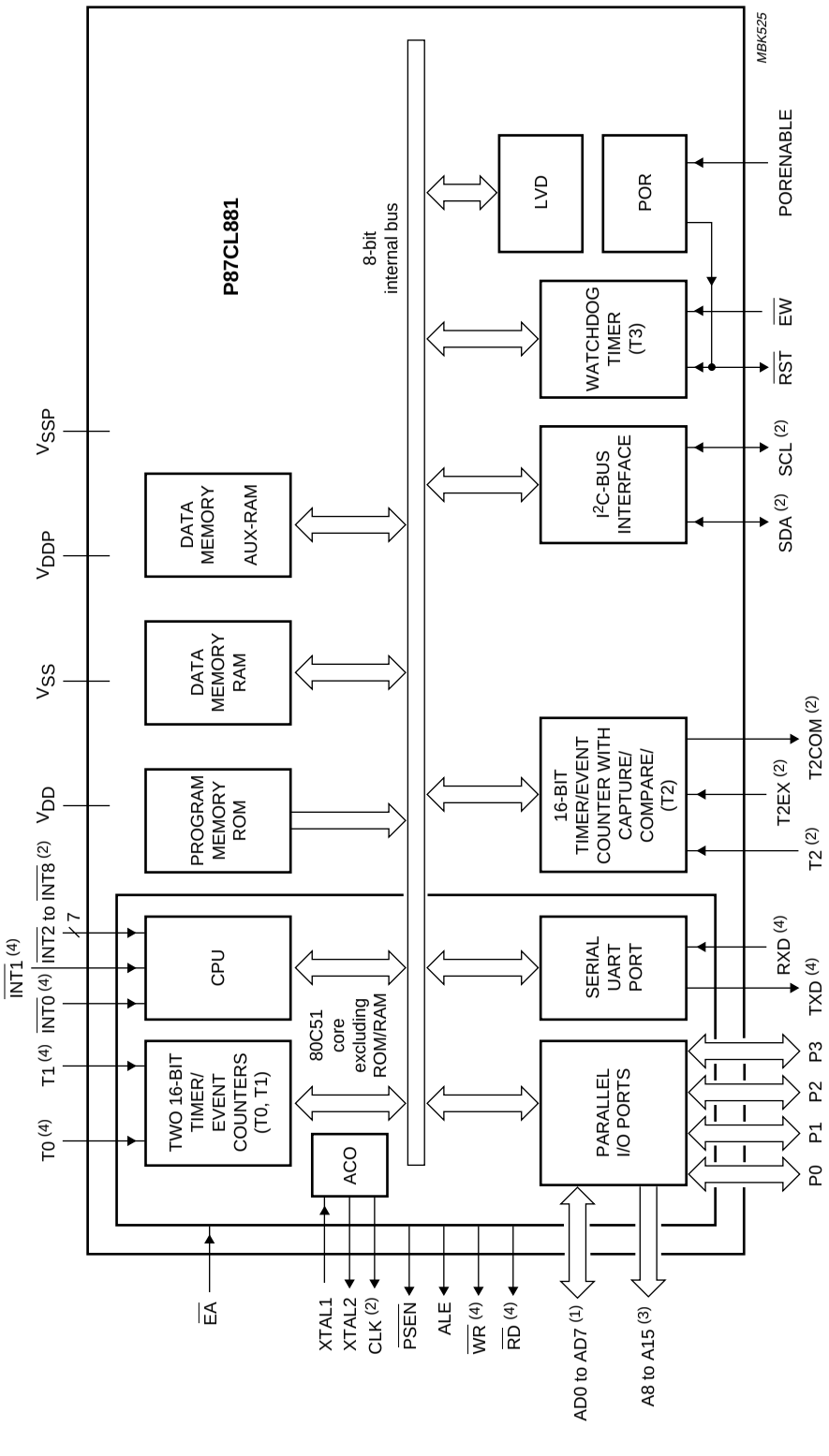


Fig.1 Block diagram.

(1) Alternative function of Port 0.
(2) Alternative function of Port 1.
(3) Alternative function of Port 2.
(4) Alternative function of Port 3.

5 PINNING INFORMATION

5.1 Pinning

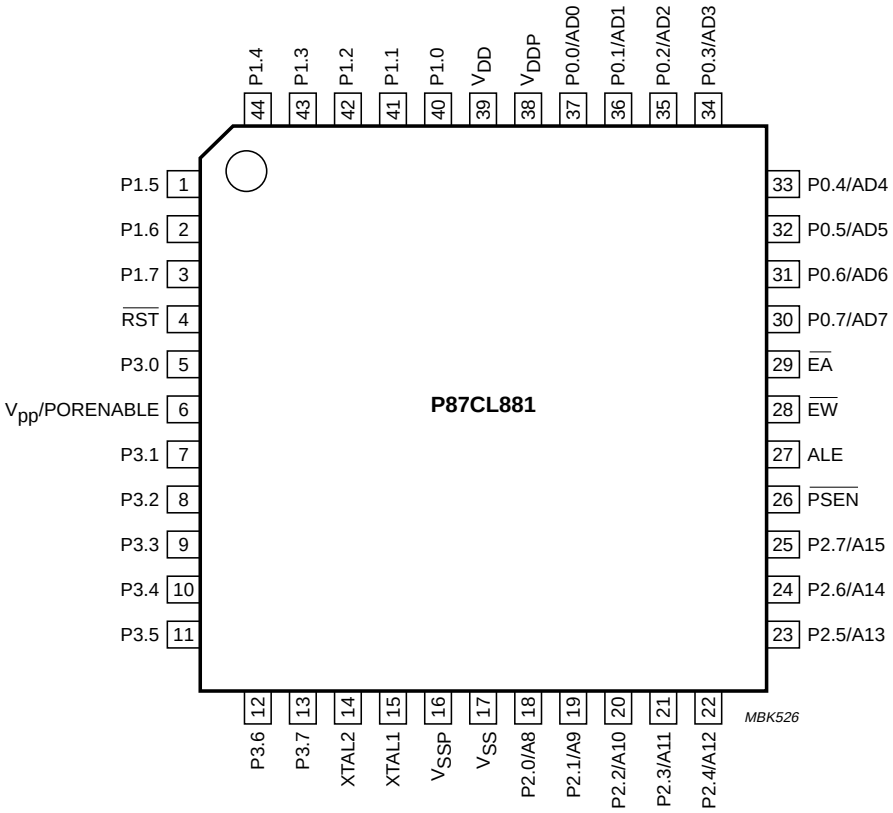


Fig.2 Pin configuration.

5.2 Pin description

Table 1 LQFP package

SYMBOL	PIN	DESCRIPTION
V_{DD}	39	**Power supply** for core.
V_{DDP}	38	**Power supply** for I/O ring.
V_{SS}	17	**Ground** for core.
V_{SSP}	16	**Ground** for I/O ring.
PORENABLE/V_{PP}	6	**PORENABLE.** If set to a logic 1, the internal Power-on-reset circuit is enabled. If external reset circuitry is used, it is recommended to keep PORENABLE LOW in order to achieve the lowest power consumption. This pin is also used for the OTP programming voltage V_{PP}.
$\overline{RST}$	4	**Active Low Reset.** A LOW level on this pin for two machine cycles while the oscillator is running, resets the device. The $\overline{RST}$ pin is also an output which can be used to reset other ICs.
$\overline{EW}$	28	Enable Watchdog Timer.
XTAL2	14	**Crystal output.** Output of the amplitude controlled oscillator. If an external oscillator clock is used this pin not used.
XTAL1	15	**Crystal Input.** Input to the amplitude controlled oscillator. Also the input for an externally generated clock source.
$\overline{PSEN}$	26	**Program Store Enable.** Read strobe to external program memory. When executing code out of external program memory, $\overline{PSEN}$ is activated twice each machine cycle. However, during each access to external data memory two $\overline{PSEN}$ activations are skipped. During Power-down mode the $\overline{PSEN}$ pin stays HIGH.
ALE	27	**Address Latch Enable.** Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods and may be used for external timing or clocking purposes. For improved EMC behaviour, the toggle of the ALE pin can be disabled by setting the RFI bit in the PCON register by software. This bit is cleared on reset and can be set and cleared by software. When set, the ALE pin will be pulled-down internally, switching an external address latch to a quiet state. The MOVX instruction will still toggle ALE if external memory is accessed. ALE will retain its normal HIGH state during Idle mode and a LOW state during the Power-down mode while in the EMC mode. Additionally, during internal access ($\overline{EA}$ = 1) ALE will toggle normally when the address exceeds the internal program memory size. During external access ($\overline{EA}$ = 0) ALE will always toggle normally, whether the RFI bit is set or not.
$\overline{EA}$	29	**External Access.** When $\overline{EA}$ is held HIGH, the CPU executes out of the internal program memory (unless the Program Counter exceeds the highest address for internal program memory). When $\overline{EA}$ is held LOW, the CPU executes out of external program memory regardless of the value of the program counter. The state of the $\overline{EA}$ pin is internally latched at reset.

SYMBOL	PIN	DESCRIPTION
P0.0/AD0	37	**Port 0.** 8-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. AD7 to AD0 provide the multiplexed low-order address and data bus during accesses to external memory.
P0.1/AD1	36	
P0.2/AD2	35	
P0.3/AD3	34	
P0.4/AD4	33	
P0.5/AD5	32	
P0.6/AD6	31	
P0.7/AD7	30	
P1.0/INT2/T2	40	**Port 1.** 8-bit bidirectional I/O port with alternative functions. Every port pin except P1.6 and P1.7 (I^2C-bus pins) can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. Port 1 also serves the alternative functions INT2 to INT9 interrupts, Timer 2 external input and Timer 2 compare output, external clock output CLK and I^2C-bus Clock and I^2C-bus Data in/outputs.
P1.1/INT3/T2EX	41	
P1.2/INT4/ T2COMP	42	
P1.3/INT5	43	
P1.4/INT6/CLK	44	
P1.5/INT7	1	
P1.6/INT8/SCL	2	
P1.7/INT9/SDA	3	
P2.0/A8	18	**Port 2.** 8-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. Port 2 emits the high order address byte during accesses to external memory that use 16-bit addresses (MOVX@DPTR). In this application it uses the strong internal pull-ups when emitting logic 1's. During accesses to external memory that use 8-bit addresses (MOVX@Ri), Port 2 emits the contents of the P2 Special Function Register.
P2.1/A9	19	
P2.2/A10	20	
P2.3/A11	21	
P2.4/A12	22	
P2.5/A13	23	
P2.6/A14	24	
P2.7/A15	25	
P3.0/RXD/data	5	**Port 3.** 8-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. RXD/data is the serial port receiver data input (asynchronous) or data I/O (synchronous). TXD/clock is the serial port transmitter data output (asynchronous) or clock output (synchronous). $\overline{INT0}$ and $\overline{INT1}$ are external interrupt lines. T0 and T1 are external inputs for Timer 0 and Timer 1 respectively. $\overline{WR}$ is the external memory write strobe and $\overline{RD}$ is the external memory read strobe.
P3.1/TXD/clock	7	
P3.2/$\overline{INT0}$	8	
P3.3/$\overline{INT1}$	9	
P3.4/T0	10	
P3.5/T1	11	
P3.6/$\overline{WR}$	12	
P3.7/$\overline{RD}$	13	

6 FUNCTIONAL DESCRIPTION

For the functional and block descriptions of the P87CL881, refer to the *"TELX family"* data sheet.

6.1 Special Function Registers

Table 2 Special Function Registers memory map and reset values; note 1

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE(2)
80C51 core			
Accumulator	ACC	E0H	0000 0000
B Register	B	F0H	0000 0000
Data Pointer Low byte	DPL	82H	0000 0000
Data Pointer High byte	DPH	83H	0000 0000
Program Counter High byte	PCH	no SFR	0000 0000
Program Counter Low byte	PCL	no SFR	0000 0000
Power Control Register	PCON	87H	0000 0000
Prescaler Register	PRESC	F3H	0000 0000
Program Status Word	PSW	D0H	0000 0000
Stack Pointer	SP	81H	0000 0111
XRAM Page Register	XRAMP	FAH	XXXX X000
Timer 0 and Timer 1			
Timer/Counter Control Register	TCON	88H	0000 0000
Timer/Counter 0 High byte	TH0	8CH	0000 0000
Timer/Counter 1 High byte	TH1	8DH	0000 0000
Timer/Counter 0 Low byte	TL0	8AH	0000 0000
Timer/Counter 1 Low byte	TL1	8BH	0000 0000
Timer/Counter Mode Control Register	TMOD	89H	0000 0000
Ports			
Alternative Port Function Control Register	ALTP	A3H	0000 0000
Port P0 output data Register	P0	80H	1111 1111
Port P0 Configuration A Register	P0CFGA	8EH	1111 1111
Port P0 Configuration B Register	P0CFGB	8FH	0000 0000
Port P1 output data Register	P1	90H	0111 1111
Port P1 Configuration A Register	P1CFGA	9EH	0000 1000
Port P1 Configuration B Register	P1CFGB	9FH	0111 1111
Port P2 output data Register	P2	A0H	1111 1111
Port P2 Configuration A Register	P2CFGA	AEH	1111 1111
Port P2 Configuration B Register	P2CFGB	AFH	0000 0000
Port P3 output data Register	P3	B0H	1111 1111
Port P3 Configuration A Register	P3CFGA	BEH	1111 1110
Port P3 Configuration B Register	P3CFGB	BFH	1111 1111

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE(2)
Timer 2			
Timer 2 Compare High byte	COMP2H	ABH	0000 0000
Timer 2 Compare Low byte	COMP2L	AAH	0000 0000
Timer 2 Reload/Capture High byte	RCAP2H	CBH	0000 0000
Timer 2 Reload/Capture Low byte	RCAP2L	CAH	0000 0000
Timer/Counter 2 Control Register	T2CON	C8H	0000 0000
Timer/Counter 2 High byte	TH2	CDH	0000 0000
Timer/Counter 2 Low byte	TL2	CCH	0000 0000
Interrupt logic			
Interrupt Enable Register 0	IEN0	A8H	0000 0000
Interrupt Enable Register 1	IEN1	E8H	0000 0000
Interrupt Enable Register 2	IEN2	F1H	0000 0000
Interrupt Priority Register 0	IP0	B8H	0000 0000
Interrupt Priority Register 1	IP1	F8H	0000 0000
Interrupt Priority Register 2	IP2	F9H	0000 0000
Interrupt Sensitivity Register 1	ISE1	E1H	0000 0000
Interrupt Polarity Register	IX1	E9H	0000 0000
Interrupt Request Flag Register 1	IRQ1	C0H	0000 0000
Low Voltage Detection			
LVD Control Register	LVDCON	F2H	0000 0000
PORACO			
Reset Status Register	RSTAT	E6H	XXX0 0000
UART			
Serial Port Buffer	S0BUF	99H	0000 0000
Serial Port Control Register	S0CON	98H	0000 0000
I^2C-bus interface			
Address Register	S1ADR	DBH	0000 0000
Serial Control Register	S1CON	D8H	0000 0000
Data Shift Register	S1DAT	DAH	0000 0000
Serial Status Register	S1STA	D9H	1111 1000
Watchdog Timer			
Watchdog Timer Control Register	WDCON	A5H	1010 0101
Watchdog Timer Interval Register	WDTIM	FFH	0000 0000

Notes

1. E7H and FDH are reserved locations and must not be written to.
2. X = undefined state.

6.2 I/O facilities

6.2.1 PORTS

The P87CL881 has 32 I/O lines treated as 32 individually addressable bits or as four parallel 8-bit addressable ports. Ports 0, 1, 2 and 3 perform the following alternative functions:

Port 0 Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.

Port 1 Used for a number of special functions:

- P1.0 to P1.7 provides the inputs for the external interrupts INT2 to INT9
- P1.0/T2 and P1.1/T2EX for external inputs of Timer 2
- P1.2/T2COMP for External activation and compare output of Timer 2
- P1.4/CLK for the clock output
- P1.6/SCL and P1.7/SDA for the I^2C-bus interface are real open-drain outputs or high-impedance; no other port configurations are available.

Port 2 Provides the high-order address bus when expanding the device with external program memory and/or external data memory.

Port 3 Pins can be configured individually to provide:

- P3.0/RXD/data and P3.1/TXD/clock are serial port receiver input and transmitter output (UART)
- P3.2/$\overline{INT0}$ and P3.3/$\overline{INT1}$ are external interrupt request inputs
- P3.4/T0 and P3.5/T1 as counter inputs
- P3.6/$\overline{WR}$ and P3.7/$\overline{RD}$ are control signals to write and read to external memories.

To enable a port pin alternative function, the port bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and input buffer. All ports have internal pull-ups. Figure 3(a) shows that the strong transistor p1 is turned on for only 1 oscillator periods after a LOW-to-HIGH transition in the port latch. When on, it turns on p3 (a weak pull-up) through the inverter IN1. This inverter and transistor p3 form a latch which holds the logic 1.

6.2.2 PORT I/O CONFIGURATION

I/O port output configurations are determined by the settings in the port configuration SFRs. Each port has two associated SFRs: PnCFGA and PnCFGB, where 'n' indicates the specific port number (0 to 3). One bit in each of the 2 SFRs relates to the output setting for the corresponding port pin, allowing any combination of the 2 output types to be mixed on those port pins.
For example, the output type of Port 1 pin 3 is controlled by setting bit 3 in the SFRs P1CFGA and P1CFGB.

The port pins may be individually configured via the SFRs with one of the following modes (P1.6 and P1.7 can be open-drain or high-impedance but never have any diodes against V_{DD}).

Mode 0 Open-drain; quasi-bidirectional I/O with n-channel open-drain output. Use as an output (e.g. Port 0 for external memory accesses ($\overline{EA}$ = 0) or access above the built-in memory boundary) requires the connection of an external pull-up resistor. The ESD protection diodes against V_{DD} and V_{SS} are still present. Except for the I^2C-bus pins P1.6 and P1.7, ports which are configured as open-drain still have a protection diode to V_{DD}. See Fig.3(a).

Mode 1 Standard port; quasi-bidirectional I/O with pull-up. The strong pull-up p1 is turned on for only two oscillator periods after a LOW-to-HIGH transition in the port latch. After these two oscillator periods the port is only weakly driven through p2 and 'very weakly' driven through p3. See Fig.3(b).

Mode 2 High-impedance; this mode turns all port output drivers off. Thus, the pin will not source or sink current and may be used as an input-only pin with no internal drivers for an external device to overcome. See Fig.3(c).

Mode 3 Push-pull; output with drive capability in both polarities. In this mode, pins can only be used as outputs. See Fig.3(d).

Tables 3 and 4 show the configuration register settings for the four output configurations. The electrical characteristics of each output configuration are specified in Chapter 8. The default port configuration after reset is given in Table 4.

Table 3 Port Configuration Register settings

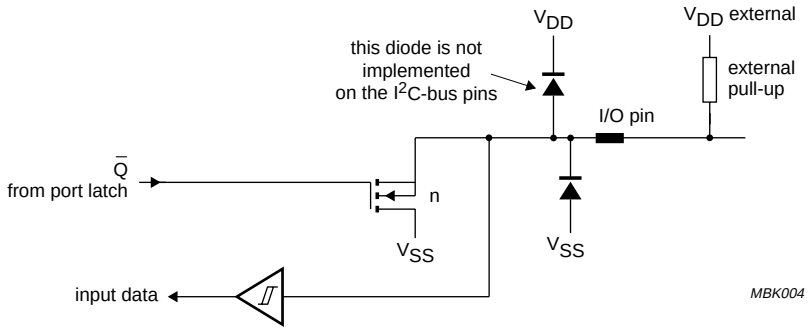
MODE(1)	PnCFGA	PnCFGB	PORT OUTPUT CONFIGURATION	
			NORMAL PORTS	I^2C-BUS PORTS (P1.6 AND P1.7)
0	0	0	open-drain	open-drain
1	1	0	quasi-bidirectional	open-drain
2	0	1	high-impedance	high-impedance
3	1	1	push-pull	open-drain

Note

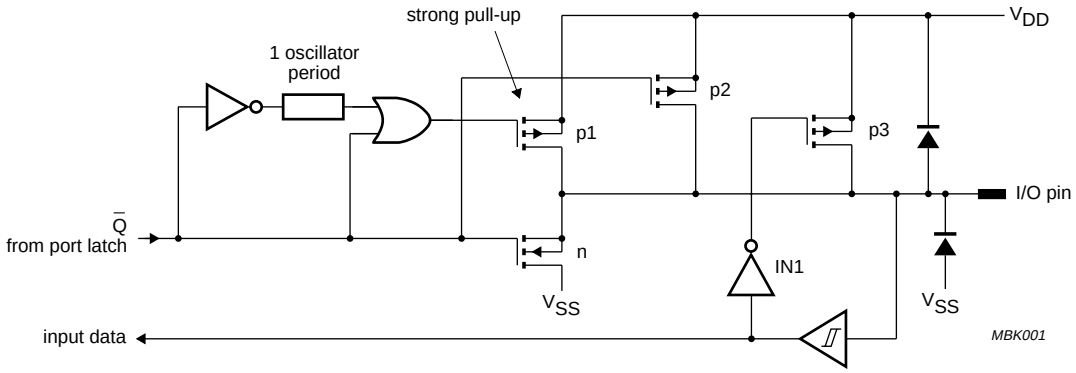
1. Mode changes may cause glitches to occur during transitions. When modifying both registers, WRITE instructions should be carried out consecutively.

Table 4 Special Function Registers for Port configurations/data

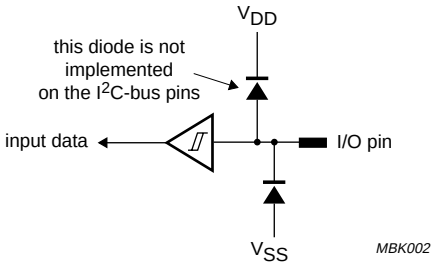
REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS (HEX)	STATE AFTER RESET
Port P0 Configuration A Register	P0CFGA	8E	1111 1111
Port P0 Configuration B Register	P0CFGB	8F	0000 0000
Port P0 output data Register	P0	80	1111 1111
Port P1 Configuration A Register	P1CFGA	9E	0000 1000
Port P1 Configuration B Register	P1CFGB	9F	0111 1111
Port P1 output data Register	P1	90	0111 1111
Port P2 Configuration A Register	P2CFGA	AE	1111 1111
Port P2 Configuration B Register	P2CFGB	AF	0000 0000
Port P2 output data Register	P2	A0	1111 1111
Port P3 Configuration A Register	P3CFGA	BE	1111 1110
Port P3 Configuration B Register	P3CFGB	BF	1111 1111
Port P3 output data Register	P3	B0	1111 1111



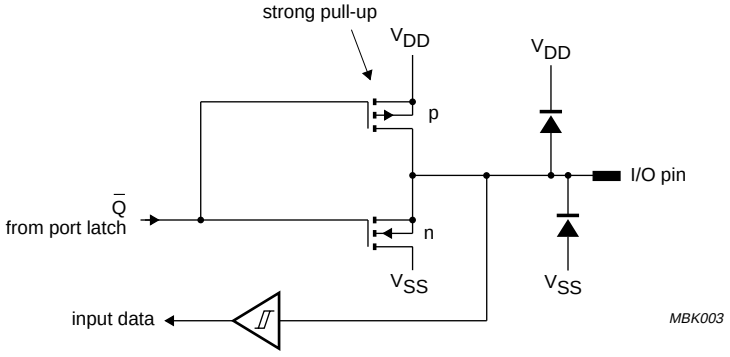
a. Open-drain.



b. Standard/quasi-bidirectional.



c. High-impedance.



d. Push-pull.

Fig.3 Port configuration options.

6.3 Internal Data Memory

The internal data memory is divided into three physically separated parts:

256 bytes of RAM, 128 bytes of Special Function Registers and 1792 bytes of AUX-RAM. These can be addressed each in a different way (see also Table 5).

1. RAM 0 to 127 can be addressed directly and indirectly as in the 80C51. Address pointers are R0 and R1 of the selected register bank.
2. RAM 128 to 255 can only be addressed indirectly. Address pointers are R0 and R1 of the selected register bank.
3. AUX-RAM 0 to 1791 is indirectly addressable via page register (XRAMP) and MOVX-Ri instructions, unless it is disabled by setting ARD = 1.
   AUX-RAM 0 to 1791 is also indirectly addressable as external data memory via MOVX-Data pointer instruction, unless it is disable by setting ARD = 1.
   When executing from internal program memory, an access to AUX-RAM 0 to 1791 when ARD = 0 will not affect the ports P0, P2, P3.6 and P3.7.

An access to external data memory locations higher than 1791 will be performed with the MOVX @ DPTR instructions in the same way as in the 80C51 structure, so with P0 and P2 as data/address bus and P3.6 and P3.7 as write and read timing signals. Note that the external data memory cannot be accessed with R0 and R1 as address pointer if the AUX-RAM is enabled (ARD = 0, default after reset).

The Special Function Registers (SFR) can only be addressed directly in the address range from 128 to 255.

Four register banks, each 8 registers wide, occupy locations 0 through 31 in the lower RAM area. Only one of these banks may be enabled at a time. The next 16 bytes, locations 32 through 47, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal 256 bytes RAM. The stack depth is only limited by the available internal RAM space of 256 bytes (see Fig.4).

Table 5 Internal Data Memory Map

LOCATION	ADDRESS	ADDRESSING
RAM	0 to 127	Direct and indirect
AUX-RAM	0 to 1791	Indirect only with MOVX
RAM	128 to 255	Indirect only
SFR	128 to 255	Direct only

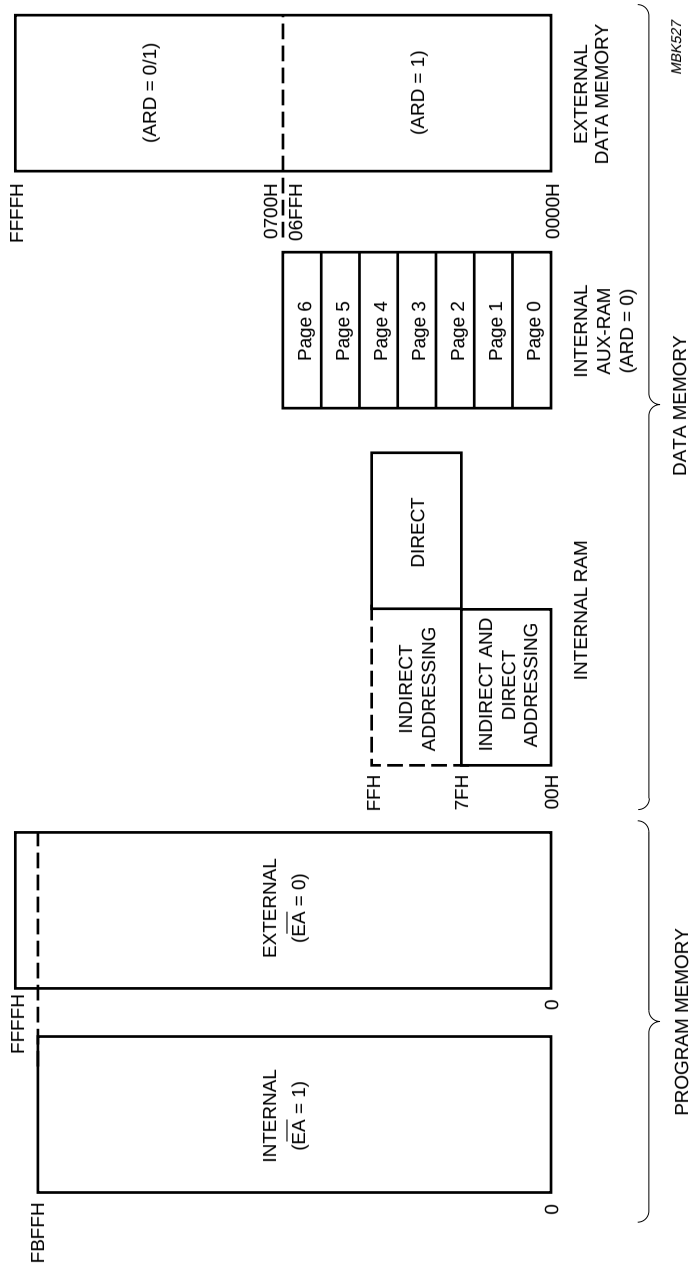


Fig.4 Memory map.

6.3.1 AUX-RAM PAGE REGISTER (XRAMP)

The AUX-RAM Page Register is used to select one of the seven 256 byte pages of the internal 1792 bytes AUX-RAM for MOVX-accesses via RO or R1. Its reset value is XXXX X000 (AUX-RAM page 0).

Table 6 AUX-RAM Page Register XRAMP (SFR address FAH)

7	6	5	4	3	2	1	0
–––––					XRAMP2	XRAMP1	XRAMP0

Table 7 Description of XRAMP bits

BIT	SYMBOL	FUNCTION
XRAMP.7 to XRAMP.3	–	Reserved, undefined during read, a write operation must write “0” to these locations.
XRAMP.2	XRAMP2	AUX-RAM page select bit 2
XRAMP.1	XRAMP1	AUX-RAM page select bit 1
XRAMP.0	XRAMP0	AUX-RAM page select bit 0

Table 8 Memory Locations for all possible MOVX accesses

ARD(1)	XRAMP2	XRAMP1	XRAMP0	INSTRUCTION TYPE	ACCESS
0000				MOVX @ Ri,A and MOVX @ A,Ri	AUX-RAM page 0 (address 0 to 255)
0001				MOVX @ Ri,A and MOVX @ A,Ri	AUX-RAM page 1 (address 256 to 511)
0010				MOVX @ Ri,A and MOVX @ A,Ri	AUX-RAM page 2 (address 512 to 767)
0011				MOVX @ Ri,A and MOVX @ A,Ri	AUX-RAM page 3 (address 768to 1023)
0100				MOVX @ Ri,A and MOVX @ A,Ri	AUX-RAM page 4 (address 1024 to 1279)
0101				MOVX @ Ri,A and MOVX @ A,Ri	AUX-RAM page 5 (address 1280 to 1535)
0110				MOVX @ Ri,A and MOVX @ A,Ri	AUX-RAM page 6 (address 1536 to 1791)
0111				MOVX @ Ri,A and MOVX @ A,Ri	No valid memory access
1	X	X	X	MOVX @ Ri,A and MOVX @ A,Ri	External RAM locations 0 to 255
0	X	X	X	MOVX @ DPTR,A and MOVX A,DPTR	AUX-RAM locations 0 to 1791 External RAM locations 1792 to 65535
1	X	X	X	MOVX @ DPTR,A and MOVX A,DPTR	External RAM locations 0 to 65535

Note

1. ARD (AUXRAM Disable) is a bit in the Special Function Register PCON.

6.4 OTP programming

6.4.1 OTP programming

The 63Kbyte One Time Programmable memory can be programmed by using a OM4260 programmer together with a programmer adapter OM5510. Since the memory is programmable only once, programming an already programmed address results in a logical AND of the old and new code. The OTP code can be read out by the programmer for verification.

6.4.1.1 SIGNATURE BYTES

The OTP memory contains three signature bytes which can be read by the programmer to identify the device. A special address space has been used for these bytes which does not influence the user address space. The values of the signature bytes are:

(030H) = 15H, indicates manufactured by Philips Semiconductors

(031H) = D6H, indicates P87CL881

(060H) = 00H, currently not used.

6.4.1.2 Security

The following protection features are available to protect P87CL881 applications against software piracy and unwanted access to data stored in the application.

1. Preventing programming of an already programmed OTP.
2. Preventing the reading of program code in OTP by disabling access of the programmer to the program memory. In this mode signature and security level verification is still possible.
3. This level has the same functionality as level 2.

Table 9 describes how these protections can be reached by programming the two least significant bits.

Table 9 Security bits and levels of protection

BITS	LEVEL	DESCRIPTION
UUU	0	0, no security
UUP	1	1 is activated
UPP	2	1 and 2 are activated
PPP	3	1, 2 and 3 are activated

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+4.0	V
V_I	input voltage on any pin with respect to ground (V_{SS})	–0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	800	mW
T_{stg}	storage temperature	–65	+150	°C

8 DC CHARACTERISTICS

V_{DD} = 1.8 to 3.6 V; V_{SS} = 0 V; f_{xtal} = 1 to 10 MHz; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS/REMARKS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	Operating;		1.8	–	3.6	V
	RAM data retention in power-down mode		1.0	–	3.6	V
V_{pp}	OTP programming voltage		12.5	–	13.0	V
I_{DD}	supply current operating	V_{DD} =3V ; f_{xtal} = 7 MHz; note 1	––		tbf.	mA
		V_{DD} =3V ; T_{amb} =2 5 °C; note 1	–	tbf.	–	mA
$I_{DD(ID)}$	supply current Idle mode	V_{DD} =3V ; f_{xtal} = 7 MHz; note 2	––		tbf.	mA
		V_{DD} =3V ; T_{amb} =2 5 °C; note 2	–	tbf.	–	mA
$I_{DD(PD)}$	supply current power-down mode	V_{DD} =3V ; T_{amb} =2 5 °C; note 3				
		POR and LVD enabled	–	25		µA
		POR and LVD disabled	–	100	–	nA
$I_{DD(block)}$	supply current per block:	V_{DD} =3V ; T_{amb} =2 5 °C; notes 4 and 5				
	Watchdog		–	110	–µ	A
	I^2C		–	90	–µ	A
	UART		–	90	–µ	A
	Timer T2		–	90	–µ	A
	Timer T0 or T1		–	5	–µ	A
Inputs (Ports, $\overline{RST}$, PORENABLE**)**						
V_{IL}	LOW-level input voltage	notes 6 and 7	0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	note 6	$0.8V_{DD}$	–	V_{DD}	V
$\lvert I_{IL} \rvert$	LOW-level input current (ports in Mode 1)	V_{IN} = 0.4 V; note 8	–	10	50	µA
$\lvert I_{IL(T)} \rvert$	LOW-level input current; HIGH-to-LOW transition (ports in Mode 1)	$V_{IN} = 0.2V_{DD}$; note 8	–	200	1000	µA
$\lvert I_{ILEAK} \rvert$	input leakage current (ports in Mode 0 or 2)	$V_{SS} \leq V_I \leq V_{DD}$	––		1	µA

SYMBOL	PARAMETER	CONDITIONS/REMARKS	MIN.	TYP.	MAX.	UNIT
Outputs (Ports, $\overline{RST}$)						
I_{OL}	LOW-level output current; except SDA and SCL	V_{OL} = 0.4 V	2	–	–	mA
I_{OL2}	LOW-level output current; SDA and SCL	V_{OL} = 0.4 V; note 9	3	—		mA
I_{OH}	HIGH-level output current except (push-pull options only)	V_{OH} =V_{DD} – 0.4 V	2	—		mA
$I_{\overline{RST}}$	$\overline{RST}$ pull-up current source	V_{DD} = 3 V; V_{OH} = V_{DD} – 0.4 V	tbf.	tbf.	–	µA
		V_{DD} = 3 V; V_{OH} = V_{SS}	–	tbf.	tbf.	µA
POR (Power-On-Reset). For the LVD (Low Voltage Detection), see note 10						
VPORH	Trip level HIGH	(Option 5 in *"TELX Family"* specification)	2.13	2.37	2.61	V
VPORL	Trip level LOW	(Option B in *"TELX Family"* specification)	–	1.30	–	V
ACO (Amplitude Controlled Oscillator)						
V_{XTAL1}	external clock signal amplitude (peak-to-peak value)		500	–	V_{DD}	mV
r_{fb}	input impedance on XTAL1		300	1000	–	kΩ
C_{1i}; C_{2i}	input capacitance on XTAL1 and XTAL2	notes 5 and 11	–	10	–	pF

Notes

1. The operating supply current is measured with all output pins disconnected; V_{IL} = V_{SS}; V_{IH} = V_{DD}; $\overline{RST}$ = V_{DD}; XTAL1 driven with square wave; XTAL2 not connected; fetch of NOP instructions; all derivative blocks disabled.
2. The Idle mode supply current is measured with all output pins and $\overline{RST}$ disconnected; V_{IL} = V_{SS}; V_{IH} = V_{DD}; XTAL1 driven with square wave; XTAL2 not connected; all derivative blocks disabled.
3. The Power-down current is measured with all output pins and $\overline{RST}$ disconnected; V_{IL} = V_{SS}; V_{IH} = V_{DD}; XTAL1 and XTAL2 not connected.
4. The typical currents are only for the specific block. To calculate the typical power consumption of the microcontroller, the current consumption of the CPU must be added.
   Example: The typical current consumption of the microcontroller in operating mode with CPU, Watchdog and UART active can be calculated as (1 + 0.110 + 0.09) mA = 1.2 mA at 3 V.
5. Verified on sampling basis.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I^2C-bus specification. Therefore, an input voltage below 0.3V_{DD} will be recognized as a logic 0 and an input voltage above 0.7V_{DD} will be recognized as a logic 1.
7. For pin PORENABLE the V_{IL} max is 0.1V_{DD}.
8. Not valid for pins SDA, SCL, $\overline{RST}$ and PORENABLE.
9. The maximum allowed load capacitance C_L is in this case limited to around 200 pF.
10. The LVD is tested according to the specification in the TELX Family specification, *"chapter Low Voltage Detection*".
11. C1i / C2i are the total internal capacitances (including gate capacitance, leadframe capacitance).

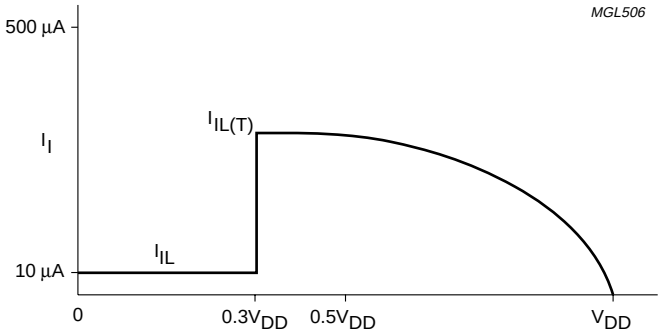
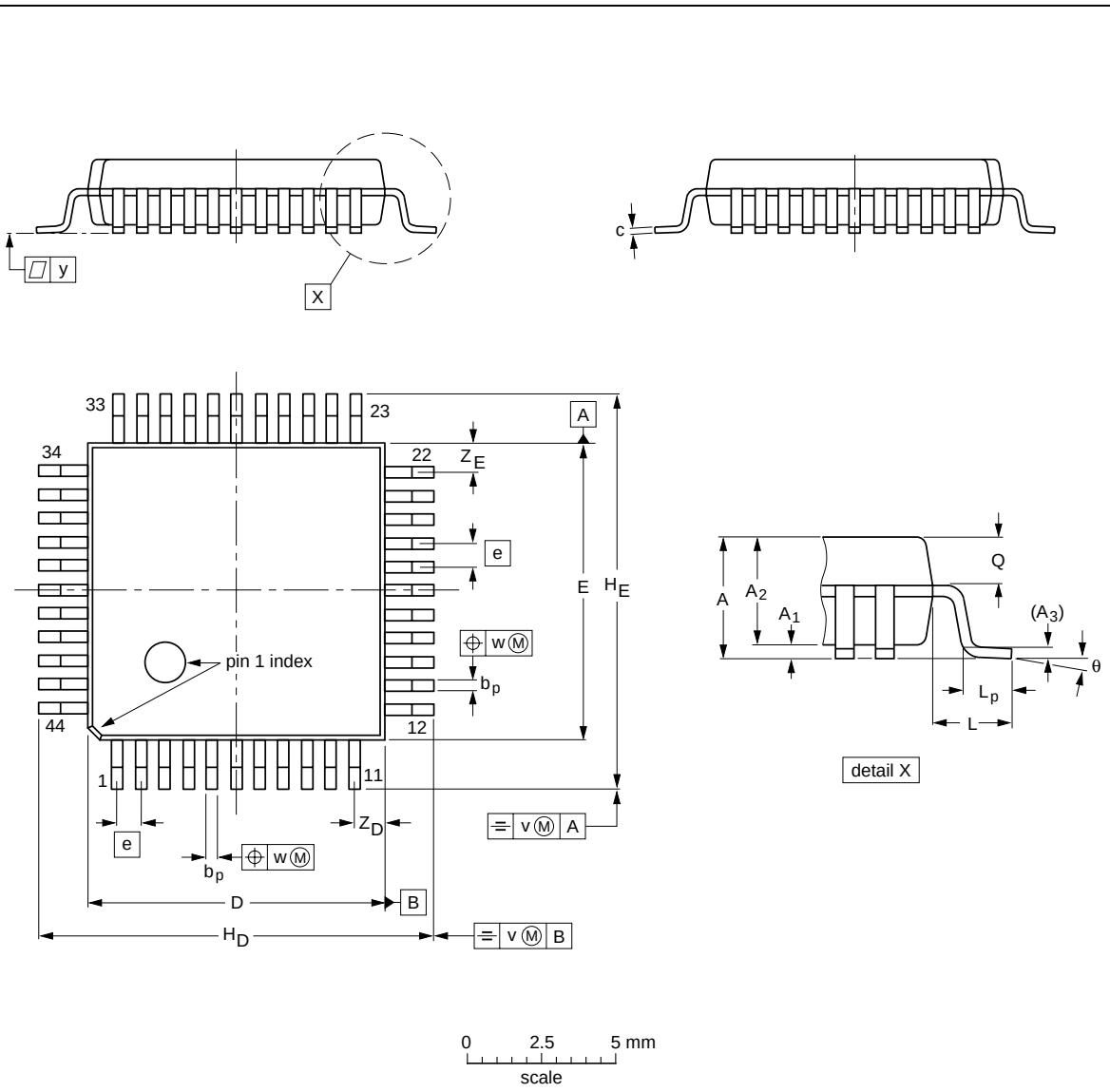


Fig.5 Input current.

9 PACKAGE OUTLINE

LQFP44: plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm **SOT389-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	cE	$D^{(1)}$	$^{(1)}$	eH	H_D	E	LL	p	QZ	v	w	y	$Z_D^{(1)}$	$E^{(1)}$	θ
mm	1.60	0.15 0.05	1.45 1.35	0.25	0.45 0.30	0.20 0.12	10.10 9.90	10.10 9.90	0.80	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.70 0.57	0.20	0.20	0.10	1.14 0.85	1.14 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT389-1						95-12-19

10 SOLDERING

10.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

10.2 Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

10.3 Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all LQFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for LQFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45 to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

10.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

11 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

12 LIFE SUPPORT APPLICATIONS

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Printed in The Netherlands 457047/00/01/pp24 Date of release: 1997 Dec 12 Document order number: 9397 750 03156

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