M8214
PRIORITY INTERRUPT CONTROL UNIT
Military

- **Not Recommended for New Designs**
- **8 Priority Levels**
- **Fully Expandable**
- **Current Status Register**
- **Priority Comparator**
- **24-Pin Dual-In-Line Package**
- **Military Temperature Range: −55°C to +125°C (T_C)**
- **±10% Power Supply Tolerance**

The Intel M8214 is an 8-level priority interrupt control unit (PICU) designed to simplify interrupt-driven microcomputer systems.

The PICU can accept 8 requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue and interrupt to the system along with vector information to identify the service routine.

The M8214 is fully expandable by the use of open collector interrupt output vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt-driven microcomputer systems.

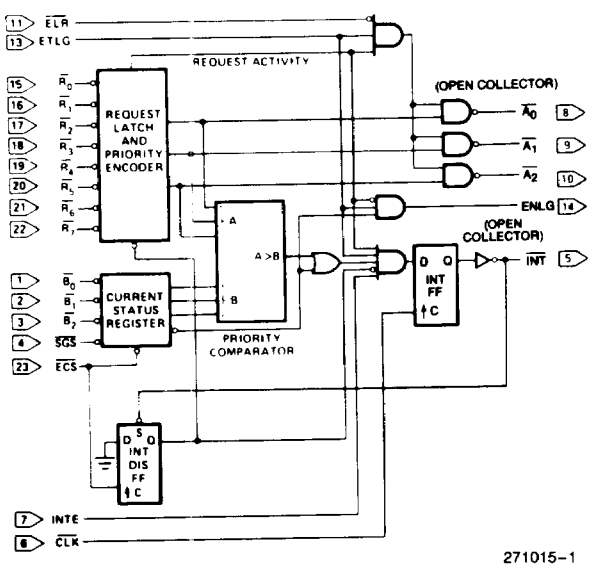
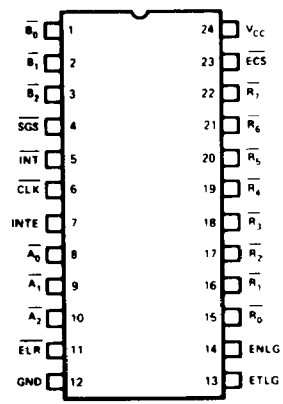


Figure 1. Logic Diagram



INPUTS	
$\overline{R_0}$-$\overline{R_7}$	Request Levels (R_7 Highest Priority)
$\overline{B_0}$-$\overline{B_2}$	Current Status
$\overline{SGS}$	Status Group Select
$\overline{ECS}$	Enable Current Status
INTE	Interrupt Enable
$\overline{CLK}$	Clock (INT F F)
$\overline{ELR}$	Enable Level Read
ETLG	Enable This Level Group
OUTPUTS	
$\overline{A_0}$-$\overline{A_2}$	Request Levels (Open Collector)
$\overline{INT}$	Interrupt (Act Low) (Open Collector)
ENLG	Enable Next Level Group

Figure 2. Pin Configuration

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ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias(1). −55°C to +125°C
Storage Temperature ..... −65°C to +160°C
All Output and Supply Voltages ..... −0.5V to +7V
All Input Voltages..... −1.0V to +5.5V
Output Currents ..... 100 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_C(1) = −55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ(1)	Max		
V_C	Input Clamp Voltage (All Inputs)			−1.2	V	I_C = −5 mA
I_F	Input Forward Current: ETLG Input All Other Inputs		−0.15 −0.08	−0.5 −0.25	mA mA	V_F = 0.45V
I_R	Input Reverse Current: ETLG Input All Other Inputs			80 40	μA μA	V_R = 5.5V
V_{IL}	Input LOW Voltage: All Inputs			0.8	V	V_{CC} = 5.0V
V_{IH}	Input HIGH Voltage: All Inputs	2.0			V	V_{CC} = 5.0V
I_{CC}	Power Supply Current		90	130	mA	(Note 2)
V_{OL}	Output LOW Voltage: All Outputs		0.3	0.45	V	I_{OL} = 10 mA
V_{OH}	Output HIGH Voltage: ENLG Output	2.4	3.0		V	I_{OH} = −1 mA
I_{OS}	Short Circuit Output Current: ENLG Output	−15	−35	−55	mA	V_{CC} = 5.0V
I_{CEX}	Output Leakage Current: $\overline{INT}$, $\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$			100	μA	V_{CEX} = 5.5V

CAPACITANCE V_{BIAS} = 2.5V, V_{CC} = 5V, T_C(1) = 25°C, f = 1 MHz

Symbol	Parameter	Limits			Units
		Min	Typ(1)	Max	
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance Except ENLG (Pin 14)		7	12	pF

NOTE:
1. Case temperatures are "instant on".

A.C. CHARACTERISTICS T_C[3] = −55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits			Units
		Min	Typ[1]	Max	
t_{CY}	$\overline{CLK}$ Cycle Time	85			ns
t_{PW}	$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	25	15		ns
t_{ISS}	INTE Setup Time to $\overline{CLK}$	16	12		ns
t_{ISH}	INTE Hold Time after $\overline{CLK}$	20	10		ns
t_{ETCS}[2]	ETLG Setup Time to $\overline{CLK}$	25	12		ns
t_{ETCH}[2]	ETLG Hold Time after $\overline{CLK}$	20	10		ns
t_{ECCS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	85	25		ns
t_{ECCH}	$\overline{ECS}$ Hold Time after $\overline{CLK}$	0			ns
t_{ECRS}	$\overline{ECS}$ Setup Time to $\overline{CLK}$	110	70		ns
t_{ECRH}	$\overline{ECS}$ Hold Time after $\overline{CLK}$	0			
t_{ECSS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	85	70		ns
t_{ECSH}[2]	$\overline{ECS}$ Setup Time after $\overline{CLK}$	0			ns
t_{DCS}[2]	$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{CLK}$	90	50		ns
t_{DCH}[2]	$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time after $\overline{CLK}$	0			ns
t_{RCS}	$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{CLK}$	100	55		ns
t_{RCH}	$\overline{R_0}$–$\overline{R_7}$ Hold Time after $\overline{CLK}$	0			ns
t_{ICS}	$\overline{INT}$ Setup Time to $\overline{CLK}$	55	35		ns
t_{CI}	$\overline{CLK}$ to $\overline{INT}$ Propagation Delay		15	30	ns
t_{RIS}	$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{INT}$	10	0		ns
t_{RIH}	$\overline{R_0}$–$\overline{R_7}$ Hold Time after $\overline{INT}$	35	20		ns
t_{RA}	$\overline{R_0}$–$\overline{R_7}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay		80	100	ns
t_{ELA}	$\overline{ELR}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay		40	55	ns
t_{ECA}	$\overline{ECS}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay		100	130	ns
t_{ETA}	ETLG to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay		35	70	ns
t_{DECS}	$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{ECS}$	20	10		ns
t_{DECH}	$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time after $\overline{ECS}$	20	10		ns
t_{REN}	$\overline{R_0}$–$\overline{R_7}$ to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	30	ns
t_{ECRN}	$\overline{ECS}$ to ENLG Propagation Delay		85	110	ns
t_{ECSN}	$\overline{ECS}$ to ENLG Propagation Delay		35	55	ns

NOTES:
1. Typical values are for T_C = 25°C, V_{CC} = 5.0V.
2. B_0–B_2, $\overline{SGS}$, CLK, R_4 grounded, all other inputs and all outputs open.
3. Case temperatures are "instant on".