UNIKC
Semiconductor

RoHS Compliant

P5010AV

N-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
100V	50mΩ @V_{GS} = 10V	5A

SOP-8

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[1]	T_A = 25 °C	I_D	5	A
	T_A = 100 °C		3	
Pulsed Drain Current[2]		I_{DM}	40	
Avalanche Current		I_{AS}	38	
Avalanche Energy	L = 0.1mH	E_{AS}	73	mJ
Power Dissipation	T_A= 25 °C	P_D	2	W
	T_A =100 °C		1.28	
Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	$R_{\theta JA}$		50	°C / W
Junction-to-Case	$R_{\theta JC}$		25	

[1]Pulse width limited by maximum junction temperature.

[2]Limited by Package

UNIKC
Semiconductor

RoHS Compliant

P5010AV
N-Channel Logic Level Enhancement Mode MOSFET

## ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)
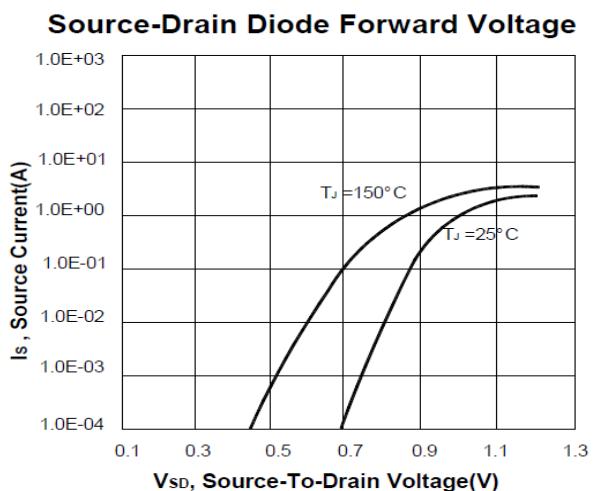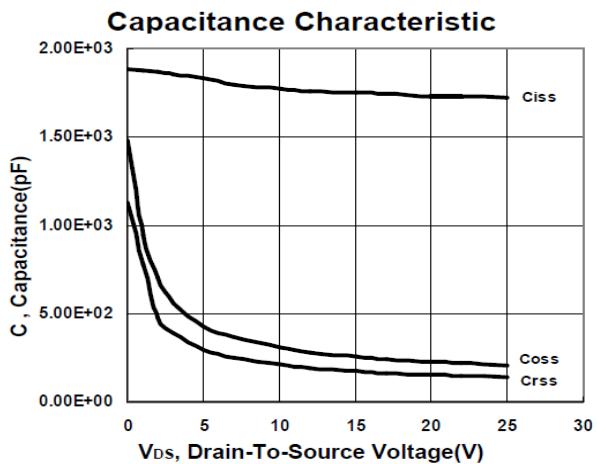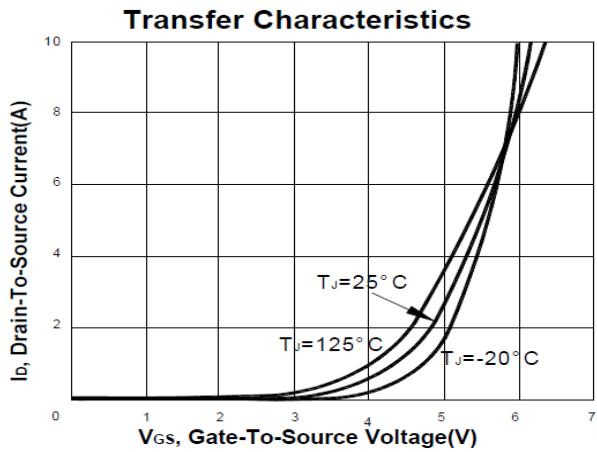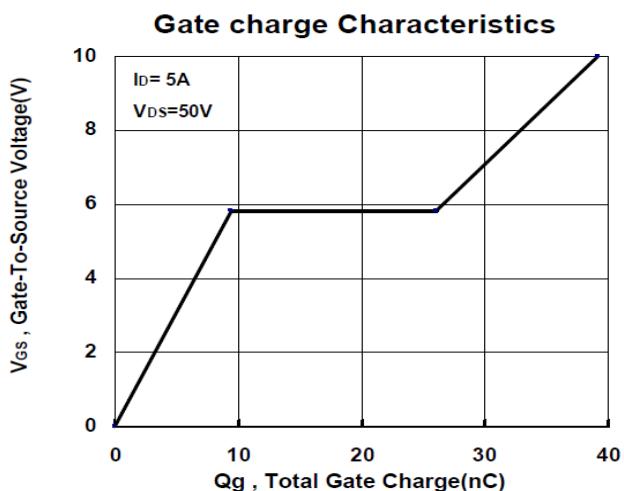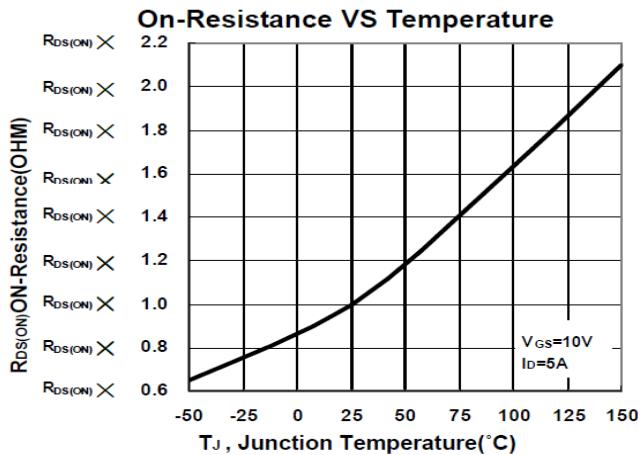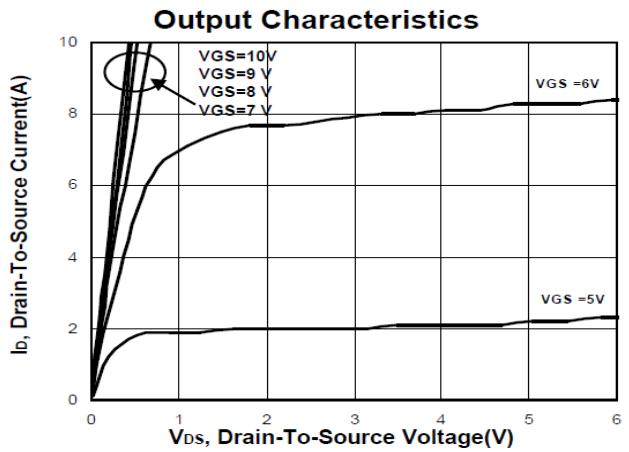
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±250	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V			1	µA
		V_{DS} = 80V, V_{GS} = 0V, T_J = 125 °C			10	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 5A		38	50	mΩ
Forward Transconductance[1]	g_{fs}	V_{DS} = 10V, I_D = 5A		6		S
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	40			A
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		1750		pF
Output Capacitance	C_{oss}			190		
Reverse Transfer Capacitance	C_{rss}			135		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz		2		Ω
Total Gate Charge[2]	Q_g	V_{DS} = 50V, I_D = 5A, V_{GS} = 10V		40		nC
Gate-Source Charge[2]	Q_{gs}			10		
Gate-Drain Charge[2]	Q_{gd}			17		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = 50V, $I_D \cong$ 5A, V_{GS} = 10V, R_{GEN} = 6Ω		7		nS
Rise Time[2]	t_r			28		
Turn-Off Delay Time[2]	$t_{d(off)}$			68		
Fall Time[2]	t_f			60		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I_S				1.6	A
Forward Voltage[1]	V_{SD}	I_F = 5A, V_{GS} = 0V			1.2	V
Reverse Recovery Time	t_{rr}	I_F = 5A, dI_F/dt = 100A / µS		54		nS
Reverse Recovery Charge	Q_{rr}			100		nC

[1]Pulse test : Pulse Width $\leq$ 300 µsec, Duty Cycle $\leq$ 2%.
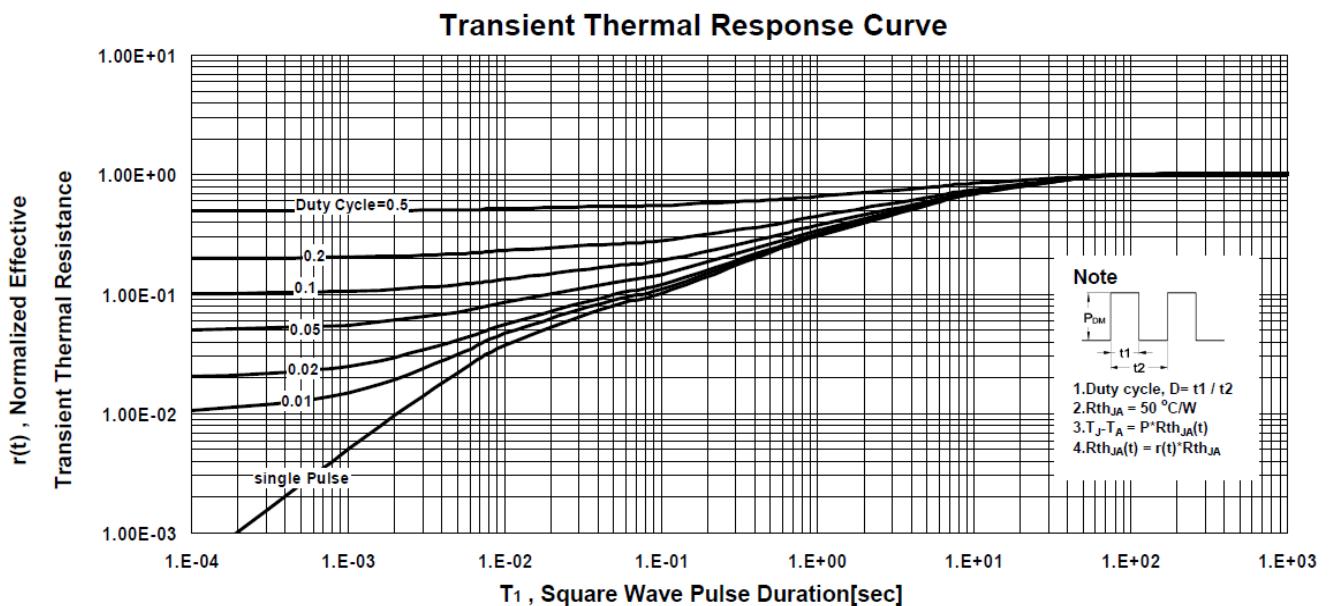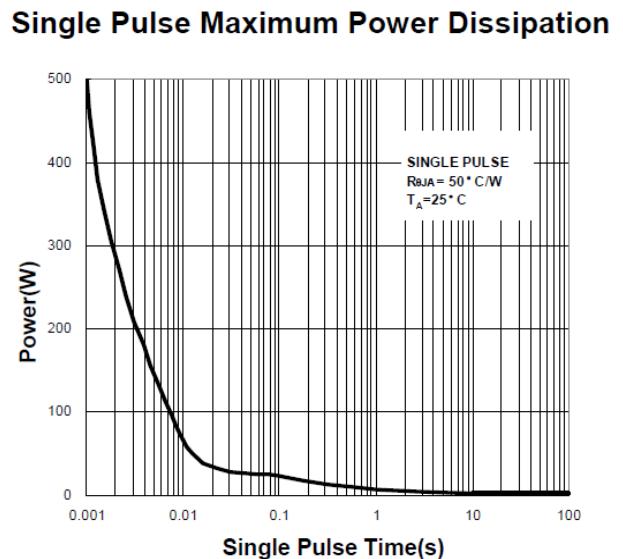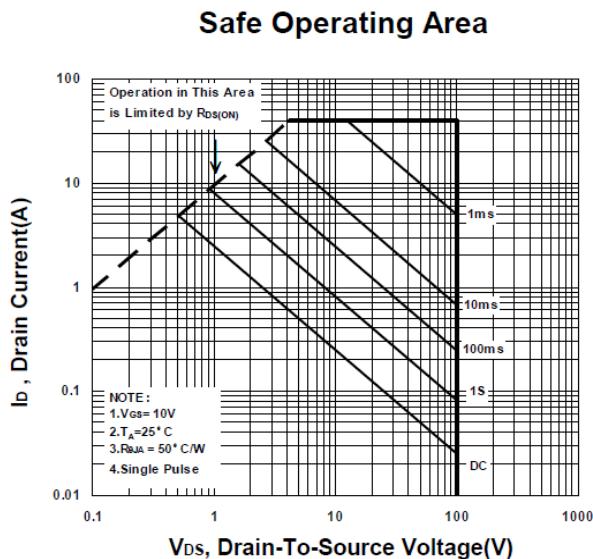
[2]Independent of operating temperature.

P5010AV
N-Channel Logic Level Enhancement Mode MOSFET

Output Characteristics

$V_{GS}=10V$
$V_{GS}=9$ V
$V_{GS}=8$ V
$V_{GS}=7$ V
$V_{GS}=6V$
$V_{GS}=5V$

I_D, Drain-To-Source Current(A)
V_{DS}, Drain-To-Source Voltage(V)

Transfer Characteristics

$T_J=25°C$
$T_J=125°C$
$T_J=-20°C$

I_D, Drain-To-Source Current(A)
V_{GS}, Gate-To-Source Voltage(V)

On-Resistance VS Temperature

$R_{DS(ON)}$ ON-Resistance(OHM)
$V_{GS}=10V$
$I_D=5A$
T_J, Junction Temperature(°C)

Capacitance Characteristic

Ciss
Coss
Crss

C , Capacitance(pF)
V_{DS}, Drain-To-Source Voltage(V)

Gate charge Characteristics

$I_D=5A$
$V_{DS}=50V$

V_{GS}, Gate-To-Source Voltage(V)
Qg, Total Gate Charge(nC)

Source-Drain Diode Forward Voltage

$T_J=150°C$
$T_J=25°C$

I_S, Source Current(A)
V_{SD}, Source-To-Drain Voltage(V)

P5010AV
N-Channel Logic Level Enhancement Mode MOSFET

Safe Operating Area

Operation in This Area is Limited by $R_{DS(ON)}$

I_D , Drain Current(A)

1ms
10ms
100ms
1S
DC

NOTE :
1.V_{GS}= 10V
2.T_A=25°C
3.$R_{θJA}$ = 50°C/W
4.Single Pulse

V_{DS}, Drain-To-Source Voltage(V)

Single Pulse Maximum Power Dissipation

Power(W)

SINGLE PULSE
$R_{θJA}$ = 50°C/W
T_A=25°C

Single Pulse Time(s)

Transient Thermal Response Curve

r(t) , Normalized Effective Transient Thermal Resistance

Duty Cycle=0.5
0.2
0.1
0.05
0.02
0.01

single Pulse

Note

P_{DM}
t1
t2

1.Duty cycle, D= t1 / t2
2.Rth_{JA} = 50°C/W
3.T_J-T_A = P*Rth_{JA}(t)
4.Rth_{JA}(t) = r(t)*Rth_{JA}

T_1 , Square Wave Pulse Duration[sec]

P5010AV
N-Channel Logic Level Enhancement Mode MOSFET

Package Dimension

SOP-8 MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8	4.9	5.0	H	0.4	0.6	0.93
B	3.8	3.9	4.0	I	0.19	0.21	0.25
C	5.79	6.0	6.2	J	0.25	0.375	0.5
D	0.33	0.4	0.51	K	0°	3°	18°
E	1.25	1.27	1.29				
F	1.1	1.3	1.65				
G	0.05	0.15	0.25				

8x0.72[.028]

6.46[.255]

8x1.78[.070]