

P45N02LI

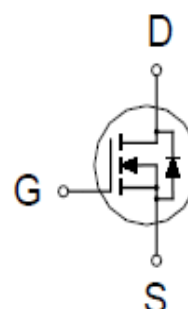
N-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
25V	20m Ω @ $V_{GS} = 10V$	26A



TO-251



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	26	A
	$T_C = 100\text{ }^{\circ}\text{C}$		16	
Pulsed Drain Current ¹		I_{DM}	70	
Avalanche Current		I_{AS}	13	
Avalanche Energy	$L = 0.1\text{ mH}$	E_{AS}	9	mJ
Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	22	W
	$T_C = 100\text{ }^{\circ}\text{C}$		8.9	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		5.6	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		70	

¹Pulse width limited by maximum junction temperature.

²Duty Cycle $\leq 1\%$.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	25			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	1.6	2.5	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20V, V _{GS} = 0V			25	μA
		V _{DS} = 20V, V _{GS} = 0V, T _J = 125°C			250	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} =10V	70			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 4.5V, I _D = 10A		21	41	mΩ
		V _{GS} =10V, I _D = 15A		14	20	
Forward Transconductance ¹	g _{fs}	V _{DS} = 15V, I _D = 15A		30		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 12.5V, f = 1MHz		529		pF
Output Capacitance	C _{oss}			100		
Reverse Transfer Capacitance	C _{rss}			76		
Total Gate Charge ²	Q _g	V _{DS} = 12.5V, V _{GS} = 10V, I _D = 15A		12		nC
Gate-Source Charge ²	Q _{gs}			2.3		
Gate-Drain Charge ²	Q _{gd}			3		
Turn-On Delay Time ²	t _{d(on)}	V _{DS} = 12.5V, I _D ≧ 15A, V _{GS} = 10V, R _{GS} =6Ω		18		nS
Rise Time ²	t _r			17		
Turn-Off Delay Time ²	t _{d(off)}			38		
Fall Time ²	t _f			10		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _J = 25 °C)						
Continuous Current	I _S				26	A
Forward Voltage ¹	V _{SD}	I _F = 15A, V _{GS} = 0V			1.4	V
Reverse Recovery Time	t _{rr}	I _F = 15A, dI _F /dt = 100A / μS		15		nS
Reverse Recovery Charge	Q _{rr}			6		nC

¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

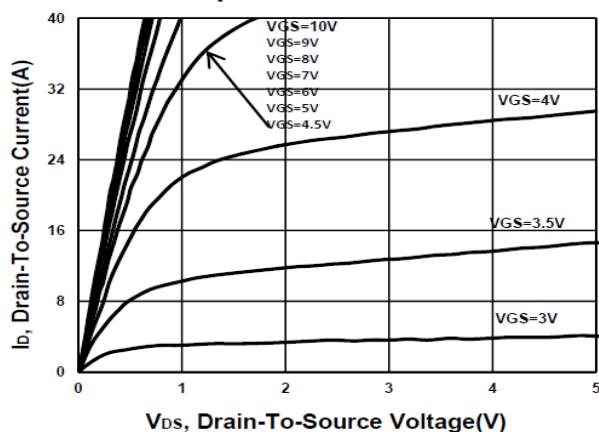
²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

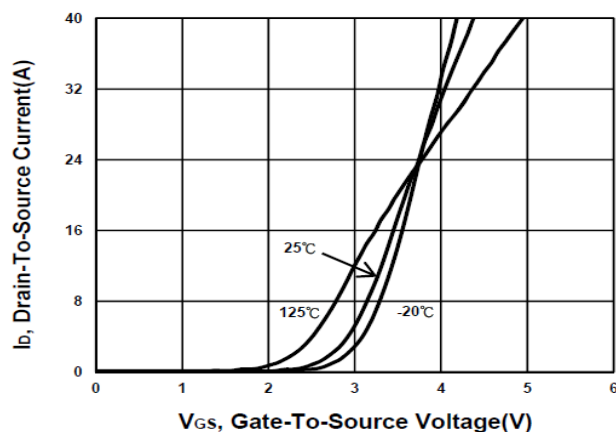
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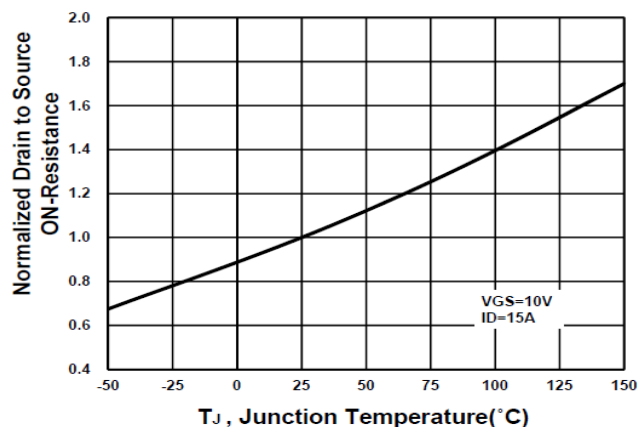
Output Characteristics



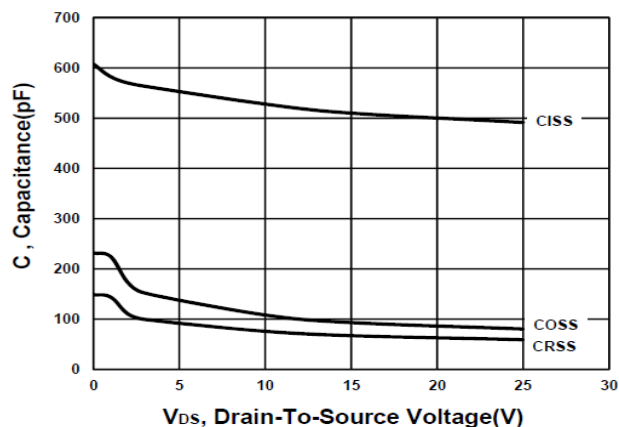
Transfer Characteristics



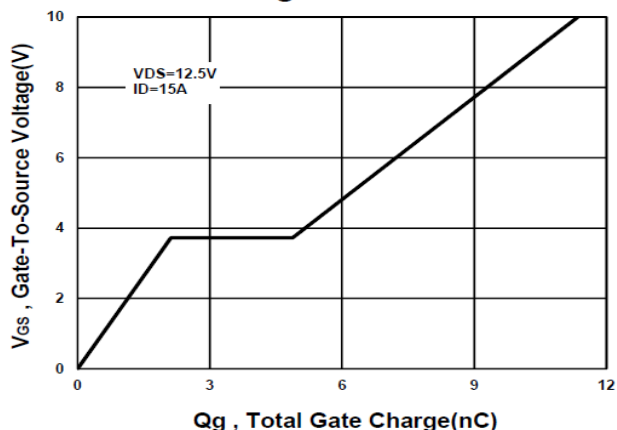
On-Resistance VS Temperature



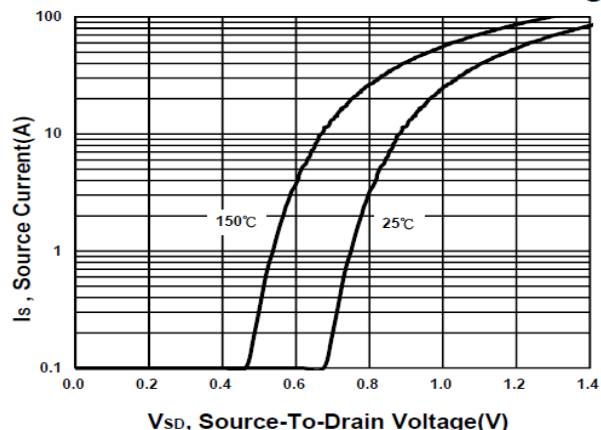
Capacitance Characteristic



Gate charge Characteristics



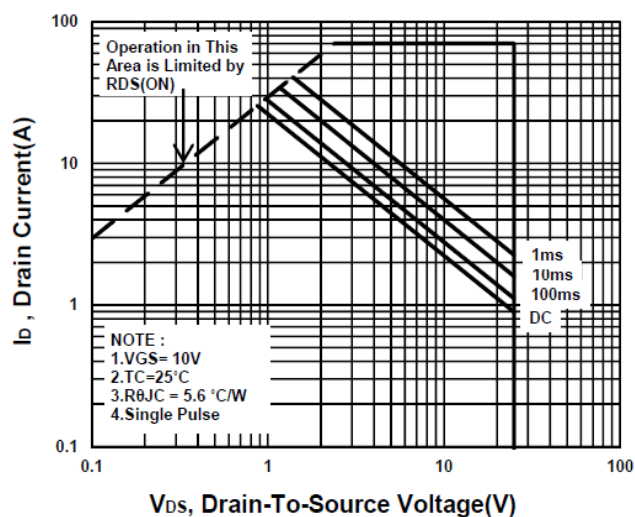
Source-Drain Diode Forward Voltage



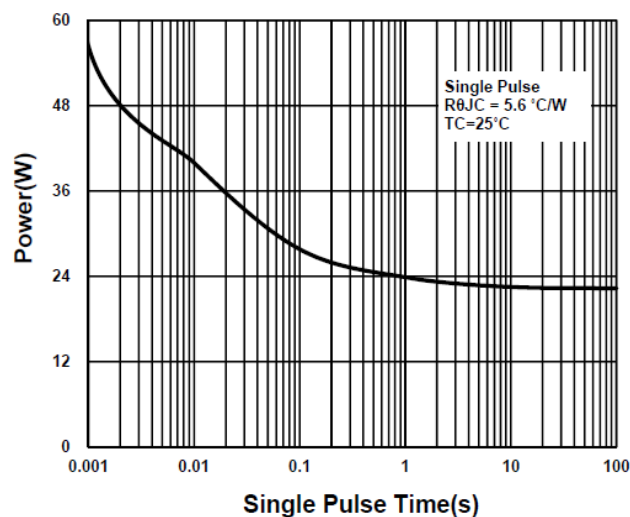
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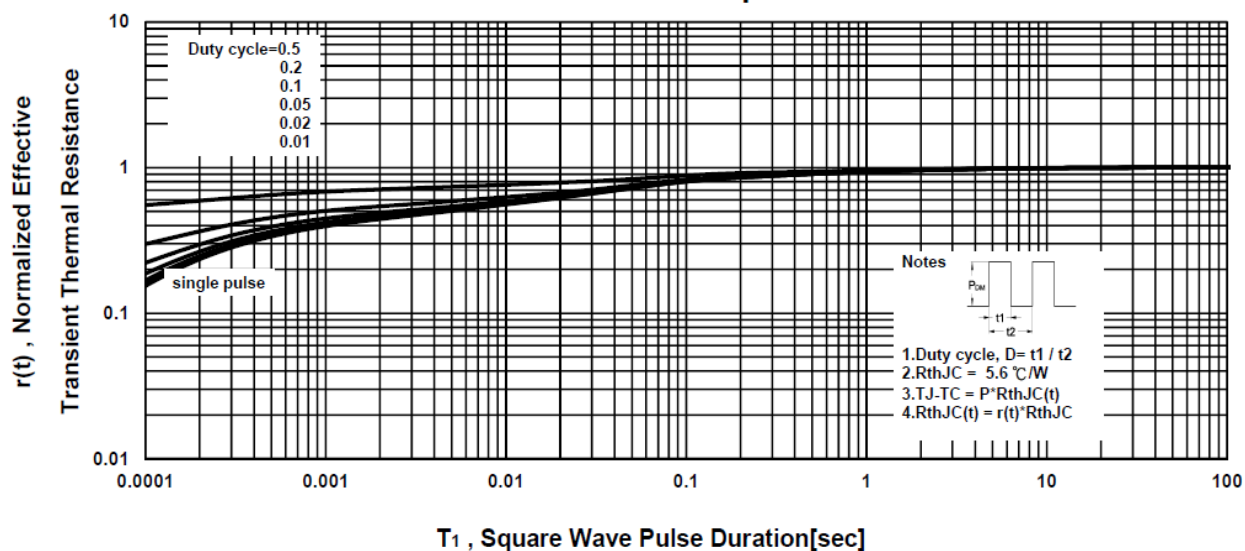
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



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Package Dimension

TO-251 MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	14	15	17.14	H	0.89		1.7
B	2.1	2.3	2.5	I	6.3		6.8
C	0.4	0.5	0.6	J	4.8		5.5
D	0.35	0.5	0.65	K	0.5	0.84	1.14
E	0.9	1.1	1.5	L	0.4	0.76	0.912
F	7		9.65	M		2.3	
G	5.3		6.22	N	1.4	2.16	2.23

