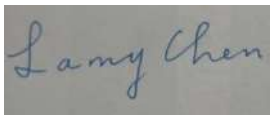
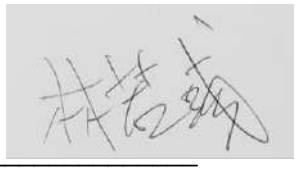
Model Name: P320HVN04.5

Issue Date: 2022/09/01

(＊)Preliminary Specifications
( )Final Specifications

Customer Signature	Date	AUO	Date
Approved By _____		Approval By PM Director CT Wu  _____	
Note		Reviewed By RD Director Lamy Chen  _____ Reviewed By Project Leader Chinese Wu  _____	
		Prepared By PM Wallace Lin  _____	

Contents

Record of Revision

Version	Date	Page	Description
0.0	2022/08/31	All	1st release

1 General Description

This specification applies to the 31.5 inch Color TFT-LCD Module P320HVN04.5. This LCD module has a TFT active matrix type liquid crystal panel 1920 x 1080 pixels, and diagonal size of 31.5 inch. This module supports 1920 x 1080 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot.

P320HVN04.5 has been designed to apply the 2 channel LVDS interface method. It is intended to support displays where high brightness, wide viewing angle, high color saturation, and high color depth are very important. Advanced wide temperature Liquid Crystal (-40~110℃) is also applied on this model to enhance the sunlight readability.

General Information

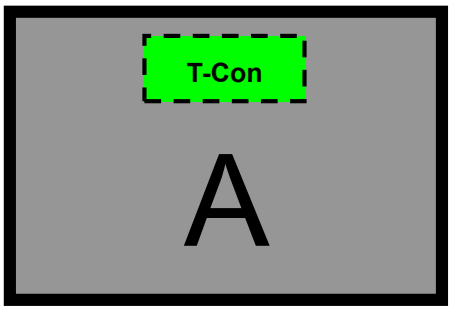
Items	Specification	Unit	Note
Active Screen Size	31.5	inch	
Display Area	698.4 (H) x 392.85(V)	mm	
Outline Dimension	721.2(H) x 415.65(V) x 33.8(D)	Mm	D: front bezel to D/B cover
Bezel Opening	701.4(H) x 395.85(V)	mm	
Bezel Width	9.9/9.9/9.9/9.9	mm	U/D/L/R
Front Bezel Surface finish	None		
Driver Element	a-Si TFT active matrix		
Display Colors	8 bit(16.7 million)	Colors	
Number of Pixels	1920x1080	Pixel	
Pixel Pitch	0.3637 (H) x 0.3637 (W)	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Sunglasses Readability	Portrait Mode		Note 3
Surface Treatment	Anti-Glare, 3H		Haze 28%
Rotate Function	Unachievable		Note 1
Display Orientation	Portrait/Landscape Enabled		Note 2
Operating Time	24/7		See Chapter 11.3 for details
Frame Rate	60	Hz	See Chapter 5.1 for details
LED MTTF	50K	hours	See Chapter 6.1 for details

Note 1. Rotate Function refers to LCD display could be able to rotate. This function does not work in this model.

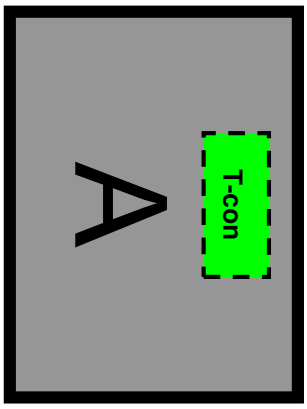
Note 2.

(1) **Landscape Mode: The default placement is T-Con Side on the lower side and the image is shown upright via viewing from the front.**

(2) **Portrait Mode: The default placement is that T-Con side has to be placed on the left side via viewing from the front.**



Landscape (Front view)



Portrait (Front view)

Note 3. The image can be seen via polarized sunglasses while this panel is placed in portrait mode.

Display Orientation:

Landscape

Portrait

Polarized Sunglasses

2 Absolute Maximum Ratings

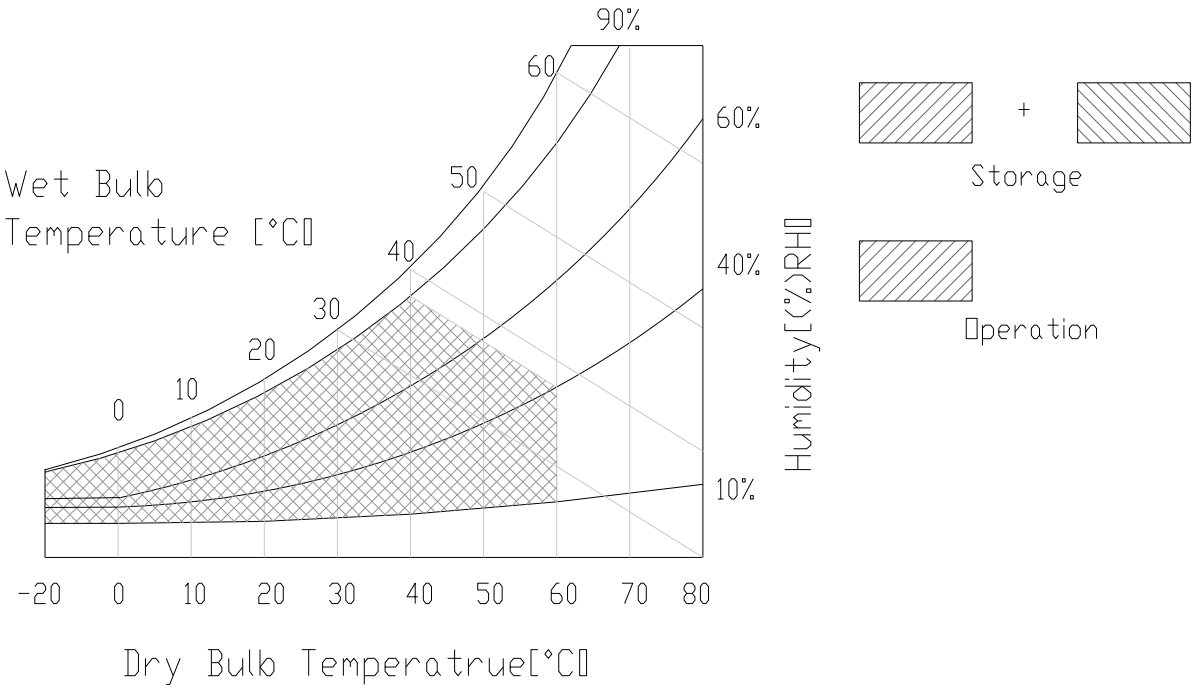
The followings are maximum values which if exceeded, may cause faulty operation or damage to the unit

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V_{DD}	-0.3	14	[Volt]	Note 1
Input Voltage of Signal	Vin	-0.3	4	[Volt]	Note 1
Operating Temperature	TOP	-20	+60	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	

Note 1. Duration:50 msec.

Note 2. Maximum Wet-Bulb should be 39℃ and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃.



3 Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 40 minutes in a dark environment at 25°C. The values specified are at an approximate distance 500 mm from the LCD surface at a viewing angle of φ and θ equal to 0°.

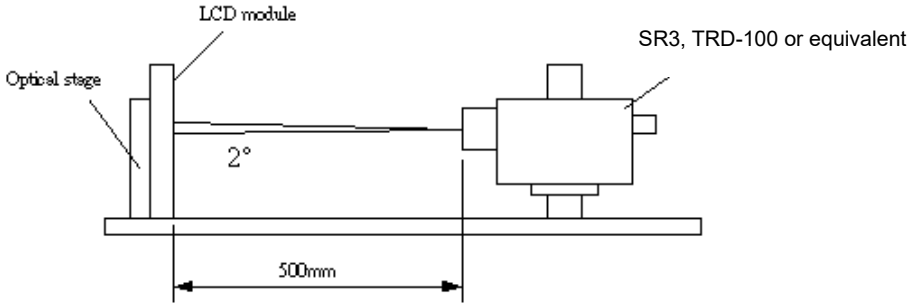


Fig. 1 Presents additional information concerning the measurement equipment and method.

Parameter		Symbol	Values			Unit	Notes
			Min.	Typ.	Max		
Contrast Ratio		CR	3200	4000	--		(1)
Surface Luminance (White)		L_{WH}	1200	1500	--	cd/m^2	(2)
Luminance Variation		$\delta_{WHITE(9P)}$	--	--	1.33		(3)
Response Time (G to G)		T_γ	--	8	10	ms	(4)
Color Gamut		sRGB		72		%	
Gamma		Gma	1.9	2.2	2.5		
Color Coordinates							
	Red	R_X	Typ.-0.03	0.592	Typ.+0.03		
		R_Y		0.322			
	Green	G_X		0.321			
		G_Y		0.570			
	Blue	B_X		0.163			
		B_Y		0.095			
	White	W_X		0.280			
		W_Y		0.290			
Viewing Angle							(5)
	x axis, right(φ=0°)	θ_r	85	89	--	degree	
	x axis, left(φ=180°)	θ_l	85	89	--	degree	
	y axis, up(φ=90°)	θ_u	85	89	--	degree	
	y axis, down (φ=270°)	θ_d	85	89	--	degree	

Note 1.

(1) Contrast Ratio (CR) is defined mathematically as:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance of } L_{on5}}{\text{Surface Luminance of } L_{off5}}$$

(2) Surface luminance is luminance value at point 5 across the LCD surface 50cm from the surface with all pixels displaying white. From more information see Fig. 2 LED current I_F = typical value (without driver board), LED input VDDB =24V, I_{DDB}. = Typical value (with driver board), L_{WH}=Lon5 where Lon5 is the luminance with all pixels displaying white at center 5 location.

(3) The variation in surface luminance, δWHITE is defined (center of Screen) as:

$$\delta_{WHITE(9P)} = \text{Maximum}(L_{on1}, L_{on2},\ldots,L_{on9}) / \text{Minimum}(L_{on1}, L_{on2},\ldots L_{on9})$$

(4) Response time T_γ is the average time required for display transition by switching the input signal for five luminance ratio (0%,25%,50%,75%,100% brightness matrix) and is based on Frame rate = 60Hz to optimize.

Measured Response Time		Target				
		0%	**25%**	**50%**	**75%**	**100%**
Start	**0%**		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

T_γ is determined by 10% to 90% brightness difference of rising or falling period. (As illustrated)

The response time is defined as the following figure(Fig. 2) and shall be measured by switching the input signal for “any level of gray(bright) “ and “any level of gray(dark)”.

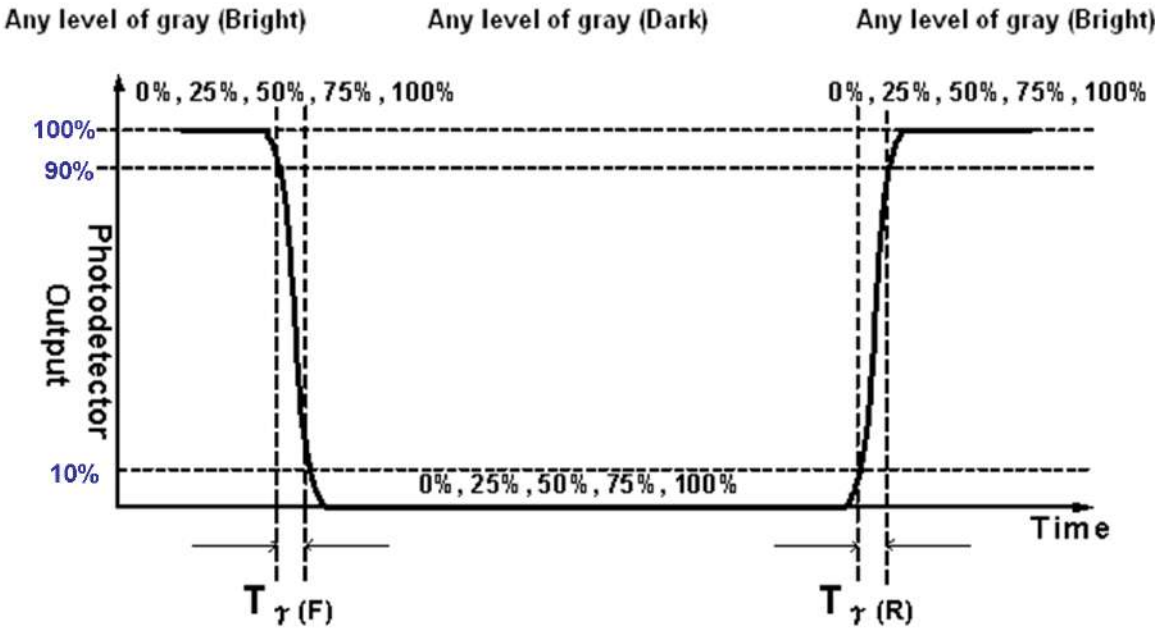
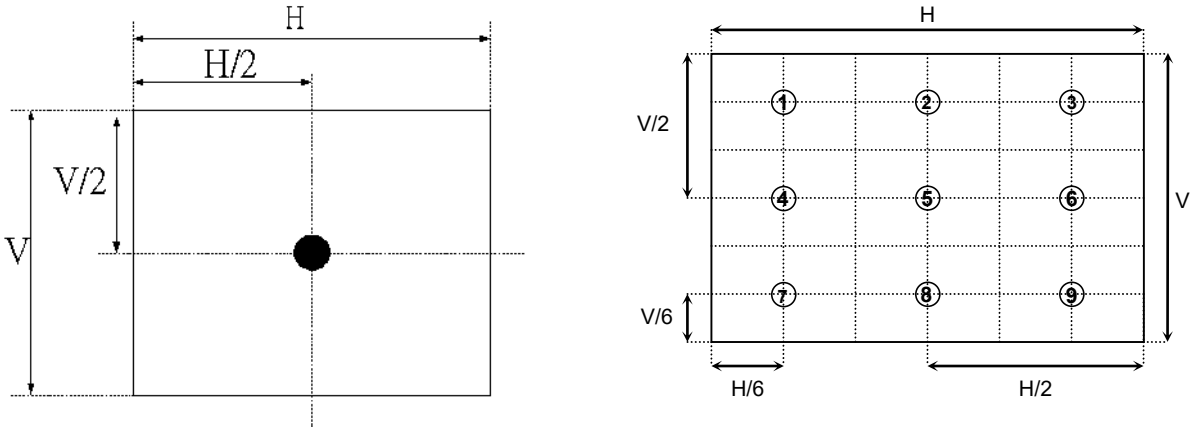


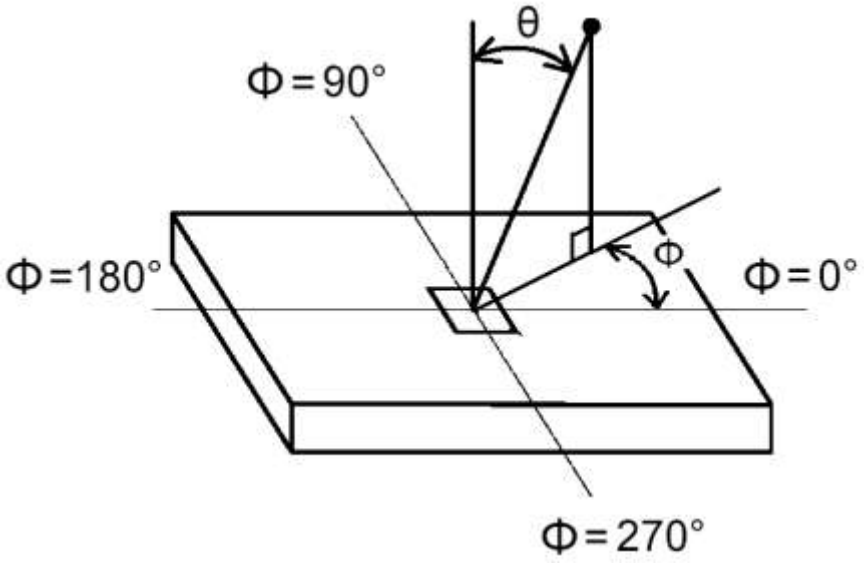
Fig. 2 Response time define

Fig. 3 Luminance



(5) Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see Fig. 4.

Fig. 4 Viewing Angle



4 Interface Specification

4.1 Input power

The P320HVN04.5 module requires power inputs which are employed to power the LCD electronics and to drive the TFT array and liquid crystal.

Item		Symbol	Min.	Typ.	Max	Unit	Note
Power Supply Input Voltage		V_{DD}	10.8	12	13.2	V	(1)
Power Supply Input Current	Black pattern	I_{DD}	-	0.39	0.47	A	(2)
	White pattern		-	0.78	0.94	A	
Power Consumption	Black pattern	P_C	-	4.68	5.64	Watt	
	White pattern		-	9.36	11.28	Watt	
Inrush Current		I_{RUSH}	--	--	3	A	(3)

Note 1.

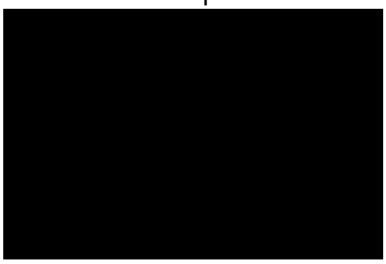
(1) The ripple voltage should be fewer than 5% of VDD.

(2) Test Condition:

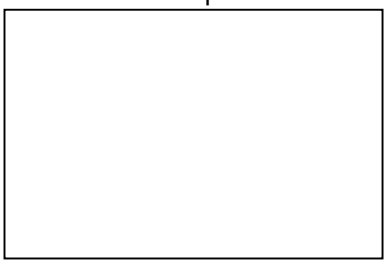
(1) V_{DD} = 12.0V, (2) Fv = 60Hz, (3) Fclk= 74.25MHz, (4) Temperature = 25 ℃

(5) Power dissipation check pattern. (Only for power design)

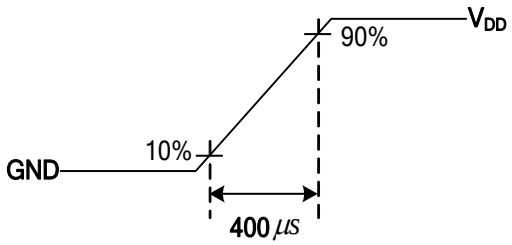
a. Black pattern



b. White pattern



(3) Measurement condition : Rising time = 400us



4.2 Input Connection

■ LCD connector: JAE FI-RTE51SZ-HF / P-two 187059-5122 or compatible

PIN	Symbol	Description	Note
1	N.C.	No connection (for AUO test only. Do not connect)	(2)
2	N.C.	No connection (for AUO test only. Do not connect)	(2)
3	N.C.	No connection (for AUO test only. Do not connect)	(2)
4	N.C.	No connection (for AUO test only. Do not connect)	(2)
5	N.C.	No connection (for AUO test only. Do not connect)	(2)
6	N.C.	No connection (for AUO test only. Do not connect)	(2)
7	LVDS_SEL	Open/High(3.3V) for NS, Low(GND) for JEIDA	(3)(4)
8	N.C.	No connection (for AUO test only. Do not connect)	(2)
9	N.C.	No connection (for AUO test only. Do not connect)	(2)
10	N.C.	No connection (for AUO test only. Do not connect)	(2)
11	GND	Ground	
12	CH1_Y0-	LVDS Channel 1, Signal 0-	
13	CH1_Y0+	LVDS Channel 1, Signal 0+	
14	CH1_Y1-	LVDS Channel 1, Signal 1-	
15	CH1_Y1+	LVDS Channel 1, Signal 1+	
16	CH1_Y2-	LVDS Channel 1, Signal 2-	
17	CH1_Y2+	LVDS Channel 1, Signal 2+	
18	GND	Ground	
19	CH1_CLK-	LVDS Channel 1, Clock -	
20	CH1_CLK+	LVDS Channel 1, Clock +	
21	GND	Ground	
22	CH1_Y3-	LVDS Channel 1, Signal 3-	
23	CH1_Y3+	LVDS Channel 1, Signal 3+	
24	N.C.	No connection (for AUO test only. Do not connect)	(2)
25	N.C.	No connection (for AUO test only. Do not connect)	(2)
26	N.C.	No connection (for AUO test only. Do not connect)	(2)
27	N.C.	No connection (for AUO test only. Do not connect)	(2)
28	CH2_Y0-	LVDS Channel 2, Signal 0-	
29	CH2_Y0+	LVDS Channel 2, Signal 0+	
30	CH2_Y1-	LVDS Channel 2, Signal 1-	
31	CH2_Y1+	LVDS Channel 2, Signal 1+	
32	CH2_Y2-	LVDS Channel 2, Signal 2-	
33	CH2_Y2+	LVDS Channel 2, Signal 2+	
34	GND	Ground	
35	CH2_CLK-	LVDS Channel 2, Clock -	
36	CH2_CLK+	LVDS Channel 2, Clock +	

37	GND	Ground	
38	CH2_Y3-	LVDS Channel 2, Signal 3-	
39	CH2_Y3+	LVDS Channel 2, Signal 3+	
40	N.C.	No connection (for AUO test only. Do not connect)	(2)
41	N.C.	No connection (for AUO test only. Do not connect)	(2)
42	N.C.	No connection (for AUO test only. Do not connect)	(2)
43	N.C.	No connection (for AUO test only. Do not connect)	(2)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No connection (for AUO test only. Do not connect)	(2)
48	V_{DD}	Power Supply, +12V DC Regulated	
49	V_{DD}	Power Supply, +12V DC Regulated	
50	V_{DD}	Power Supply, +12V DC Regulated	
51	V_{DD}	Power Supply, +12V DC Regulated	

Note 2.

(1) Pin number start from the left side as the following figure(Fig. 5).

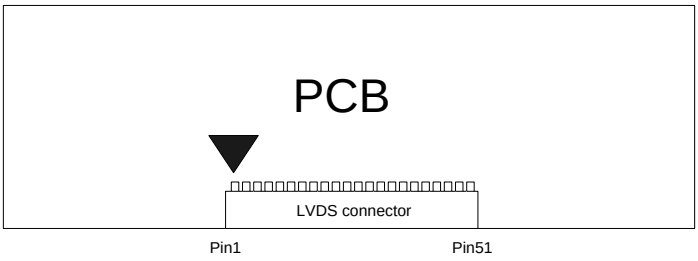


Fig. 5

(2) Please leave this pin unoccupied. It cannot be connected with any signal (Low/GND/High).

(3) Input control signal threshold voltage definition

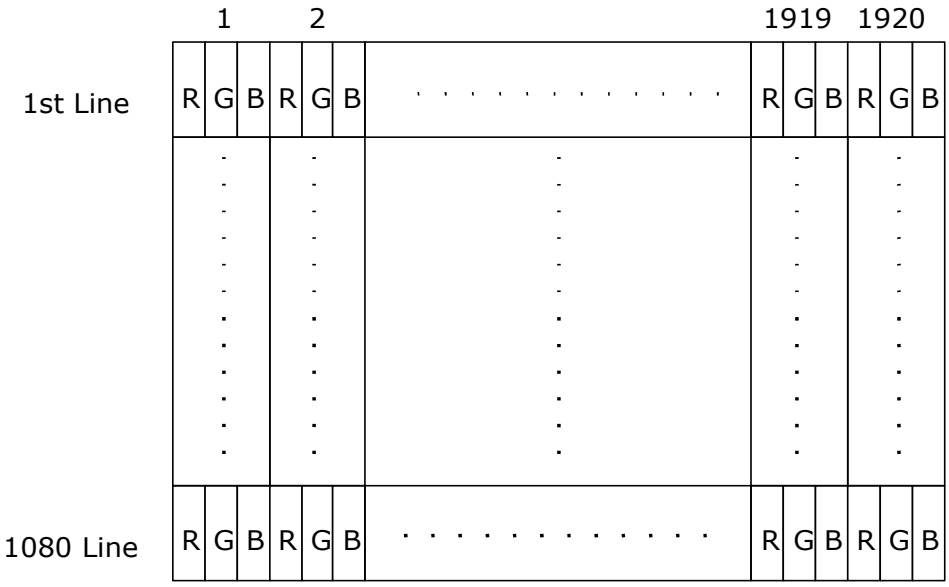
Item	Symbol	Min.	Typ.	Max.	Unit
Input High Threshold Voltage	VIH	2.7	-	3.6	V
Input Low Threshold Voltage	VIL	0	-	0.6	V

(4) LVDS data format selection

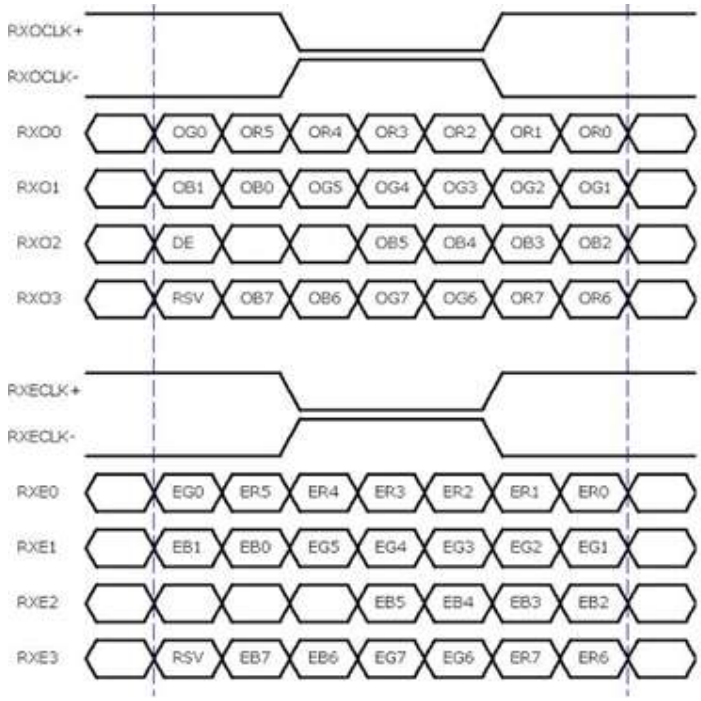
LVDS_SEL	Mode
H or OPEN	NS
L	JEIDA

4.3 Input Data Format

4.3.1 LCD Pixel Format



4.3.2 LVDS Data Format



8 Bit Color Bit Order			
MSB	R7	G7	B7
	R6	G6	B6
	R5	G5	B5
	R4	G4	B4
	R3	G3	B3
	R2	G2	B2
	R1	G1	B1
LSB	R0	G0	B0

Note 3.

a. O = "Odd Pixel Data" E = "Even Pixel Data"

b. Refer to 4.3.1 LCD pixel format, the 1st data is 1 (Odd Pixel Data), the 2nd data is 2 (Even Pixel Data) and the last data is 1920 (Even Pixel Data).

4.3.3 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 8 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

Color		Input Color Data																							
		RED								GREEN								BLUE							
		MSB							LSB	MSB							LSB	MSB							LSB
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

5 Signal Timing Specification

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

5.1 Input Timing

5.1.1 Timing table

Timing Table (DE only Mode)

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	1120	1125	1480	Th
	Active	Tdisp (v)		1080		2160
	Blanking	Tblk (v)	40	45	400	Th
Horizontal Section	Period	Th	1030	1100	1325	Tclk
	Active	Tdisp (h)		960		
	Blanking	Tblk (h)	70	140	365	Tclk
Clock	Frequency	Fclk=1/Tclk	53	74.25	82	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	60	67.5	73	KHz

Note 1.

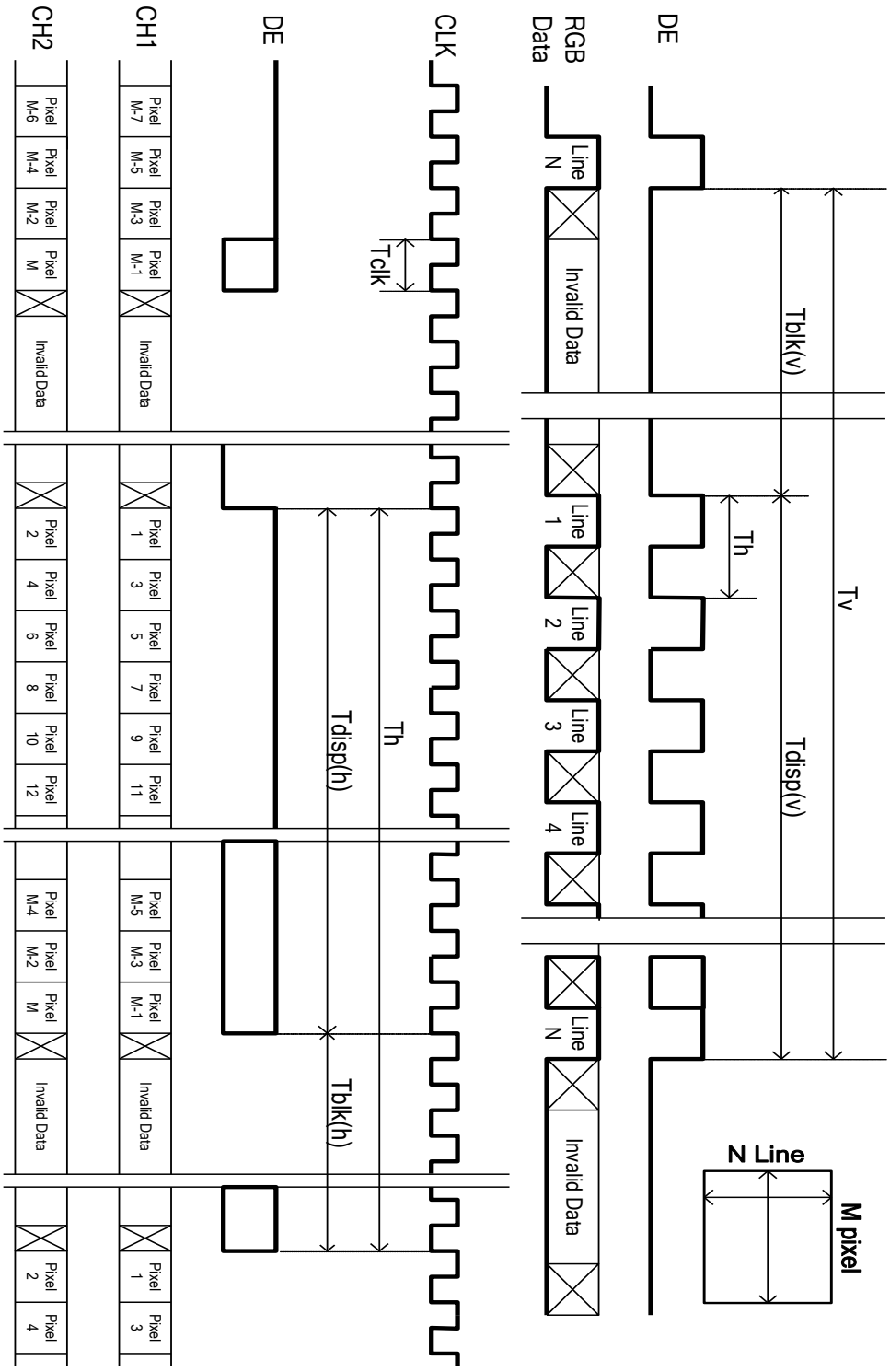
(1) **Display position is specific by the rise of DE signal only.**
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.

(2) **Vertical display position is specified by the rise of DE after a "Low" level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.**

(3) **If a period of DE "High" is less than 1920 DCLK or less than 1080 lines, the rest of the screen displays black.**

(4) **The display position does not fit to the screen if a period of DE "High" and the effective data period do not synchronize with each other.**

5.1.2 Signal Timing Waveform



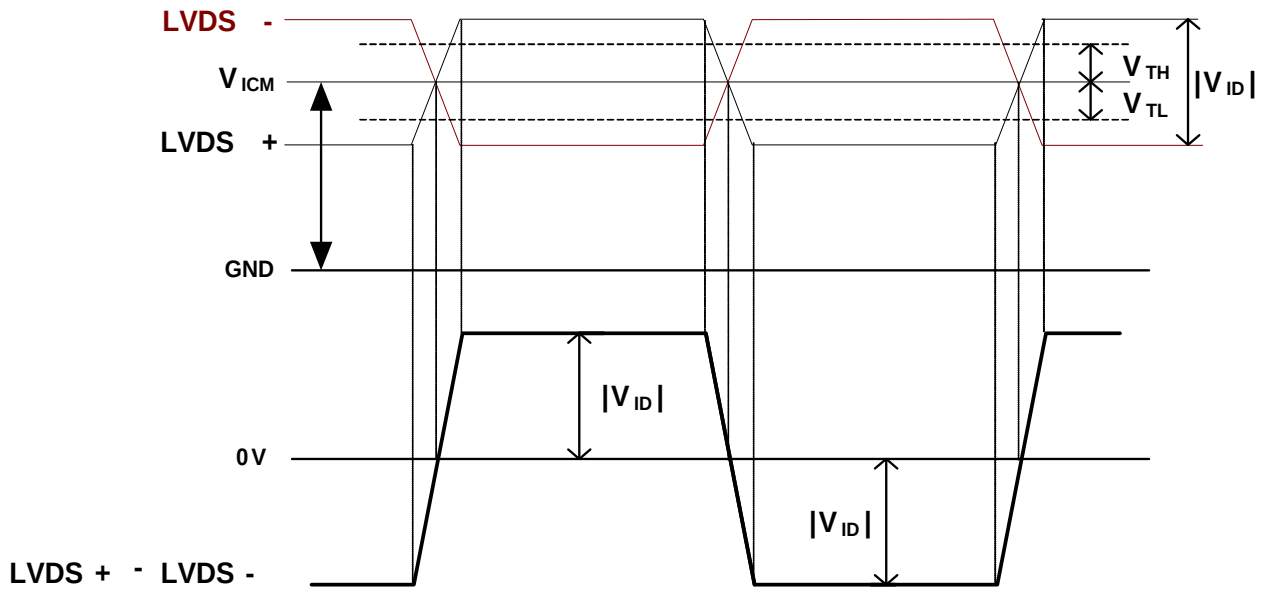
5.2 Input interface characteristics

5.2.1 LVDS spec

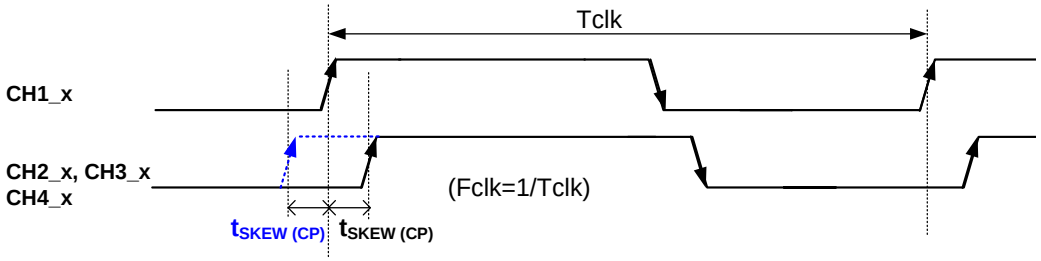
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LVDS Interface	Input Differential Voltage	$\|V_{ID}\|$	200	400	600	mV_{DC}	(1)
	Differential Input High Threshold Voltage	V_{TH}	+100	--	+300	mV_{DC}	(1)
	Differential Input Low Threshold Voltage	V_{TL}	-300	--	-100	mV_{DC}	(1)
	Input Common Mode Voltage	V_{ICM}	1.1	1.25	1.4	V_{DC}	(1)
	Input Channel Pair Skew Margin	$t_{SKEW\ (CP)}$	-500	--	+500	ps	(2)
	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	--	Fclk +3%	MHz	(3)
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30	--	200	KHz	(3)
	Receiver Data Input Margin Fclk = 85 MHz Fclk = 65 MHz	tRMG	 -0.4 -0.5	 -- --	 0.4 0.5	ns	(4)

Note 1.

(1) **VICM = 1.25V**



(2) **Input Channel Pair Skew Margin**



(3) **LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below Fig. 6.**

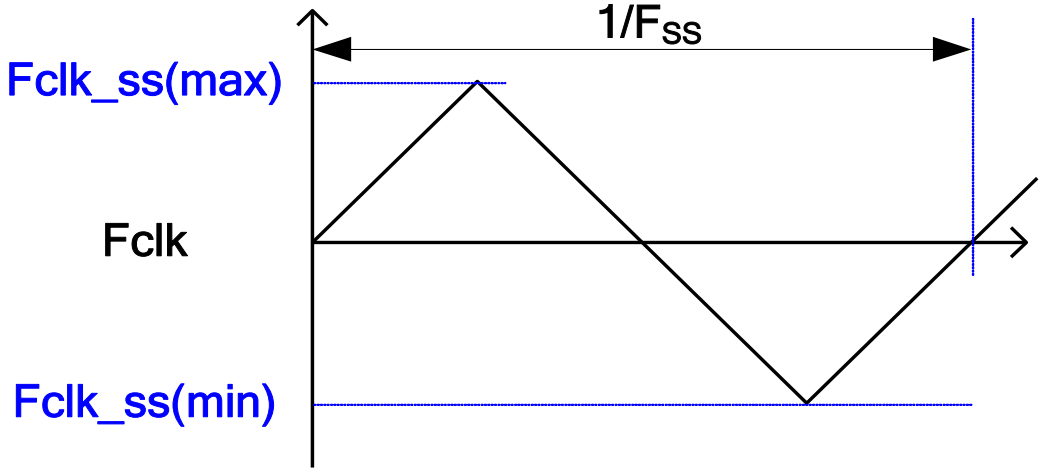
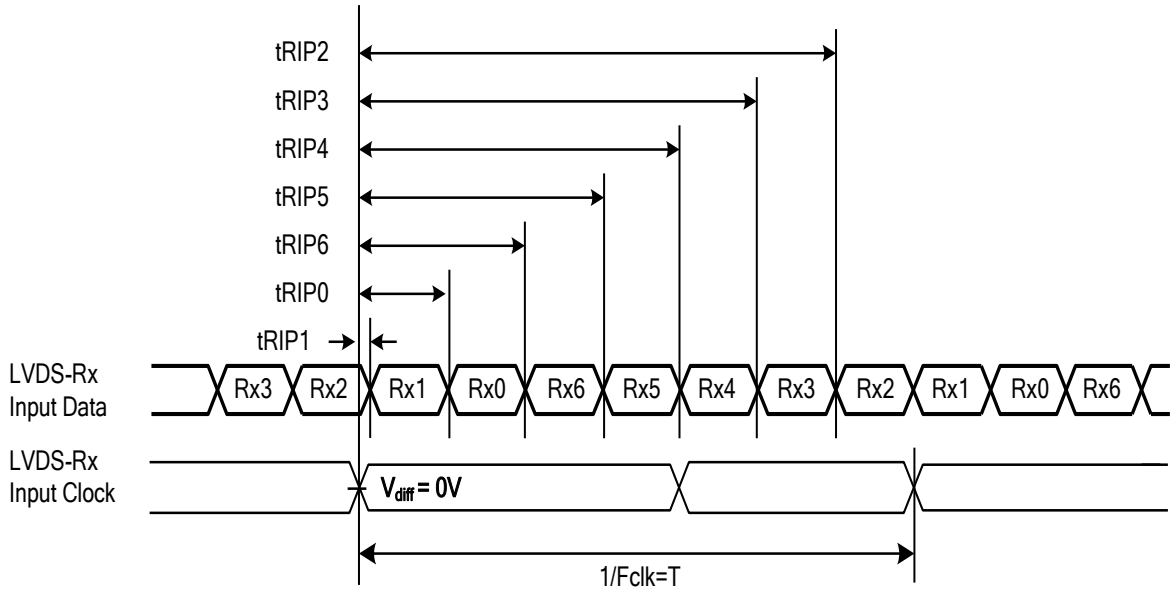


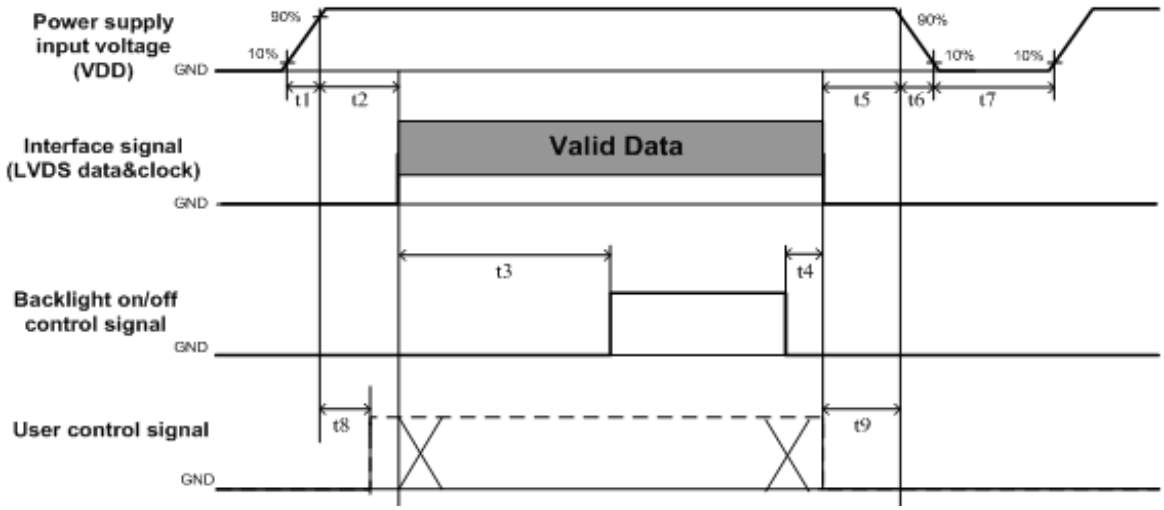
Fig. 6

(5) **Receiver Data Input Margin**

Parameter	Symbol	Rating			Unit	Note
		Min	Type	Max		
Input Clock Frequency	Fclk	Fclk (min)	--	Fclk (max)	MHz	T=1/Fclk
Input Data Position0	tRIP1	-|tRMG|	0	|tRMG|	ns	
Input Data Position1	tRIP0	T/7-|tRMG|	T/7	T/7+|tRMG|	ns	
Input Data Position2	tRIP6	2T/7-|tRMG|	2T/7	2T/7+|tRMG|	ns	
Input Data Position3	tRIP5	3T/7-|tRMG|	3T/7	3T/7+|tRMG|	ns	
Input Data Position4	tRIP4	4T/7-|tRMG|	4T/7	4T/7+|tRMG|	ns	
Input Data Position5	tRIP3	5T/7-|tRMG|	5T/7	5T/7+|tRMG|	ns	
Input Data Position6	tRIP2	6T/7-|tRMG|	6T/7	6T/7+|tRMG|	ns	



5.3 Power Sequence for LCD



Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2	40	---	---	ms
t3	640	---	---	ms
t4	0[*1]	---	---	ms
t5	0	---	---	ms
t6	---	---	---[*2]	ms
t7	1000	---	---	ms
t8	20[*3]	---	50	ms
t9	0	---	---	ms

Note 1.

(1) **t4=0 : concern for residual pattern before BLU turn off.**

(2) **t6 : voltage of VDD must decay smoothly after power-off. (Customer system decide this value)**

(3) **When user control signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.**

6 Backlight Specification

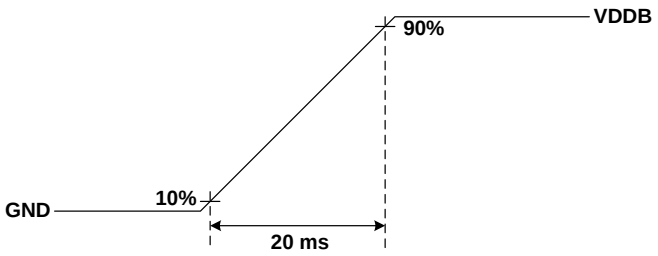
6.1 Electrical specification

	Item	Symbol		Condition	Min	Typ	Max	Unit	Note
1	Power Supply Input Voltage	VDDB		-	22.8	24	25.2	V	-
2	Power Supply Input Current	I_{DDB}		VDDB=24V	-	2.48	-	A	(1)
3	Power Consumption	P_{DDB}		VDDB=24V	-	60	69.6	Watt	(1)
4	Inrush Current	I_{RUSH}		VDDB=24V	-	-	6	A	(2)
5	Control signal voltage	V_{Signal}	Hi	VDDB=24V	2	-	5.5	V	-
			Low		0	-	0.8		(3)
6	Control signal current	I_{Signal}		VDDB=24V	-	-	1.5	mA	-
7	External PWM Duty ratio (input duty ratio)	D_EPWM		VDDB=24V	0	-	100	%	(4)
8	External PWM Frequency	F_EPWM		VDDB=24V	120	-	960	Hz	(4)
9	DET status signal	DET	HI	VDDB=24V	Open Collector			V	(5)
			Lo		0	-	0.8	V	(5)
10	Input Impedance	Rin		VDDB=24V	300			Kohm	-
11	LED MTTF	LED_MTTF		-	50,000	-	-	Hr	(6)(7)

Note 1.

(1) Dimming ratio= 100%,（Ta=25±5℃, Turn on for 45minutes）

(2) MAX input current while DB turn on, measurement condition VDDB rising time=20ms(VDDB: 10%~90%)



(3) When BLU off (VDDB = 24V , VBLON = 0V) , IDDB (max) = 0.1A

(4) Less than 5% dimming control is functional well and no backlight shutdown happened

(5) Normal: 0~0.8V ; Abnormal : Open collector

(6) LED MTTF is defined as the time which luminance of LED is 50% compared to its original value. [Operating condition: Continuous operating at Ta = 25±2℃, for single LED only]

(7) MTTF is a reference index, it is not representative of warranty.

6.2 Input Pin Assignment

LED DB connector: CI0114M1HRL-NH(CviLux)

Pin	Symbol	Description	Note
1	VDDB	Power Supply Input Voltage	
2	VDDB	Power Supply Input Voltage	
3	VDDB	Power Supply Input Voltage	
4	VDDB	Power Supply Input Voltage	
5	VDDB	Power Supply Input Voltage	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	DET	BLU status detection:	(1)
12	VBLON	BLU On-Off control:	(2)(3)
13	NC	NC	(4)
14	PDIM	External PWM	(2)(5)

Note 1.

(1) DET status

DET	BLU status
0 ~ 0.8V	Normal
Open collector	Abnormal

Recommend pull high R > 10K ohm, pull high voltage VDD = 3.3V

(2) input control signal threshold voltage definition

Item	Symbol	Min.	Typ.	Max.	Unit
Input High Threshold Voltage	VIH	2	-	5.5	V
Input Low Threshold Voltage	VIL	0	-	0.8	V

(3) VBLON

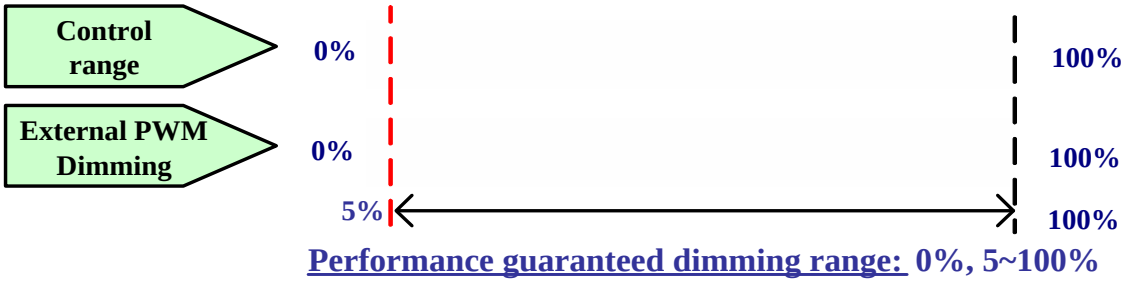
Mode selection

VBLON	Note
H or OPEN	BL On
L	BL Off

(4) Please leave this pin unoccupied. It cannot be connected by any signal (Low/GND/High).

(5) PDIM

PWM Dimming range:



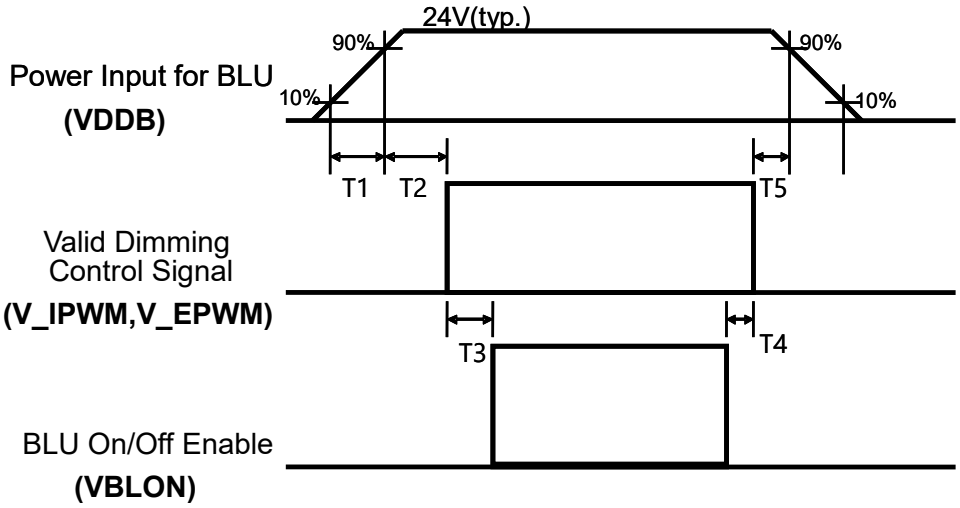
External PWM function dimming ratio 0%~100%, Judge condition as below:

(1) Backlight module must be lighted ON normally.

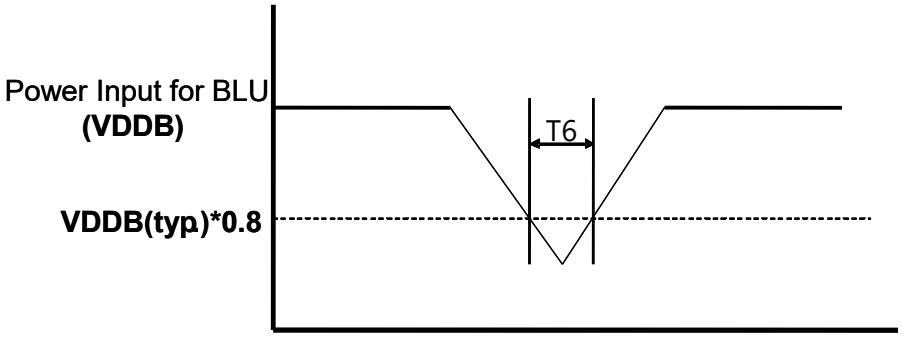
(2) All protection function must work normally.

(3) Uniformity and flicker could be guaranteed at External PWM function dimming ratio 5%~100%

6.3 Power Sequence for Backlight



Dip condition



Parameter	Min	Typ	Max	Units
T1	20	-	-	ms
T2	250	-	-	ms
T3	200			ms
T4	0	-	-	ms
T5	0	-	-	ms
T6		-	1000	ms*1

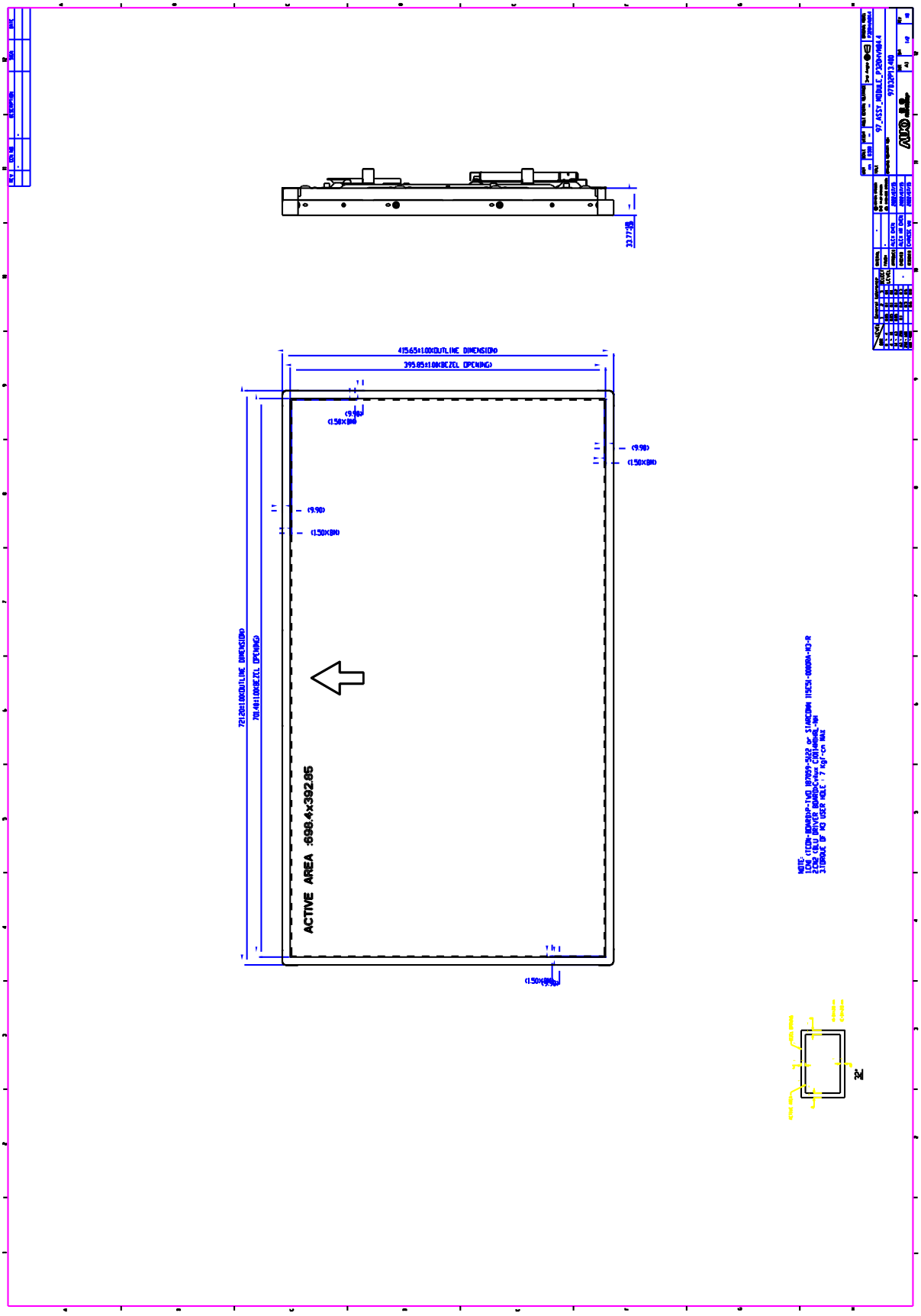
Note 1. T6 describes VDDB dip condition and VDDB couldn't lower than 10% VDDB.

7 Mechanical Characteristics

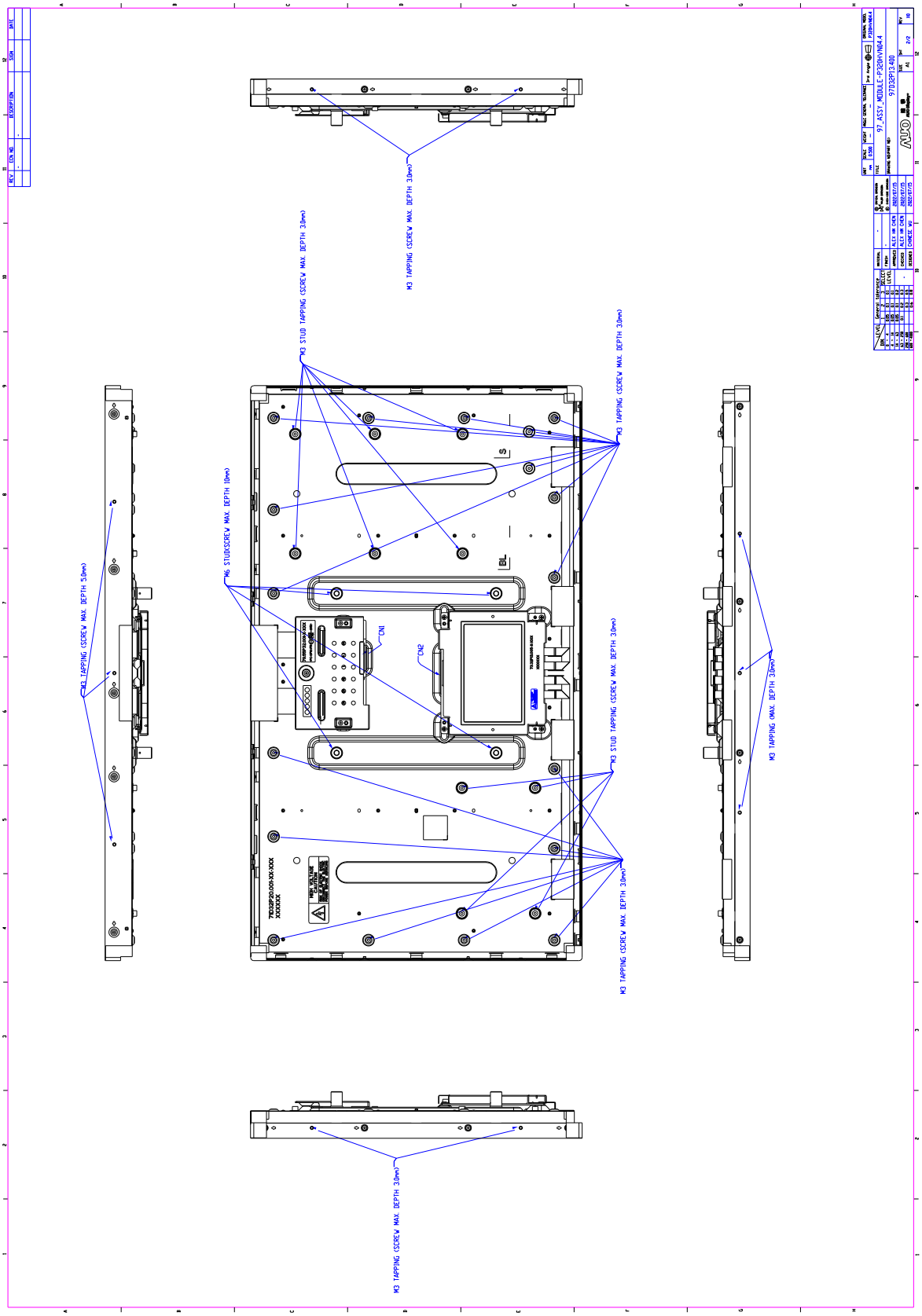
The contents provide general mechanical characteristics for the model P320HVN04.5. In addition the figures in the next page are detailed mechanical drawing of the LCD.

Item		Dimension	Unit	Note
Outline Dimension	Horizontal	721.2	mm	
	Vertical	415.65	mm	
	Depth (Dmin)	33.8	mm	Front bezel to Back Bezel
	Depth (Dmax)	58.5	mm	Front Bezel to Wall Mount
Weight	5.2		Kg	

Front View



Back View


M3 TAPPING (SCREW MAX. DEPTH 3.0mm)
M3 STUD TAPPING (SCREW MAX. DEPTH 3.0mm)
M3 TAPPING (SCREW MAX. DEPTH 3.0mm)
M6 STUD(SCREW MAX. DEPTH 10mm)
M3 TAPPING (SCREW MAX. DEPTH 5.0mm)
M3 STUD TAPPING (SCREW MAX. DEPTH 3.0mm)
M3 TAPPING (SCREW MAX. DEPTH 3.0mm)
M3 TAPPING (SCREW MAX. DEPTH 3.0mm)
M3 TAPPING (SCREW MAX. DEPTH 3.0mm)
CN1
CN2

8 Reliability Test Items

	Test Item	Q'ty	Condition
1	High temperature storage test	3	60℃, 500hrs
2	Low temperature storage test	3	-20℃, 500hrs
3	High temperature operation test	3	60℃, 500hrs
4	High temperature and High humidity operation(THB)	3	60℃ 75%, 500hrs
5	Low temperature operation test	3	-20℃, 500hrs
6	Vibration test (With carton)	1(PKG)	Random wave (1.04Grms 2~200Hz) Duration : X,Y,Z 20min per axes
7	Drop test (With carton)	1(PKG)	Height: 45.7 cm Direction: 1 corner 3edges 6flats (ASTMD 5276)

9 International Standard

9.1 Safety

(1) UL 62368-1; Audio/video, information and communication technology equipment – Part 1: Safety requirements.

(2) IEC 62368-1; Audio/video, information and communication technology equipment – Part 1: Safety requirements.

(3) EN 62368-1; Audio/video, information and communication technology equipment – Part 1: Safety requirements.

9.2 EMC

(1) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz. “American National standards Institute(ANSI), 1992

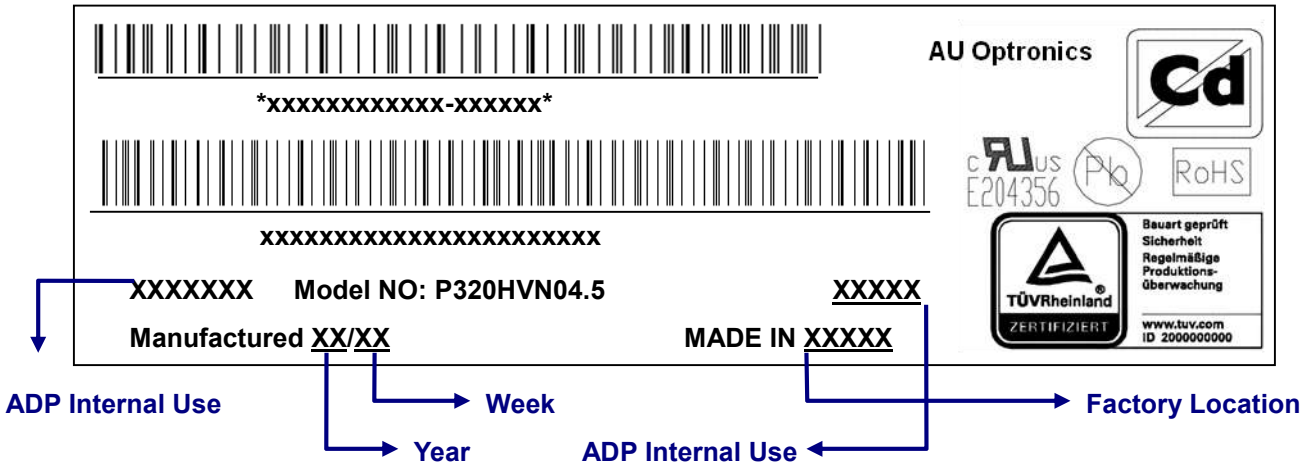
(2) C.I.S.P.R “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” International Special committee on Radio Interference.

(3) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” European Committee for Electrotechnical Standardization. (CENELEC), 1998.

10 Packing

10.1 Definition of Label

A. Panel Label:



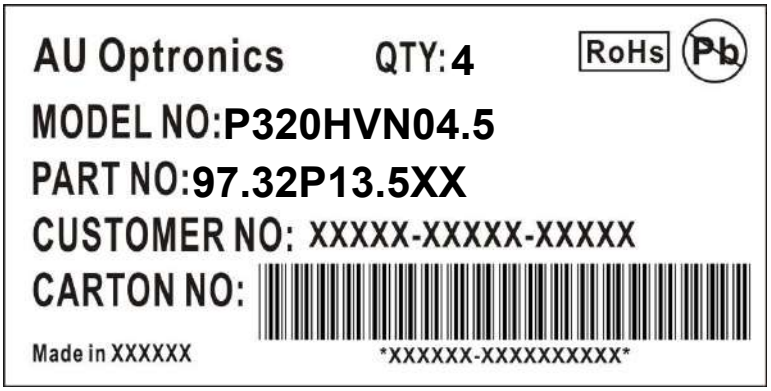
Green mark description

(1) For Pb & Cd Free Product, ADP will add Pb & Cd for identification.

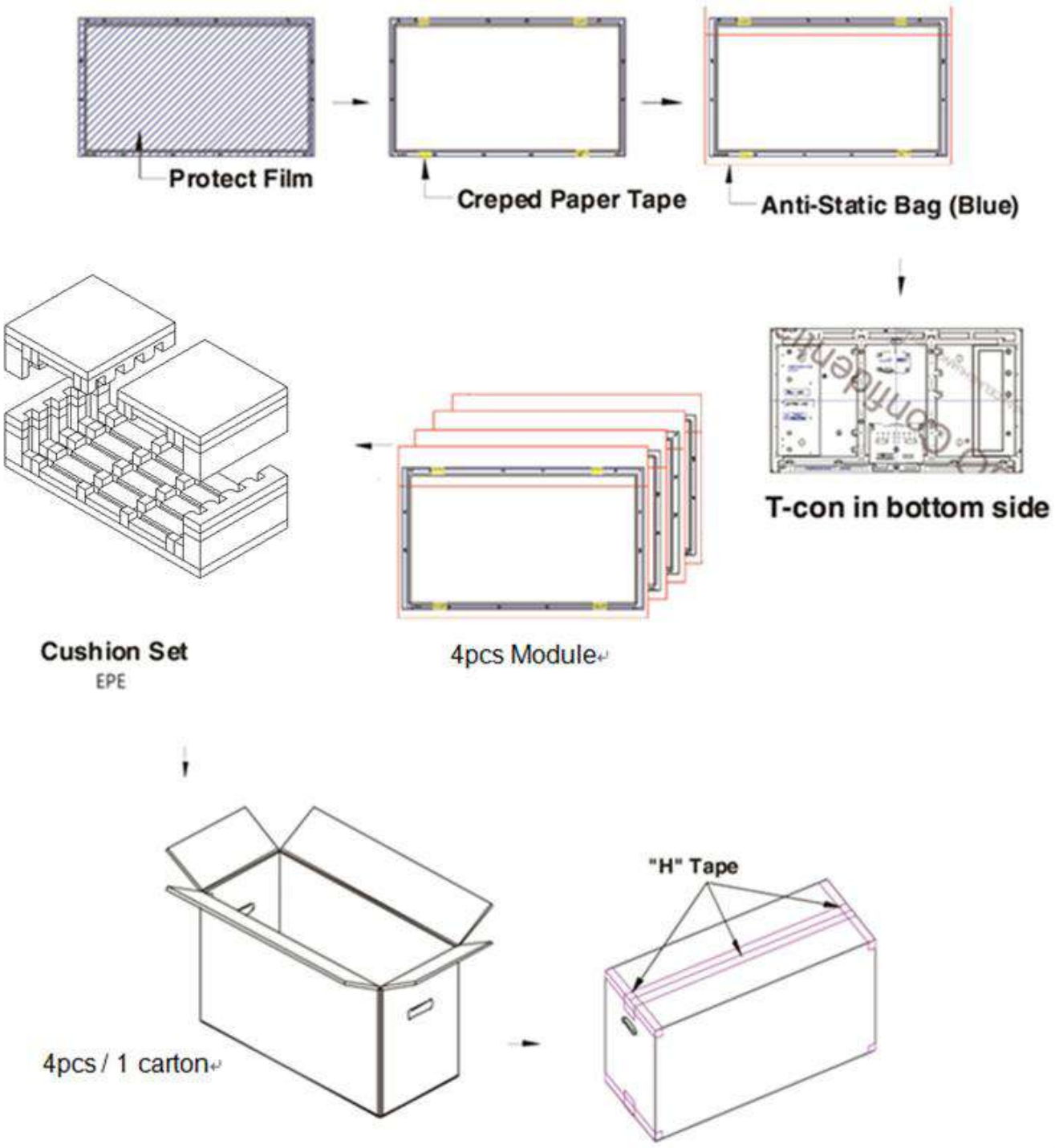
(2) For RoHs compatible products, ADP will add RoHS for identification.

Note: The green Mark will be present only when the green documents have been ready by ADP internal green team. (definition of green design follows the ADP green design checklist.)

B. Carton Label:

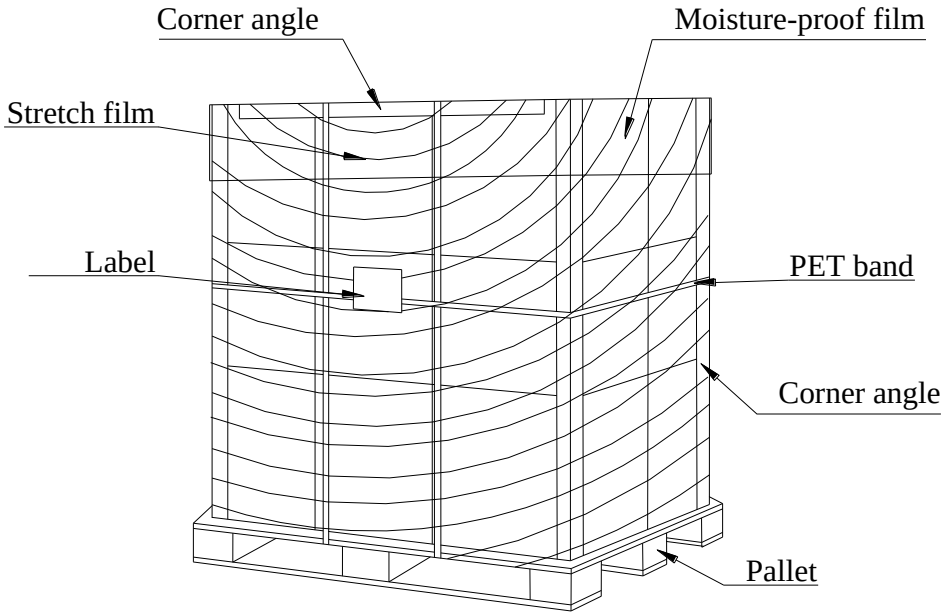


10.2 Packing Methods



10.3 Pallet and Shipment Information

	Item	Specification			Packing Remark
		Qty.	Dimension	Weight (kg)	
1	Packing Box	4pcs/box	820mm*376mm*537mm	23.84	Panel 5.2kg
2	Pallet	1	1150mm*840mm*132mm	15.6	
3	Boxes per Pallet	6 boxes/pallet			
4	Panels per Pallet	24 pcs/pallet			
5	Pallet	24	1150mm*840mm*1206mm	158.64	



11 Precautions

Please pay attention to the followings when you use this TFT LCD module.

11.1 Mounting Precautions

(1) You must mount a module using holes arranged in four corners or four sides.

(2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied to module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.

(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.

(4) You should adopt radiation structure to satisfy the temperature specification.

(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter cause circuit broken by electro-chemical reaction.

(6) Do not touch, push or rub the exposed polarizer with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)

(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizer. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.

(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.

(9) Do not open the case because inside circuits do not have sufficient strength.

11.2 Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage: V=±200mV(Over and under shoot voltage)

(2) Response time depends on the temperature. (In lower temperature, it becomes longer.)

(3) Brightness depends on the temperature. (In lower temperature, it may become lower.) And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.

(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.

(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may

be important to minimize the interface.The conductive material and signal cables are kept away from LED driver inductor to prevent abnormal display, sound noise and temperature rising.

11.3 Operating Condition for Public Information Display

The device listed in the product specification is designed and manufactured for PID (Public Information Display) application. To optimize module's lifetime and function, below operating usages are required.

(1) Normal operating condition
   A. Operating temperature: -20~60℃
   B. Operating humidity: 10~90%
   C. Display pattern: dynamic pattern (Real display).
      Note) Long-term static display would cause image sticking.

(2) Operation usage to protect against image sticking due to long-term static display.
   A. Suitable operating time: 24 hours a day
   B. Liquid Crystal refresh time is required. Cycling display between 5 minutes' information (static) display and 10 seconds' moving image.
   C. Periodically change background and character (image) color.
   D. Avoid combination of background and character with large different luminance.

(3) Periodically adopt one of the following actions after long time display.
   A. Running the screen saver (motion picture or black pattern)
   B. Power off the system for a while

(4) LCD system is required to place in well-ventilated environment. Adapting active cooling system is highly recommended.

(5) Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions, such as high temperature/ humidity, display stationary patterns, or long operation time etc…, it is strongly recommended to contact AUO for filed application engineering advice. Otherwise, its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock market and controlling systems.

11.4 Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.

11.5 Precautions for Strong Light Exposure

(1) Strong light exposure causes degradation of polarizer and color filter.

(2) To keep display function well as a digital signage application, especially the component of TFT is very sensitive to sunlight, it is necessary to set up blocking device protecting panel

from radiation of ambient environment.

11.6 Storage

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.

(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

(3) Storage condition is guaranteed under packing conditions.

(4) The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition.

11.7 Handling Precautions for Protection Film

(1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.

(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.

(3) You can remove the glue easily. When the glue remains on the bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

11.8 Dust Resistance

(1) AUO module dust tests are conducted with marked areas (e.g., holes and slits around the front bezel and back cover) sealed, to comply with JIS D0207 (see Figure 1).

(2) To prevent particles from entering the module, please ensure the set has all the highlighted areas (holes and slits) adequately sealed or covered by set mechanism.

(3) AUO's testing procedure cannot replicate all real world operation scenarios. It is up to the module user to apply the most appropriate dust resistance solution for its particular application.

Fig TBD

