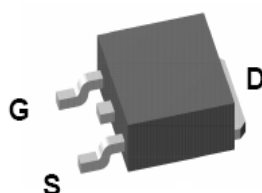


P2904BD

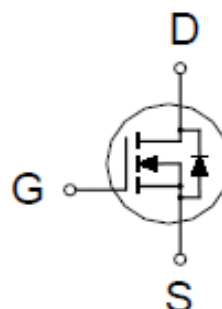
N-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
40V	29m Ω @ $V_{GS} = 10V$	25A



TO-252



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	$T_A = 25\text{ }^{\circ}\text{C}$	I_D	25	A
	$T_A = 70\text{ }^{\circ}\text{C}$		20	
Pulsed Drain Current ¹		I_{DM}	75	
Avalanche Current		I_{AS}	27	
Avalanche Energy ²		E_{AS}	37	mJ
Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	30	W
	$T_C = 70\text{ }^{\circ}\text{C}$		20	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		4.1	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		40	

¹Pulse width limited by maximum junction temperature.

P2904BD

N-Channel Logic Level Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

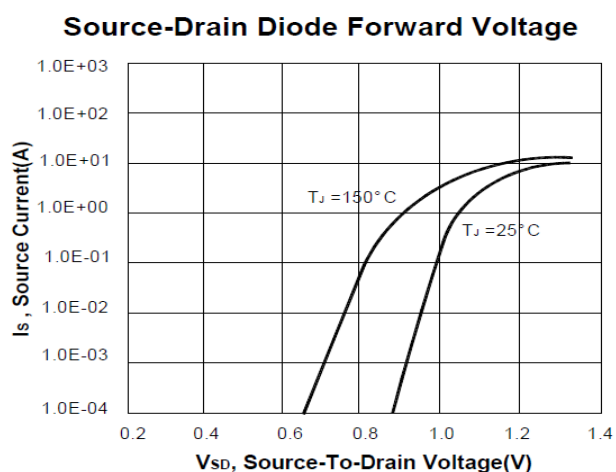
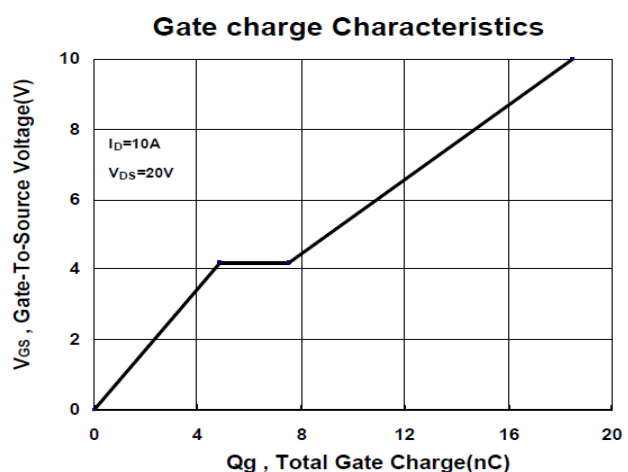
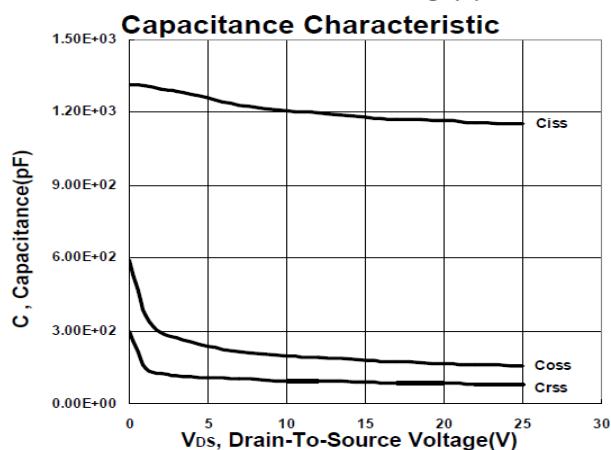
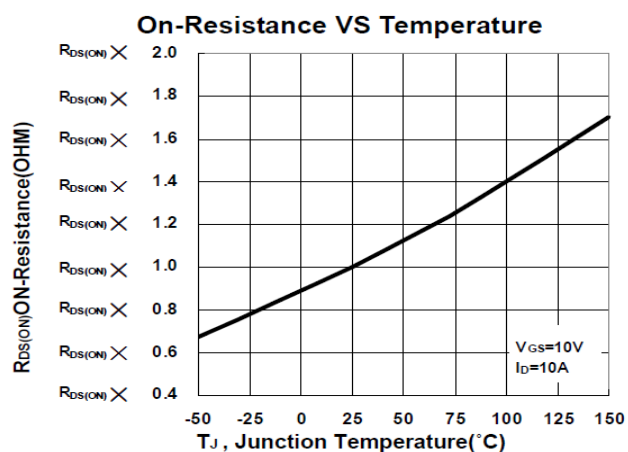
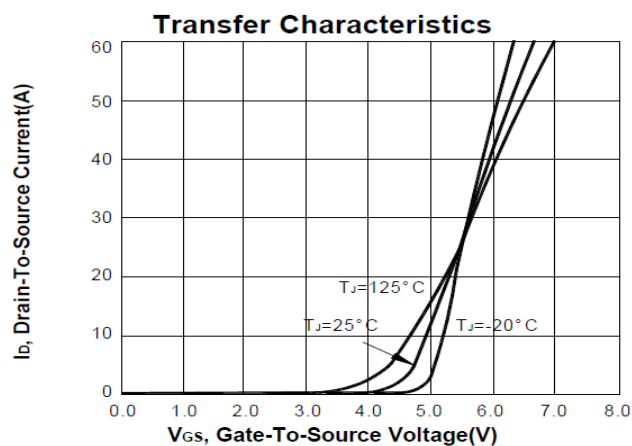
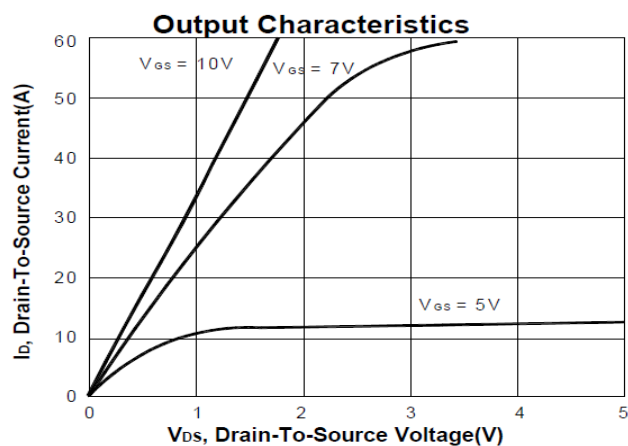
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT S
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	2.4	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 32V, V_{GS} = 0V$			1	μA
		$V_{DS} = 30V, V_{GS} = 0V, T_J = 125^\circ C$			10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	75			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 10A$		19	29	mΩ
		$V_{GS} = 7V, I_D = 8A$		22	45	
		$V_{GS} = 5V, I_D = 8A$		26	50	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 10A$		30		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 20V, f = 1MHz$		1150		pF
Output Capacitance	C_{oss}			157		
Reverse Transfer Capacitance	C_{rss}			80		
Total Gate Charge ²	Q_g	$V_{GS} = 10V$		19		nC
		$V_{GS} = 4.5V$		9		
Gate-Source Charge ²	Q_{gs}	$V_{DS} = 0.5V_{(BR)DSS}, I_D = 10A$		4.5		
Gate-Drain Charge ²	Q_{gd}			3		
Gate Resistance	R_g	$V_{GS} = 0V, V_{DS} = 0V, f = 1MHz$		1.55		Ω
Turn-On Delay Time ²	$t_{d(on)}$	$V_{DS} = 20V, R_L = 1\Omega$ $I_D \cong 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		10		nS
Rise Time ²	t_r			6		
Turn-Off Delay Time ²	$t_{d(off)}$			26		
Fall Time ²	t_f			6		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _J = 25 °C)						
Continuous Current	I_S				23	A
Forward Voltage ¹	V_{SD}	$I_F = 10A, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F = 10A, dI_F/dt = 100A/\mu s$		38		nS
Reverse Recovery Charge	Q_{rr}			29		nC

¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

P2904BD

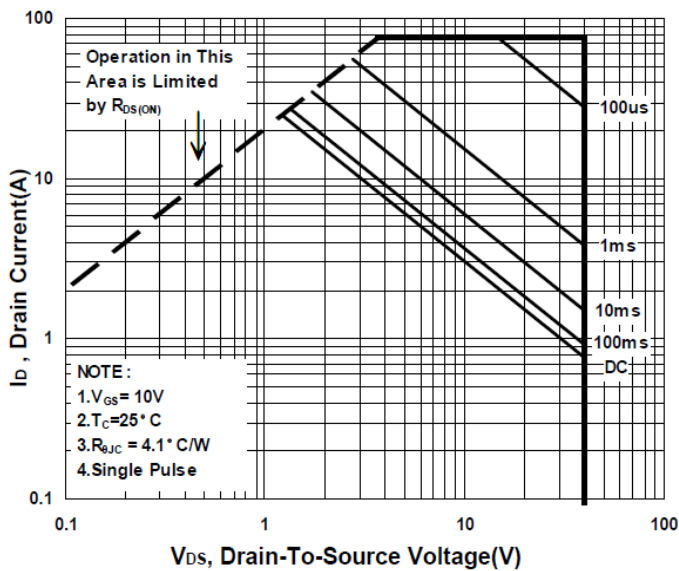
N-Channel Logic Level Enhancement Mode MOSFET



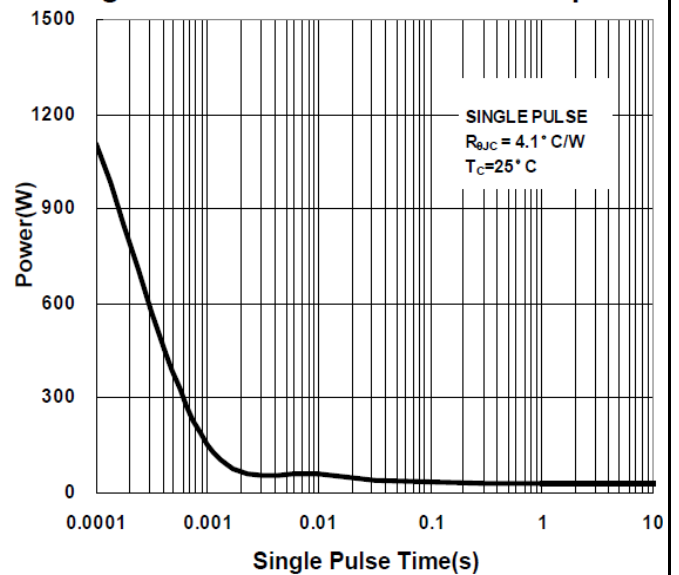
P2904BD

N-Channel Logic Level Enhancement Mode MOSFET

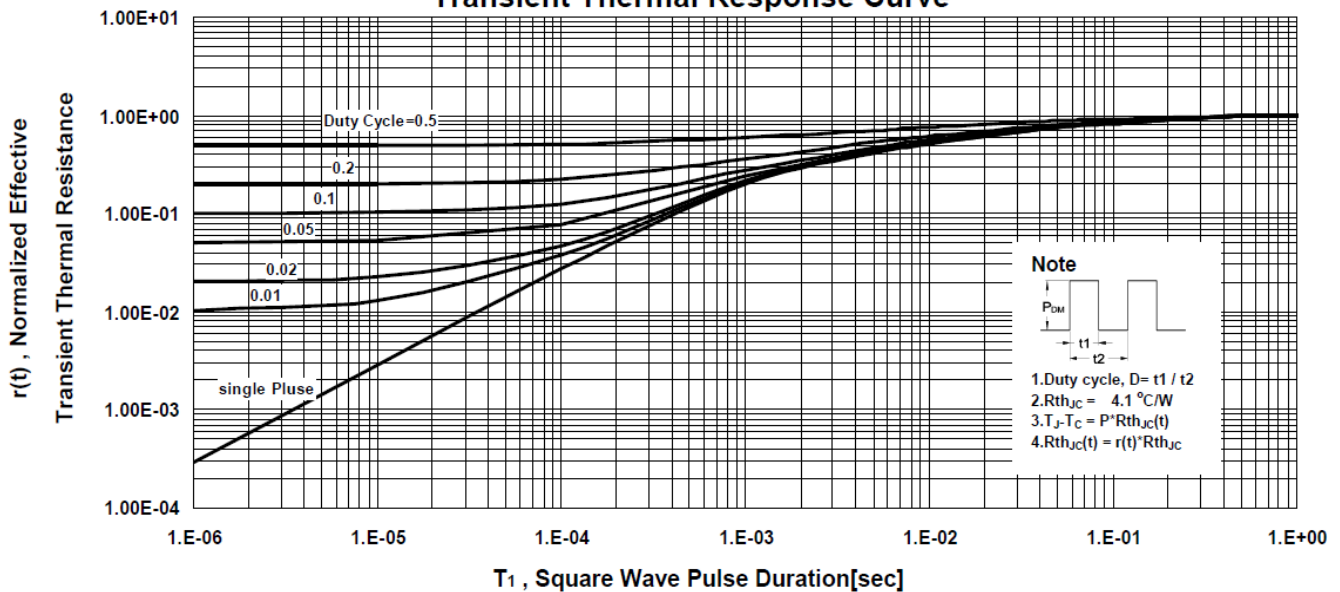
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



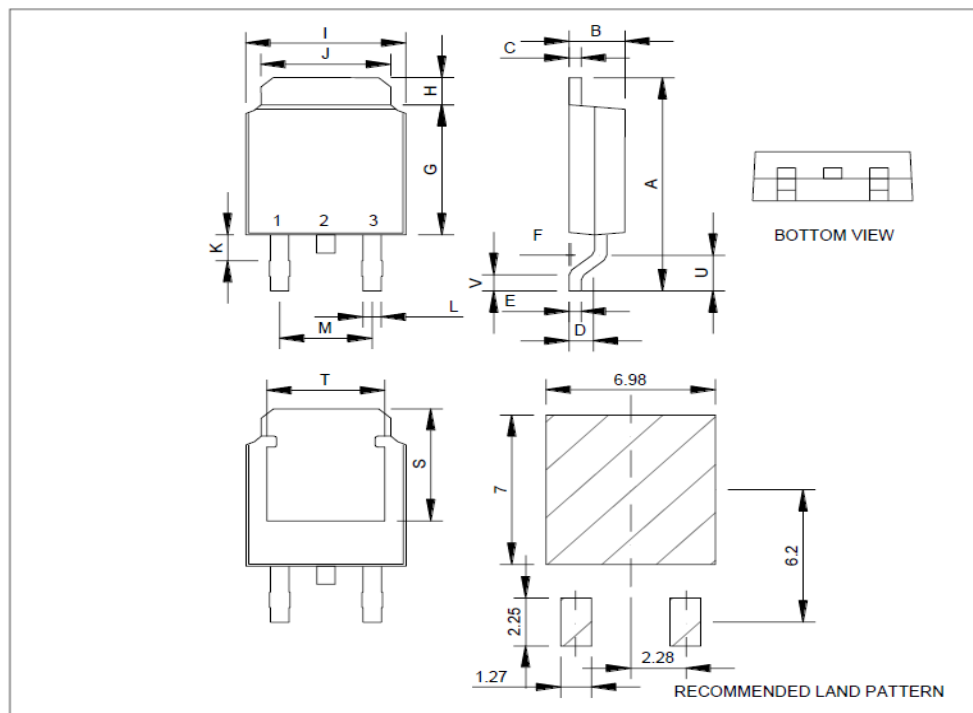
P2904BD

N-Channel Logic Level Enhancement Mode MOSFET

Package Dimension

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	10	10.41	J	4.8		5.64
B	2.1	2.2	2.4	K	0.15		1.1
C	0.4	0.5	0.61	L	0.4	0.76	0.89
D	0.82	1.2	1.5	M	4.2	4.58	5
E	0.4	0.5	0.61	S	4.9	5.1	5.3
F	0		0.2	T	4.6	4.75	5.44
G	5.3	6.1	6.3	U	1.4		1.78
H	0.9		1.7	V	0.55	1.25	1.7
I	6.3	6.5	6.8				



*因为各家封装模具不同而外观略有所差异，不影响电性及Layout。