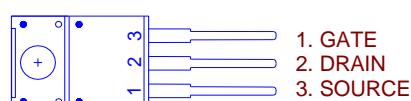
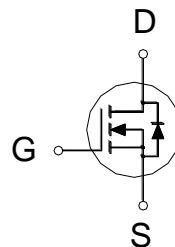


NIKO-SEM

N-Channel Enhancement Mode Field Effect Transistor
P0465CTF:TO-220F
P0465CTFS:TO-220FS
Halogen-Free & Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
650V	2.7Ω	4A

**100% UIS tested****ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current ²	$T_C = 25^\circ\text{C}$	I_D	4	A
	$T_C = 100^\circ\text{C}$		2.4	
Pulsed Drain Current ^{1, 2}		I_{DM}	15	
Avalanche Current ³		I_{AS}	2	
Avalanche Energy ³		E_{AS}	20	mJ
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	24	W
	$T_C = 100^\circ\text{C}$		9.8	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		5.1	°C / W
Junction-to-Ambient	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.²Limited only by maximum temperature allowed³ $V_{DD} = 50\text{V}$, $L = 10\text{mH}$, starting $T_J = 25^\circ\text{C}$ **ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$	650			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2.5	3.2	4.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 30\text{V}$			± 100	nA

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Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V, T_C = 25^\circ C$			10	μA
		$V_{DS} = 520V, V_{GS} = 0V, T_C = 100^\circ C$			100	
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 2A$		2.2	2.7	Ω
Forward Transconductance ¹	g_{fs}	$V_{DS} = 10V, I_D = 2A$		2.6		S

DYNAMIC

Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$		521		pF
Output Capacitance	C_{oss}			59		
Reverse Transfer Capacitance	C_{rss}			12		
Total Gate Charge ²	Q_g	$V_{DD} = 520V, I_D = 4A, V_{GS} = 10V$		14		nC
Gate-Source Charge ²	Q_{gs}			3.5		
Gate-Drain Charge ²	Q_{gd}			6		
Turn-On Delay Time ²	$t_{d(on)}$			28		
Rise Time ²	t_r	$V_{DD} = 325V, I_D = 4A, R_G = 25\Omega$		60		nS
Turn-Off Delay Time ²	$t_{d(off)}$			91		
Fall Time ²	t_f			75		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ C$)

Continuous Current ³	I_S			4	A
Forward Voltage ¹	V_{SD}	$I_F = 4A, V_{GS} = 0V$		1	V
Reverse Recovery Time	t_{rr}	$I_F = 4A, dI_F/dt = 100A/\mu S$		374	nS
Reverse Recovery Charge	Q_{rr}			3.1	μC

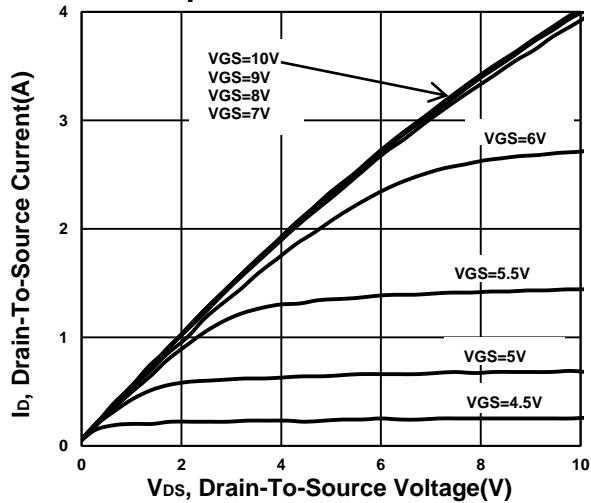
¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.³Pulse width limited by maximum junction temperature.

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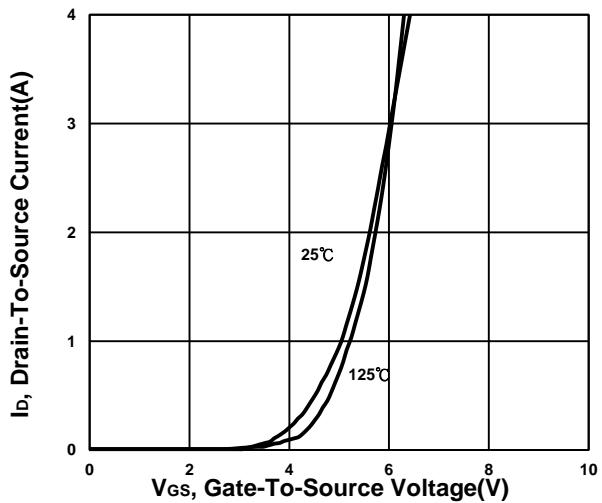
N-Channel Enhancement Mode Field Effect Transistor

**P0465CTF:TO-220F
P0465CTFS:TO-220FS
Halogen-Free & Lead-Free**

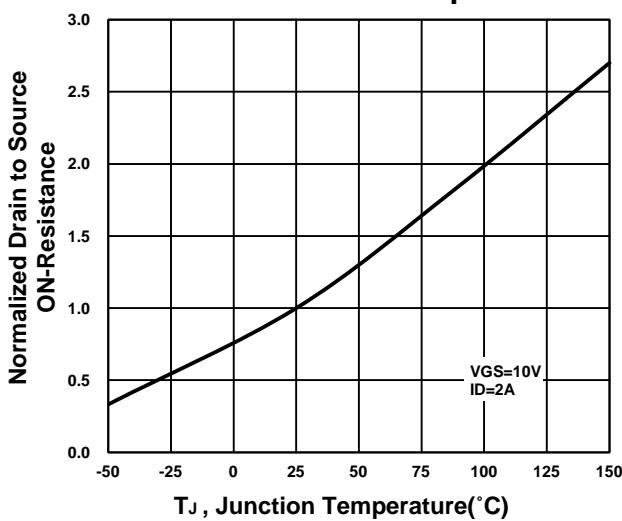
Output Characteristics



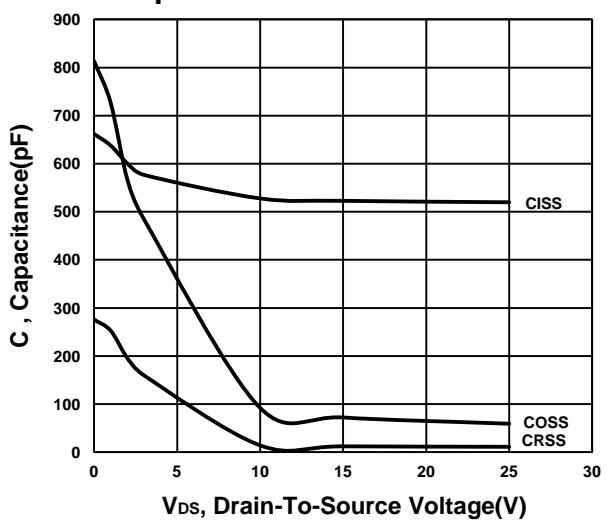
Transfer Characteristics



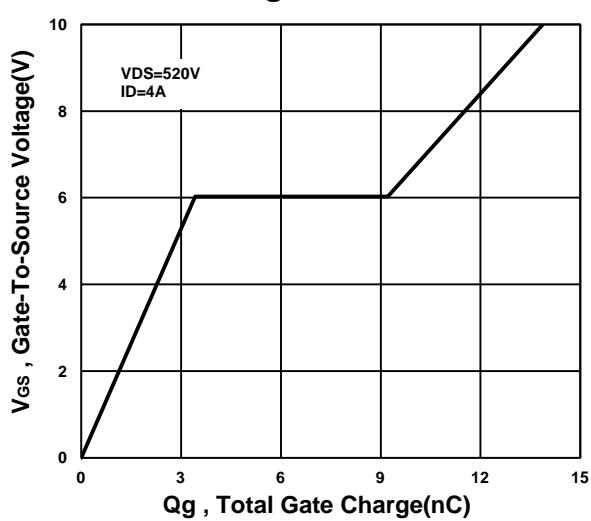
On-Resistance VS Temperature



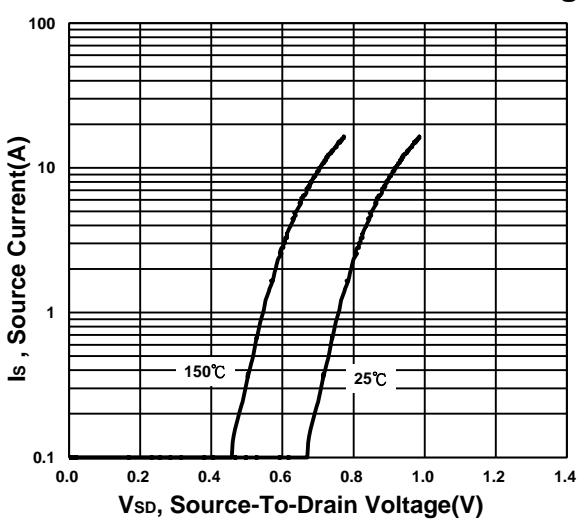
Capacitance Characteristic



Gate charge Characteristics



Source-Drain Diode Forward Voltage



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