Features

System Functions

- Programmable Signal Processing Platform with MOST® Network Interface
- Software available for Amplifier System including Digital Crossover, Parametric Equalizer, and Tone Controls
- Software available for Two-Way Active Speaker System
- Software available for Digital Radio

High System Integration

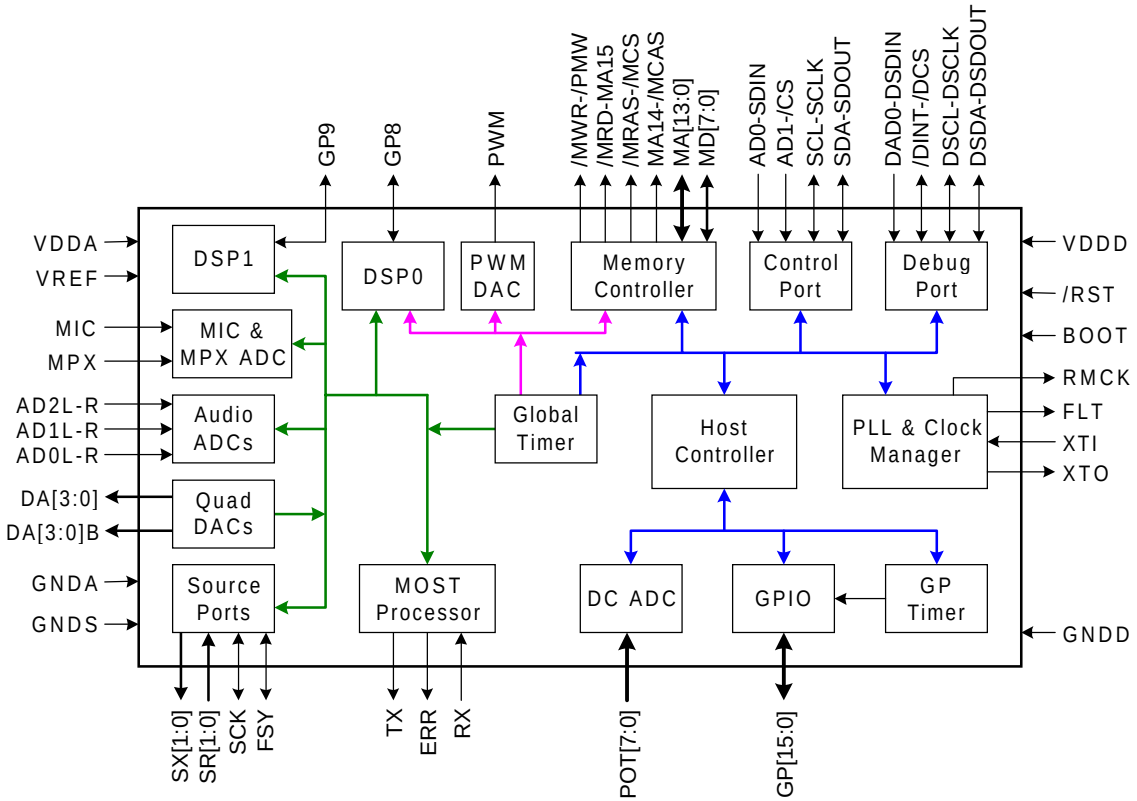
- MOST Core for Optical Networking
- Programmable 16-bit Host Controller
- Two Programmable Fixed-Point DSPs
- Quad Audio DACs with 103 dB Dynamic Range
- Stereo Audio ADCs with 98 dB Dynamic Range
- Microphone ADC for Voice Input
- MPX ADC for Radio Function
- Built-in DC Measurement ADC
- Built-in DRAM/SRAM Memory Controller
- Standard 128-pin MQFP Package

Description

The OS8804 is a highly integrated media processing system with a full-featured interface to the multimedia MOST Network. The MOST Network interface provides communication with, and control of, other equipment on the Network. The OS8804 operates in a 3.3 V environment with a temperature range of –40 °C to +85 °C.

The OS8804 is a programmable media processing system with built-in peripherals making it ideal for digital radio, amplifier, or active speaker systems. Proprietary sound processing algorithms can be implemented with the embedded DSPs.

On-chip stereo ADCs accepts audio inputs from existing sources such as AM-FM radio or other analog sources. Four channels of high-fidelity audio DACs provide analog outputs for passive speakers. The MPX ADC is suitable for implementation of various radio standards. The DC-measurement ADC provides an analog interface and the GPIO provide a digital interface to other system components. DSP0 also controls a PWM DAC which can support high-efficiency sub-woofer applications or a volume control for low-power applications.



Intellectual Property

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Patents

There are a number of patents and patents pending on the MOST technology. The rights to these patents are not granted without any specific Agreement between the users and the patent owners.

Product Overview

Product Overviews give a general description of products which are in development and subject to change. For complete information please see the Data Sheet for this product. Oasis SiliconSystems has worked diligently to ensure that the information in this document is accurate and reliable. However, the information in this document is subject to change without notice and is provided “as is” without warranty of any kind (expressed or implied).

Support and Further Information

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1 Overview

The OS8804 is a flexible hardware platform that can be programmed to support a wide variety of signal processing system solutions. Software is available from Oasis SiliconSystems for applications including digital radio, amplifiers, and active speakers. Programming tools such as simulators, emulators, assemblers, and C compilers are available to support user-developed applications.

The OS8804 is a monolithic CMOS integrated circuit, which combines high-speed micro-controllers and digital signal processors with high quality analog circuitry. It has four processors, ten ADCs and DACs, and a variety of digital I/O. The programmable Host Controller and fixed point DSPs enable the OS8804 to be a cost-effective solution for a wide variety of applications.

The MOST Processor provides a standard interface to the MOST Network. An internal clock manager provides all the timing for all components on the chip, which enables the entire chip to operate synchronously to the MOST Network. When the device is not connected to a MOST Network, the MOST Processor still provides an efficient means to route real-time data between resources such as the DSP, Source Ports, and Source Converters.

As shown in Figure 1-1, the chip contains three primary busses: the Control bus, the Routing bus, and the DSP I/O bus. The Control bus is managed by the Host Controller and communicates low-speed control information. The Routing bus is controlled by the MOST Processor and communicates high-speed source data. The DSP0 I/O bus connects DSP0 to the external memory controller for applications that require large amounts of data memory. Both DSPs connect to a MOST Routing Port and to a COM Port over their respective I/O busses (see Figure 1-2).

COM Ports provide bi-directional communications between the Host Controller and each DSP and the MOST Processor. Through the Control bus, the Host Controller also has access to the program controllers of each DSP and can download programs to DSP Program memory or disable the DSPs for minimum power consumption.

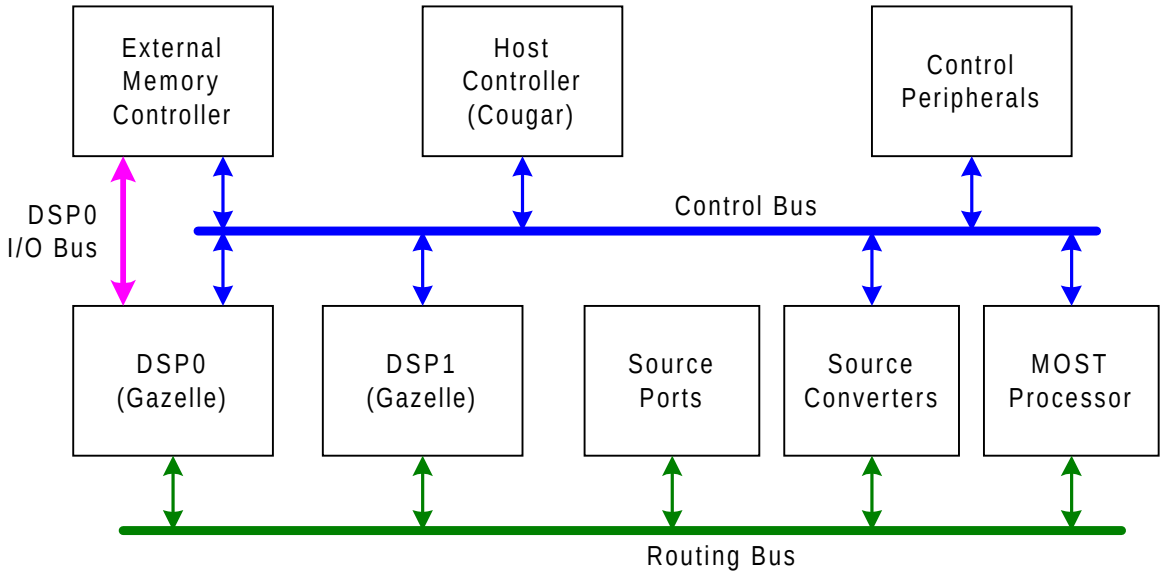

Figure 1-1: OS8804 *Block Diagram*

Peripherals such as the GPIO pins, Clock Manager, and the DC measurement ADC are connected to the Control bus and are managed by the Host Controller. The Control Port and Debug Port peripherals allow the Host Controller to communicate with external devices. The Source Converters are connected to both the Control and Routing busses, so that the Host Controller can enable the Converters and adjust the volume, while the high-speed MOST Processor routes the Source-Converter data across the Routing bus.

Each DSP has a local I/O bus with peripherals. These peripherals include the COM port to the Control bus, a MOST Routing Port to the Routing bus, and (for DSP0) a PWM DAC and an external memory port. The external memory port provides access to large amounts of DRAM or SRAM storage for DSP0. Figure 1-2 is a more detailed illustration of the three busses on the OS8804.

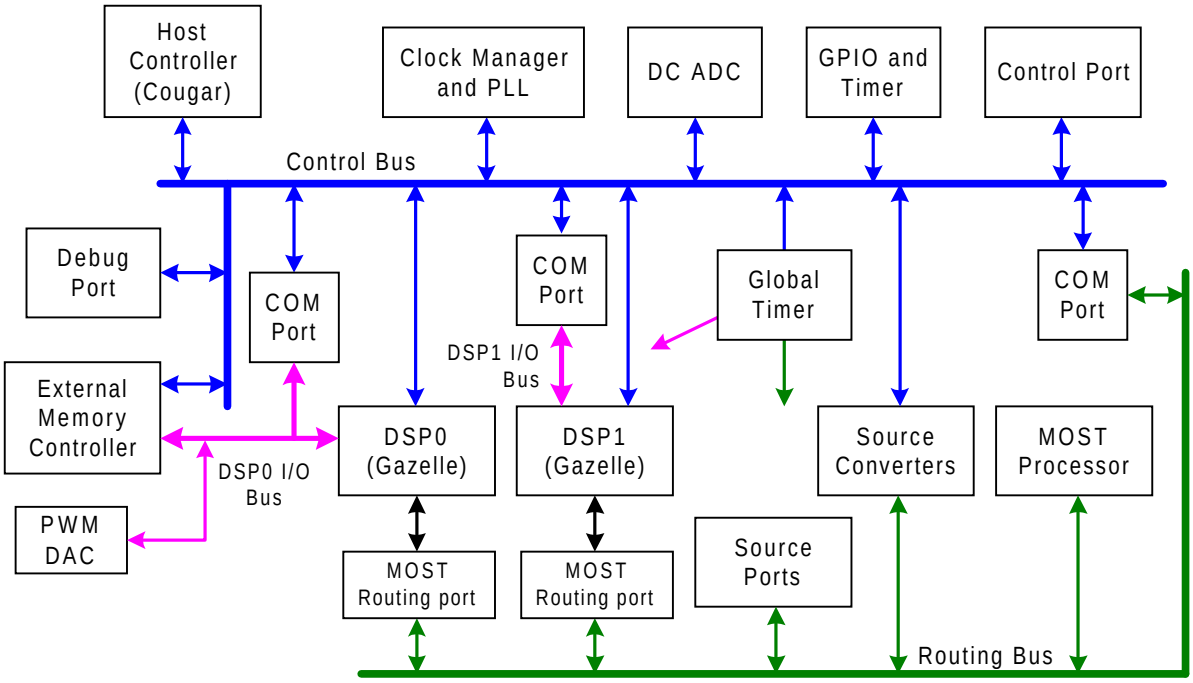

Figure 1-2: OS8804 *Bus Overview*

The MOST Processor includes a MOST Transceiver that provides compatibility to the MOST Network. The MOST Processor routes real time data between resources on and off chip. It operates as a cross-point switch, allowing data to stream over the Routing bus between the DSPs, Source Converters, Source Ports, and the MOST Network, as illustrated in Figure 1-3. The Routing bus has sufficient bandwidth to simultaneously route 15 high-fidelity stereo-audio channels on and off chip, through the devices on the Routing bus.

1.1 Host Controller

The Host Controller has multiple byte instructions and a CISC architecture, which minimizes the amount of program code required to perform control applications. A byte/word-mode switch enables it to efficiently process byte and word variables without wasting data RAM. The Controller operates at a maximum of 17 MIPS. Instructions can be one, two, or three bytes long. The first byte specifies the opcode and the following bytes provide an 8- or 16-bit direct memory address or immediate data.

The Host Controller can address up to 64k bytes of internal or external Program memory, and 2k bytes of internal data RAM for variables. NetServices software is available from Oasis SiliconSystems that runs on the Host Controller and manages both low- and high-level Network Protocol processing for the MOST Network.

1.2 Control Bus and Peripherals

The Host Controller manages the Control bus peripherals including a Control Port and Debug Port for communications with the external system, if present.

The Control Port is a slave device to the external system and provides a serial interface between the Host Controller and the external system. If the Host Controller needs servicing, a GPIO pin can signal the external system. The Control Port operates in one of three formats: I^2C, Oasis-specific SPI, or generic SPI format. In both I^2C and Oasis-specific SPI (OSPI), the data exchange between the external system and the Control Port starts with a byte that includes a 7-bit address and a R/W bit. When writing data to the chip, the first byte is considered the memory address pointer (MAP), and indicates where the rest of the data should be stored. When reading data from the Control Port, the previously written MAP is used to retrieve data. This data format supports efficient transfer of blocks of data. The generic SPI (GSPI) format does not interpret the data, leaving the data format up to the user.

The Debug Port is a second serial interface to the external system. Although listed as a “Debug” Port, the port is generic and supplies a secondary interface to the Host Controller. The Debug port has a unique interrupt vector that is not maskable. The Debug Port shares pins with three of the GPIO pins and supports the same three formats that the Control Port supports.

The Control bus also contains three COM Ports, supporting inter-processor communications between the Host Controller and the two DSPs as well as the MOST Processor. The MOST Processor communications utilize a format similar to the Control and Debug Port (MAP followed by data). The DSPs should be programmed to support the same format used by the MOST Processor to maximize code reuse. Through the MOST COM Port, the Host Controller can initialize the MOST Processor and transmit and receive messages across the MOST Network. The DSP COM Ports can be utilized in the same manner.

The Global Timer flag register supplies timing flags, at up to 8xFs, to synchronize communications across the processors. The DSPs and MOST Processor have access to the same register. The Global Timer also provides a periodic time interval, based on the sample frequency Fs.

The General Purpose I/O and Timer Port peripheral is connected to the external GPIO pins. Ten pins are dedicated to general-purpose I/O control (GP[9:0]). Three GPIO pins (GP[18:16]) are multiplexed with the Debug Port pins. GP19-BOOT provides an alternate start-up reset vector address for the Host Controller. Four of the GPIO pins (GP[15:12]) can generate interrupts in the Host Controller. Two of the interrupt pins (GP[13:12]) store the GPIO timer value in a capture register. The last two GPIO pins (GP[11:10]) can be configured as timer outputs and toggle the pin when a compare register matches the timer. The GPIO timer, is clocked at 64Fs and should not be confused with the Global Timer flag register mentioned above. The GP9 and GP8 pins can be controlled by DSP1 and DSP0, respectively.

The Clock Manager peripheral contains a PLL and generates all clocks needed for the OS8804. It also provides an external programmable clock (RMCK), to synchronize the external system devices. When the OS8804 is configured as a MOST Network slave device, the timing source is the MOST Network receive pin RX. When the OS8804 is configured as a MOST Network master, the timing source can be an external crystal, the external Source Port clock SCK, or the external Source Port data pin SR0 when configured as an SPDIF input.

The DC Measurement ADC peripheral consists of an eight-to-one mux and an over-sampling ADC. The resolution is programmable from 5 to 12 bits. The conversion process takes approximately 1 ms to achieve 12-bit resolution, and 250 µs to achieve 10-bit resolution. The POT[7:0] pins provide the eight analog inputs.

1.3 MOST Processor and Routing Bus Peripherals

The MOST Processor interfaces to the MOST optical Network and manages the transfer of real-time data between on-chip resources. Included in the MOST Processor is a MOST optical Network transmitter and receiver. The MOST receiver, in conjunction with the Clock Manager, recovers the clock, decodes the data, and passes the information to the MOST Processor. The transmitter accepts data from the Processor, encodes the data, and transmits it on the MOST Network.

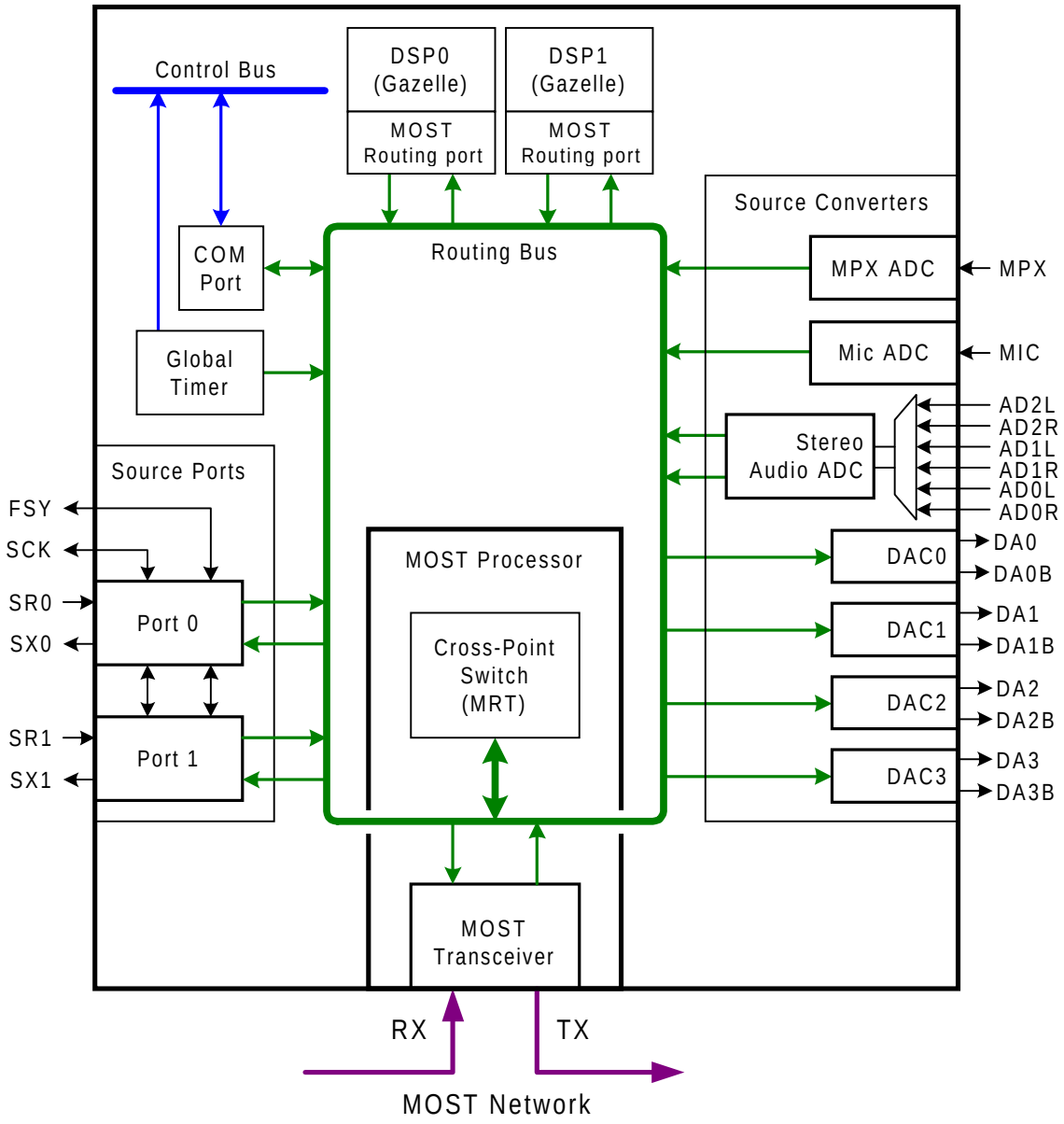

Figure 1-3: Routing Bus Block Diagram

The MOST Processor is a hard-coded RISC micro-controller, which routes data internally and onto the optical Network. For high-speed source data, the MOST Processor acts like a cross-point switch using the MOST Routing Table (MRT) to determine connections across the Routing bus. For low-speed data, such as control messages, it communicates with the Host Controller through the COM port. This port enables the Host Controller to instruct the MOST Processor to send and receive messages and to route the appropriate source data between the MOST Network and the on-chip resources.

The MOST Network can communicate 60 bytes of synchronous data (Source data) at the audio sample rate (Fs). The MOST Processor can route the received data back onto the Network, or (using the Routing bus) to the internal DSPs, Source Converters, or Source Ports. The transmitted MOST data can also come from the DSPs, Source Ports, and Source Converters. Each DSP can sink and source up to 16 bytes per Fs period (eight 16-bit channels). Each Source Port can sink and source up to 8 bytes per Fs period (four 16-bit channels).

The Source Converters consist of: the MPX ADC (16-bit samples at four times the audio sample rate), the stereo audio ADCs (two 16-bit samples at the audio sample rate), the microphone ADC (16-bit samples at ¼ the audio sample rate), and the audio DACs (four 16-bit samples at the audio sample rate).

The MOST transceiver uses the TX and RX pins for transmitting and receiving MOST optical Network data. The MOST Processor, Routing bus, and Routing bus peripherals are illustrated in Figure 1-3.

The Global Timer peripheral provides inter-processor synchronization. The MOST Processor uses the flags in this register to transfer data across the Routing bus. The DSPs can also use this register to synchronize with the MOST Processor when transferring data across the MOST Routing Port.

1.3.1 Source Data Ports

Two serial-input and two serial-output ports communicate source data between internal and external components. The data format is programmable via the SDC1 register in the MOST Processor I/O space. Data is clocked through all four ports in the same data format with the same clock and frame sync.

Data is serial shifted into and out of the Source Ports through the serial receive SR[1:0] and the serial transmit SX[1:0] pins. Source port 0 can be configured to transmit and receive SPDIF data (SX0 and SR0). If the OS8804 is configured as a MOST Network master, then the PLL can recover a clock from the SR0 bit stream when configured for SPDIF. If the chip is a slave, SPDIF data and serial source data must be entered synchronously. External synchronization can be achieved by using the OS8804 RMCK output as the master clock for the external system.

The Source Data Ports are accessed by the MOST Processor eight times per sample frequency. Therefore, a maximum of four 16-bit channels can be input to or sent out each Source Port.

1.3.2 Source Data Converters

The Source Converters are high-speed ADCs and DACs that reside on the Routing bus. The Source Converters consists of four audio-band DACs, two audio-band ADCs, a 4x audio-bandwidth MPX ADC, and a ¼x audio bandwidth microphone ADC. The MPX, audio, and microphone ADCs are over-sampling delta-sigma converters which provide wide dynamic range and excellent linearity. An analog MUX, in front of the audio ADCs, selects one of three stereo input pairs. All ADCs have input gain stages and all DACs have output attenuators. The Host Controller controls the ADC input MUX and the gain and attenuation settings through the Control bus.

The inputs to the ADCs are single ended and must be AC coupled. The MPX pin is the input to the MPX ADC and the MIC pin is the input to the microphone ADC. The two audio ADC inputs are AD0L-AD0R, AD1L-AD1R, or AD2L-AD2R pins, depending on the state of the input multiplexer.

The ADCs output their data to the Routing bus and MOST Processor. The MOST Processor can then route the data to the MOST transmitter to go out on the Network, route the data back to the DSPs for further processing, or route the data out the Source Data Port. Since the MPX ADC runs at 4xFs, the MOST Processor sends the 16-bit audio data to the Most Network four times per frame. Since the Mic ADC runs at ¼xFs, the MOST Network sees the same copy of Mic data four times before the next data is available.

The four DACs have differential outputs, which are available on the DA[3:0] and DA[3:0]B pins. Lower performance applications can use the DA[3:0] pins as single-ended outputs. The DACs are fed data from the Routing bus and MOST Processor. The MOST Processor can get the data from the MOST Network receiver, the DSPs, or the Source Data Ports.

1.4 DSP Processors

The two DSP cores have a RISC architecture, which provides the optimum cost performance trade-off for a wide variety of signal-processing applications. The RAM-based architecture allows software to be developed and downloaded for different system requirements. The DSP processor performs 18x14 bit operations with single-cycle instructions that produces 60 MIPs at 60 MHz. The right Vector memory and I/O register width are 18 bits and the left Vector memory width is 14 bits. A combination hardware/software stack provides high-speed interrupt servicing for high-priority interrupts and die-area-efficient servicing for low-priority interrupts. Special I/O instructions during high-priority interrupts provide low overhead I/O processing.

The Host Controller connects to the DSP's program controller and has read/write access to the program counter, the program control register, and Program memory. This feature allows downloading programs and visibility of the DSP internal operation through the Host Controller.

All the memories associated with the DSP processor are on-chip. The Program memory is 26 bits wide and 1280 locations deep. The data memory section is divided into left and right sides with each side having a Pointer RAM and a Vector RAM. Each Pointer RAM is 24 bits wide and both left and right Pointer RAMs are 32 locations deep. Left Vector/data RAM is 14 bits wide and 512 locations deep. Right Vector/data RAM is 18 bits wide and 512 locations deep.

The left and right Pointer RAMs store pointer values which consist of a 10-bit address, 6-bit update, and 8-bit modulo field. The accumulator consists of the low accumulator (14 bits), the high accumulator (18 bits), and the guard bits (4 bits).

The general purpose pins GP8 and GP9 can be controlled by either the Host Controller, or DSP1 can control GP9 and DSP0 can control GP8.

The MOST Routing Port peripheral supports the transfer of data between the DSP and the Routing bus. The MOST Processor can be programmed to transfer data (in either direction) between the Source Ports, Source Converters, or the MOST Network and the DSPs.

The DSP I/O bus contains the Global Timer flag register that provides periodic flags at up to 8xFs. These flags support inter-processor synchronization as the same Global Timer is available to the Host Controller and the MOST Processor. As an example, the MOST Processor reads and writes the DSP's MOST Routing port 8 times per sample period. The DSPs can use the Global timer GTR.FS8 flag to update the MOST Routing port. This process synchronizes data flow between the DSPs and the MOST Processor.

DSP0 has access to the external memory port, if not used by the Host Controller, which supports direct connections to DRAM or SRAM memory chips. This expands DSP0's data memory up to 512k 16-bit words, when using DRAM, and 16k 16-bit words, when using SRAM. External data communication occurs through 16-bit I/O registers and includes modulo and post-incrementing addressing features.

DSP0's I/O bus also includes a pulse-width-modulation (PWM) DAC peripheral for sub-woofer applications or low frequency volume control.

Notes: