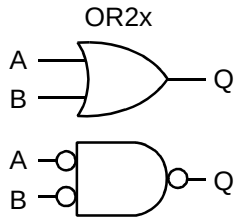
Description

OR2x is a family of 2-input gates which perform the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

HDL Syntax

Verilog ..... OR2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: OR2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	OR21	OR22	OR24	OR26
A	1.0	1.0	2.1	2.1
B	1.0	1.0	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR21	2.0	TBD	2.6
OR22	2.0	TBD	3.6
OR24	4.0	TBD	7.3
OR26	5.0	TBD	10.7

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OR21	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.21 0.28	0.30 0.39	0.42 0.53	0.56 0.69	0.68 0.81
OR22	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.23 0.32	0.34 0.48	0.43 0.61	0.53 0.71	0.65 0.82
OR24	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.21 0.31	0.31 0.45	0.40 0.57	0.49 0.68	0.59 0.78
OR26	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.24 0.39	0.35 0.55	0.44 0.67	0.52 0.78	0.61 0.88

Delay will vary with input conditions. See page 2-17 for interconnect estimates.