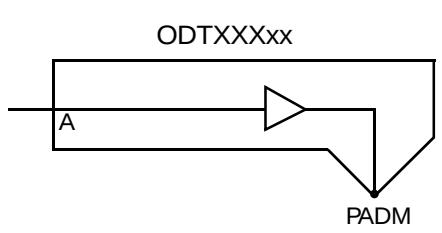


## AMI5HG 0.5 micron CMOS Gate Array

### Description

ODTXXXxx is a family of 1 to 24 mA, non-inverting, TTL-level output buffer pieces.

| Logic Symbol                                                                      | Truth Table                                                                                                      |   |      |   |   |   |   |
|-----------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|---|------|---|---|---|---|
|  | <table> <tr> <th>A</th><th>PADM</th></tr> <tr> <td>L</td><td>L</td></tr> <tr> <td>H</td><td>H</td></tr> </table> | A | PADM | L | L | H | H |
| A                                                                                 | PADM                                                                                                             |   |      |   |   |   |   |
| L                                                                                 | L                                                                                                                |   |      |   |   |   |   |
| H                                                                                 | H                                                                                                                |   |      |   |   |   |   |

### HDL Syntax

Verilog ..... ODTXXXxx *inst\_name* (PADM, A);

VHDL ..... *inst\_name*: ODTXXXxx port map (PADM, A);

### Pin Loading

| Pin Name    | Load     |          |          |          |          |          |          |
|-------------|----------|----------|----------|----------|----------|----------|----------|
|             | ODTXXX01 | ODTXXX02 | ODTXXX04 | ODTXXX08 | ODTXXX12 | ODTXXX16 | ODTXXX24 |
| A (eq-load) | 4.3      | 4.3      | 6.2      | 8.3      | 8.2      | 8.2      | 10.3     |

### Power Characteristics

| Cell     | Output Drive (mA) | Power Characteristics <sup>a</sup>                  |                             |
|----------|-------------------|-----------------------------------------------------|-----------------------------|
|          |                   | Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA) | EQL <sub>pd</sub> (Eq-load) |
| ODTXXX01 | 1                 | TBD                                                 | 149.5                       |
| ODTXXX02 | 2                 | TBD                                                 | 155.0                       |
| ODTXXX04 | 4                 | TBD                                                 | 165.6                       |
| ODTXXX08 | 8                 | TBD                                                 | 189.8                       |
| ODTXXX12 | 12                | TBD                                                 | 210.7                       |
| ODTXXX16 | 16                | TBD                                                 | 234.8                       |
| ODTXXX24 | 24                | TBD                                                 | 248.2                       |

a. See page 2-15 for power equation.

### Propagation Delays (ns)

Conditions: T<sub>J</sub> = 25°C, V<sub>DD</sub> = 5.0V, Typical Process

| ODTXXX01 | Capacitive Load (pF) |                  | 15   | 25    | 35    | 50    | 75 (max) |
|----------|----------------------|------------------|------|-------|-------|-------|----------|
|          | From: A              | t <sub>PLH</sub> | 2.52 | 3.69  | 4.86  | 6.58  | 9.33     |
|          | To: PADM             | t <sub>PHL</sub> | 7.11 | 10.44 | 13.76 | 18.75 | 27.11    |

## AMI5HG 0.5 micron CMOS Gate Array

Pad  
Logic

| ODTXXX02 | Capacitive Load (pF) |                                      | 15           | 50           | 75            | 100           | 150 (max)     |
|----------|----------------------|--------------------------------------|--------------|--------------|---------------|---------------|---------------|
|          | From: A<br>To: PADM  | t <sub>PLH</sub><br>t <sub>PHL</sub> | 1.63<br>3.87 | 3.59<br>9.51 | 4.99<br>13.53 | 6.38<br>17.54 | 9.20<br>25.55 |
| ODTXXX04 | Capacitive Load (pF) |                                      | 15           | 50           | 100           | 200           | 300 (max)     |
|          | From: A<br>To: PADM  | t <sub>PLH</sub><br>t <sub>PHL</sub> | 1.02<br>2.18 | 2.04<br>4.90 | 3.46<br>8.88  | 6.31<br>16.87 | 9.18<br>24.84 |
| ODTXXX08 | Capacitive Load (pF) |                                      | 15           | 50           | 100           | 200           | 300 (max)     |
|          | From: A<br>To: PADM  | t <sub>PLH</sub><br>t <sub>PHL</sub> | 0.91<br>1.50 | 1.45<br>2.87 | 2.15<br>4.82  | 3.57<br>8.75  | 5.02<br>12.69 |
| ODTXXX12 | Capacitive Load (pF) |                                      | 15           | 50           | 100           | 200           | 300 (max)     |
|          | From: A<br>To: PADM  | t <sub>PLH</sub><br>t <sub>PHL</sub> | 0.97<br>1.40 | 1.37<br>2.35 | 1.87<br>3.66  | 2.85<br>6.27  | 3.84<br>8.91  |
| ODTXXX16 | Capacitive Load (pF) |                                      | 15           | 50           | 100           | 200           | 300 (max)     |
|          | From: A<br>To: PADM  | t <sub>PLH</sub><br>t <sub>PHL</sub> | 1.10<br>1.59 | 1.41<br>2.33 | 1.80<br>3.33  | 2.58<br>5.29  | 3.34<br>7.24  |
| ODTXXX24 | Capacitive Load (pF) |                                      | 15           | 50           | 100           | 200           | 300 (max)     |
|          | From: A<br>To: PADM  | t <sub>PLH</sub><br>t <sub>PHL</sub> | 1.05<br>1.26 | 1.39<br>1.80 | 1.80<br>2.53  | 2.54<br>3.88  | 3.27<br>5.17  |

Delay will vary with input conditions. See page 2-17 for interconnect estimates.