

GENERAL DESCRIPTION

OBGZ11 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

PWM switching frequency at normal operation is internally fixed and is trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VCC low startup current and low operating current contribute to a reliable power on startup and low standby design with OBGZ11.

OBGZ11 offers comprehensive protection coverage with auto-recovery including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VCC under voltage lockout (UVLO), over temperature protection (OTP), and over voltage protection (OVP). Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 25KHz is minimized in the design and audio noise is eliminated during operation.

OBGZ11 is offered in SOT23-6 package.

APPLICATIONS

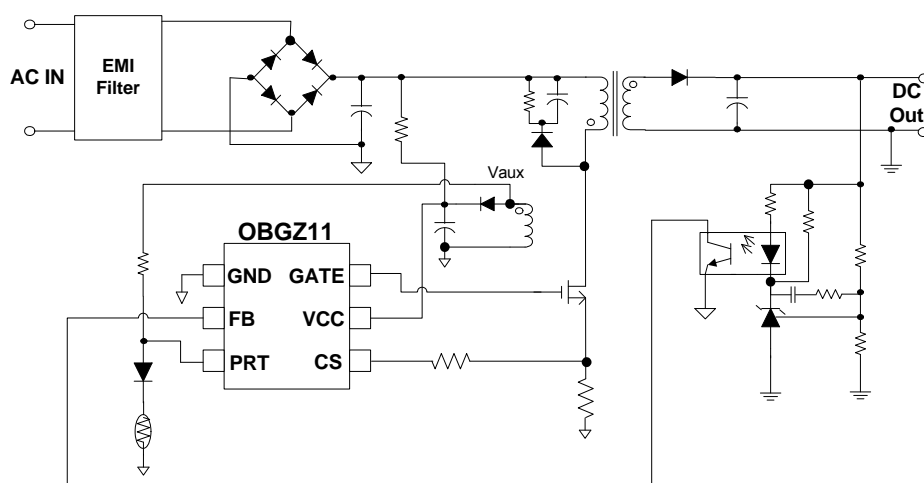
Offline AC/DC flyback converter for

- Printer, Storage power supply
- Power Adapter

FEATURES

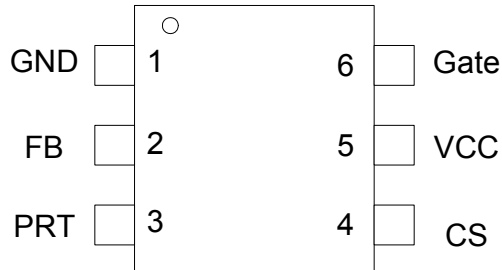
- Power on soft start reducing MOSFET Vds stress
- Frequency shuffling for EMI
- Extended burst mode control for improved efficiency and low standby power design
- Audio noise free operation
- Over Load operation with increased frequency
- Comprehensive protection coverage
 - VCC Under Voltage Lockout with hysteresis (UVLO)
 - VCC Over Voltage Protection (VCC OVP)
 - Cycle-by-cycle over current threshold setting for constant output power limiting over universal input voltage range
 - Over Load Protection (OLP) with auto-recovery
 - External (if NTC resistor is connected at PRT pin) or internal Over Temperature Protection (OTP)
 - Output Over Voltage Protection (Output OVP) and the OVP triggered voltage can be adjusted by the resistor connected between auxiliary winding and PRT pin
 - Output diode short protection with auto-recovery

TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration



Ordering Information

Part Number	Description
OBGZ11MP	SOT23-6, Halogen-free in T&R

Package Dissipation Rating

Package	R θ JA(°C/W)
SOT23-6	200

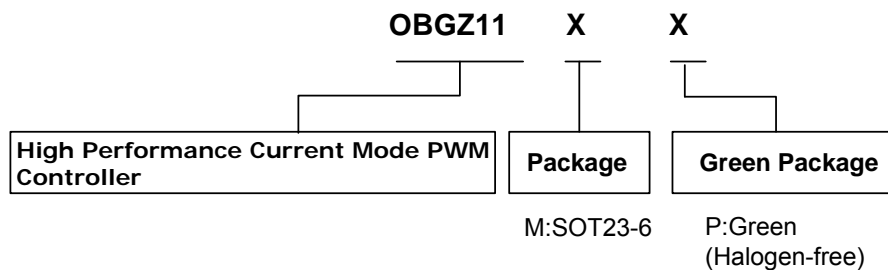
Recommended operating condition

Symbol	Parameter	Range
VCC	VCC Supply Voltage	12 to 26V

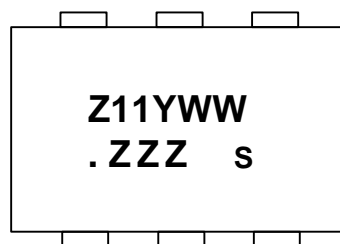
Absolute Maximum Ratings

Parameter	Value
VCC DC Supply Voltage	V _{OV} P-1V
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
PRT Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T _J	-40 to 150 °C
Operating Ambient Temperature T _A	-40 to 85 °C
Min/Max Storage Temperature T _{stg}	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



Marking Information

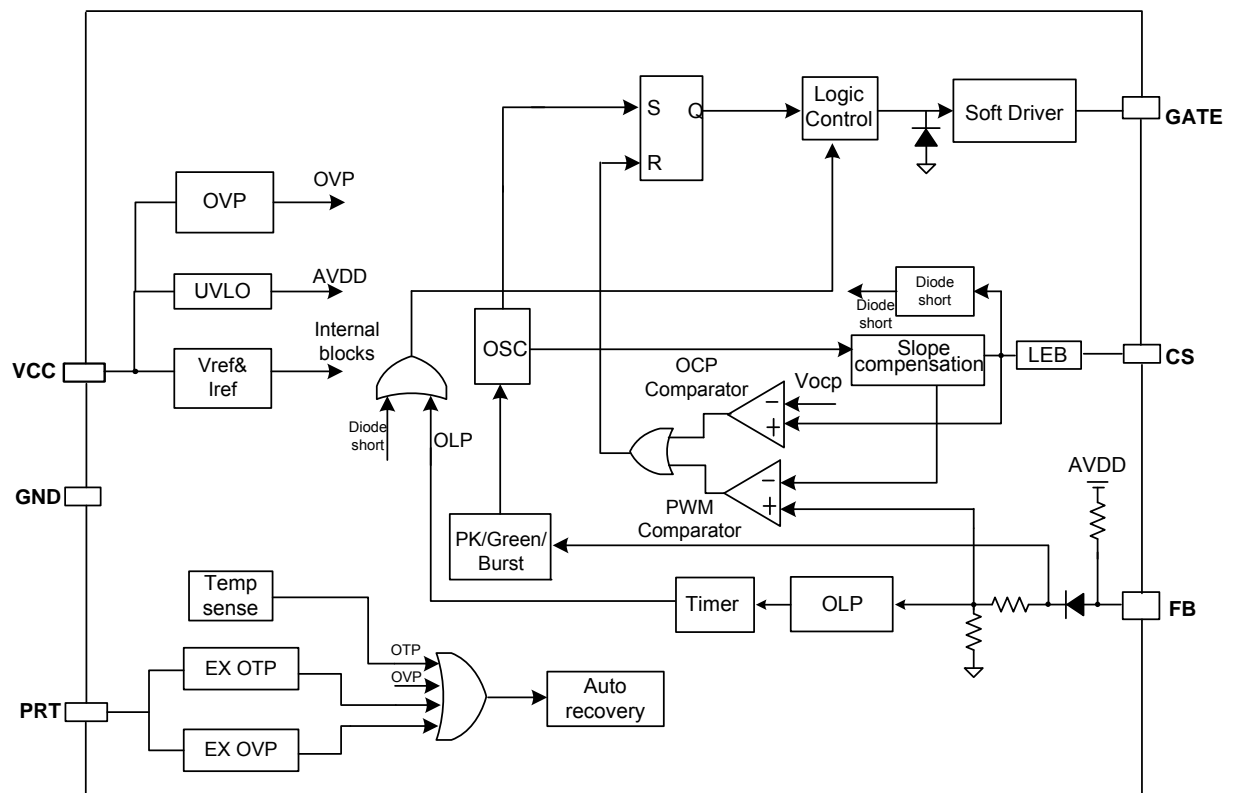


Y:Year Code
 WW:Week Code(01-52)
 S: Internal code
 ZZZ: Lot code

TERMINAL ASSIGNMENTS

Pin Name	I/O	Description
GND	P	Ground
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin CS.
PRT	I	Dual functions pin. Connecting a NTC resistor to ground for OTP detection. Connecting a resistor from Vaux can adjust OVP trigger voltage. If both OTP and OVP are needed, a diode should be connected between PRT pin and the NTC resistor.
CS	I	Current sense input
VCC	P	Power Supply
Gate	O	Totem-pole gate driver output for power MOSFET

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

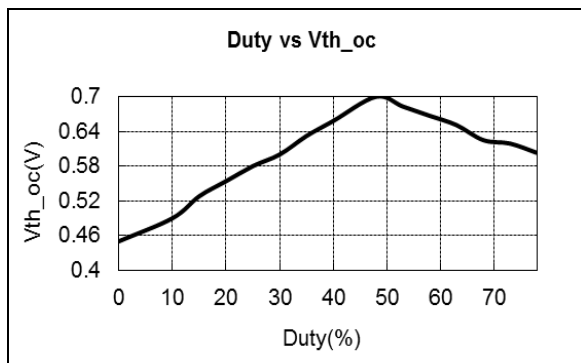
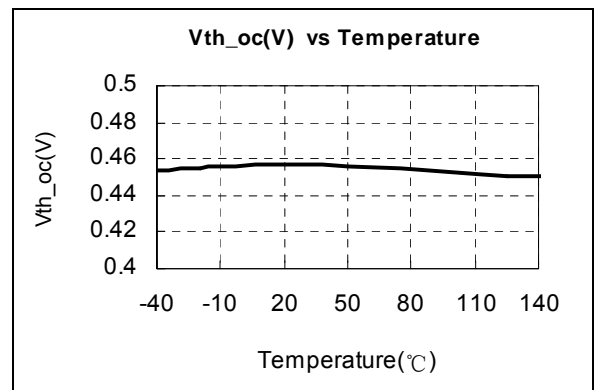
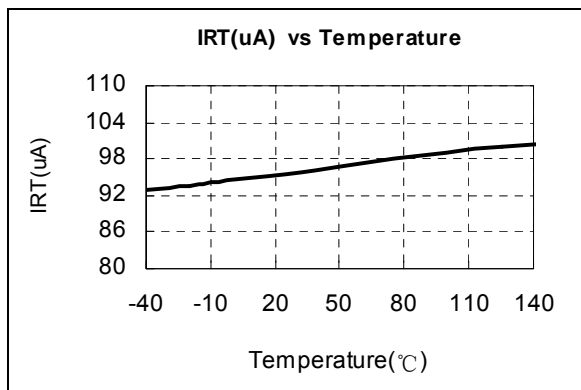
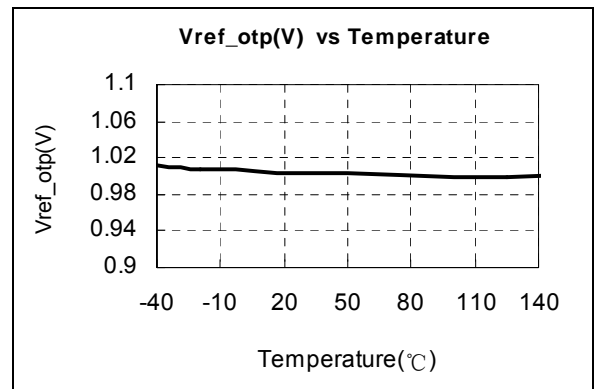
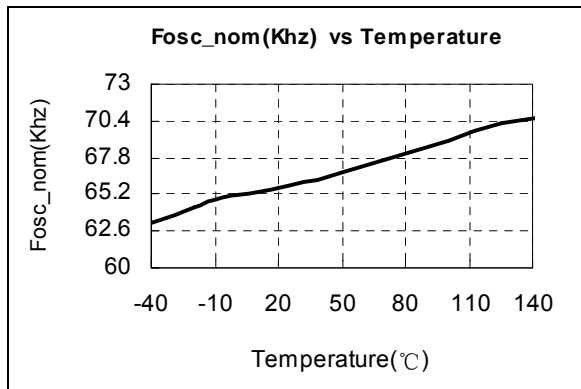
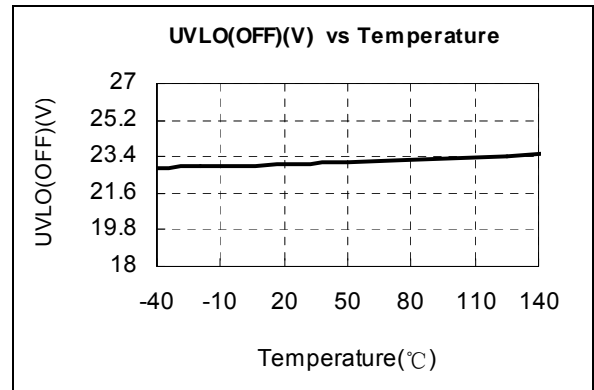
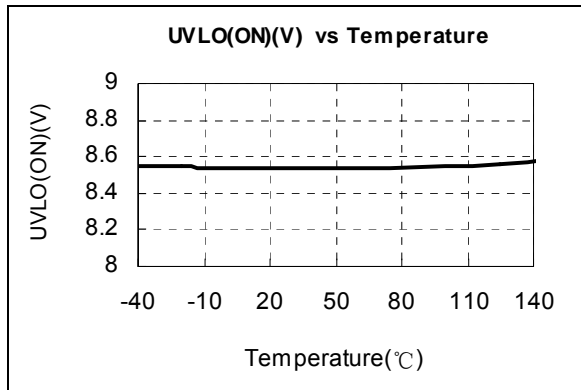
(T_A = 25°C, VCC=18V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VDD)						
I _{startup}	VCC Start up Current	VCC=UVLO(OFF)-1V, measure leakage current into VCC		2	5	uA
I _{VCC_Operation}	Operation Current	VDD=18V,CS=4V, FB=3.5V,measure I(VCC)		2.5	3	mA
I _{VCC_Burst}	Burst Current	CS=0V,FB=0.5V, measure I(VCC)		0.55	0.75	mA
UVLO(ON)	VCC Under Voltage Lockout Enter		6.5	7.3	8.1	V
UVLO(OFF)	VCC Under Voltage Lockout Exit (Recovery)		14.7	16.2	17.7	V
V _{pull-up}	Pull-up PMOS active			10		V
OVP	VCC Over Voltage Protection threshold voltage	FB=3V,CS=0V. Slowly ramp VCC, until no gate switching.	26.5	28	29.5	V
Feedback Input Section(FB Pin)						
V _{FB_Open}	V _{FB} Open Loop Voltage			5.1		V
A _{vcs}	PWM input gain $\Delta V_{FB}/\Delta V_{CS}$			3.5		V/V
Maximum duty cycle	Max duty cycle @ VCC=18V,VFB=3V,VCS=0V		75	80	85	%
V _{ref_green}	The threshold enter green mode			2.1		V
V _{ref_burst_H}	The threshold exits burst mode			1.33		V
V _{ref_burst_L}	The threshold enters burst mode			1.23		V
I _{FB_Short}	FB pin short circuit current	Short FB pin to GND and measure current		0.21		mA
V _{TH_OLP}	Open loop protection, FB Threshold Voltage			4.4		V
T _{d_OLP}	Open loop protection, Debounce Time			15		ms
Z _{FB_IN}	Input Impedance			30		KΩ
Current Sense Input(CS Pin)						
SST_CS	Soft start time for CS peak			4		ms
T _{blanking}	Leading edge blanking time			300		ns
T _{d_OC}	Over Current Detection and Control Delay	From Over Current Occurs till the Gate driver output start to turn off		90		ns
V _{TH_OC}	Internal Current Limiting Threshold Voltage with zero duty cycle		0.43	0.45	0.47	V
V _{TH_OC_Clap}	OCP CS voltage clamber			0.72		V
T _{d_OCP}	Over Current protection debounce Time			60		ms
PRT pin						

IRT	Output current for external OTP detection		92	100	108	uA
VOTP	Threshold voltage for external OTP		0.95	1	1.05	V
Ioutput_ovp	Current threshold for adjustable output OVP			60		uA
Td_output_ovp	Output OVP debounce time			5		Cycles
In-chip OTP						
OTP enter				150		°C
OTP exit				130		°C
Oscillator						
F _{OSC}	Normal Oscillation Frequency	VDD=18V,FB=3V, CS=0V	60	65	70	KHz
Fosc_PK	Peak frequency	VDD=18V,FB=4.5V, CS=0V		130		KHz
SST_freq	Soft start time of frequency			30		ms
Δf _{OSC}	Frequency jittering			+/-6		%
F _{shuffling}	Shuffling frequency			32		Hz
Δf _{Temp}	Frequency Temperature Stability			1		%
Δf _{VCC}	Frequency Voltage Stability			1		%
F _{Burst}	Burst Mode Switch Frequency			25		KHz
Gate driver						
VOL	Output low level @ VDD=18V, Io=5mA				1	V
VOH	Output high level @ VCC=18V, Io=20mA		6			V
V _{clamping}	Output clamp voltage			11.5		V
T _r	Output rising time 1.2V ~ 10.8V @ CL=1000pF			150		ns
T _f	Output falling time 10.8V ~ 1.2V @ CL=1000pF			50		ns

CHARACTERIZATION PLOTS

VDD = 18V, TA = 25°C condition applies if not otherwise noted.



OPERATION DESCRIPTION

OBGZ11 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications. The 'extended burst mode' control greatly reduces the standby power consumption and helps the design easier to meet the international power conservation requirements.

- **Startup Current and Start up Control**

Startup current of OBGZ11 is designed to be very low so that VCC could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

- **Operating Current**

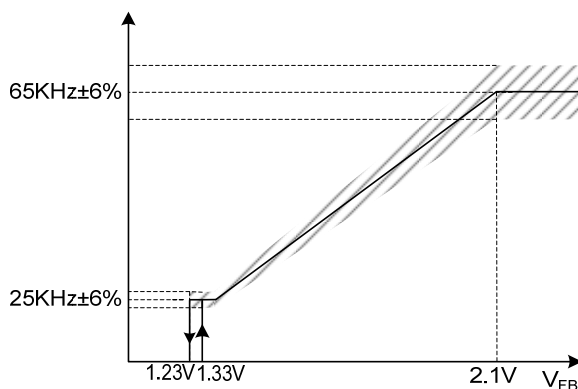
The Operating current of OBGZ11 is low at 2.5mA (typical). Good efficiency is achieved with OBGZ11 low operation current together with the 'extended burst mode' control features.

- **Soft Start**

OBGZ11 features an internal 4ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VCC reaches UVLO(OFF), the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

- **Frequency shuffling for EMI improvement**

The frequency shuffling (switching frequency modulation) is implemented in OBGZ11. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.



- **Extended Burst Mode Operation**

At light load or no load condition, most of the power dissipation in a switching mode power

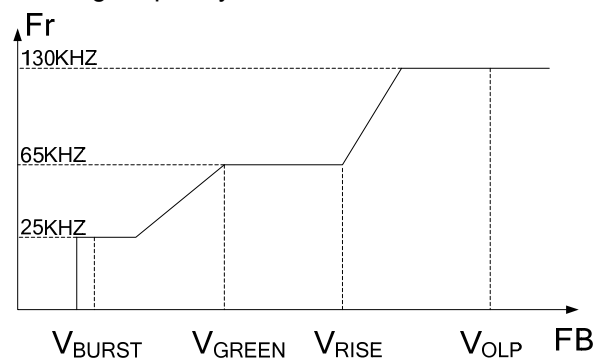
supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below $V_{ref_burst_L}$ (the threshold enter burst mode) and device enters Burst Mode control. The Gate drive output switches when FB input rises back to $V_{ref_burst_H}$ (the threshold exit burst mode). Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

- **Oscillator Operation**

During the full load power operation, OBGZ11 operates at a 65KHz (typical) fixed frequency. The efficiency and system cost is controlled at an optimal level. In over load mode, frequency is increased from 65KHz (typical) to 130KHz (typical).

At light load levels, OBGZ11 enters the light load mode, where the output current is reduced. The switching losses are reduced by lowering the switching frequency.



- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in OBGZ11 current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power

MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

● Internal Synchronized Slope Compensation

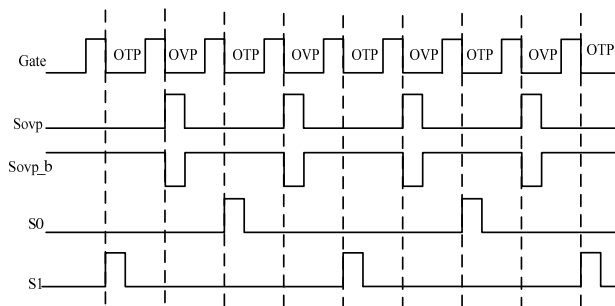
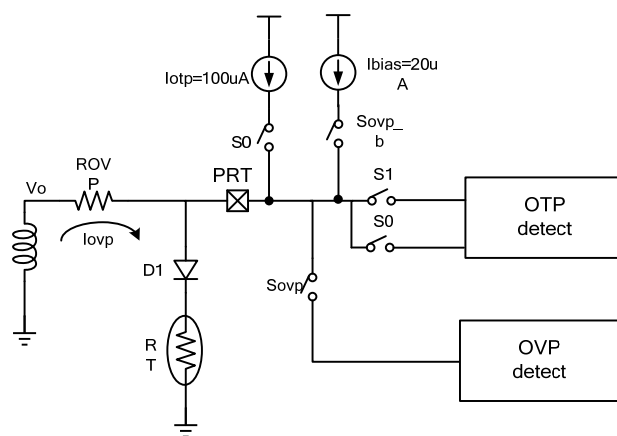
Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

● Driver

The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

● Dual Function of External OTP and Output OVP



On-Bright proprietary dual function of external OTP and output OVP provides feasible and accurate detection of external OTP through NTC resistor and output OVP. The dual function is realized through time-division technology as shown in the figure.

For external OTP detection, when switch control signal S1= "1", about 20uA (typical) current flows out from PRT pin. When switch control signal S0= "1", about 120uA (typical) current flows out from PRT pin. The PRT pin voltage difference ΔV_{otp} at phase S0 and S1 phase is equal to

$$\Delta V_{otp} = \frac{RT \cdot ROVP}{ROVP + RT} \cdot 100\mu A$$

When $\Delta V_{otp} < 1V$, external OTP protection is triggered after 60 Gate cycles debounce.

For output OVP detection, when Sovp= "1", lovp is equal to $V_o/ROVP$. If lovp is larger than 60uA (typical), OVP protection is triggered after 5 Gate cycles debounce. By selecting proper Rovp resistance, output OVP level can be programmed.

$$\frac{V_{out} * \frac{N_{aux}}{N_{out}} - 0.15V}{R_{ovp}} \geq 60\mu A$$

Vout: output voltage

Nout: the secondary winding turns

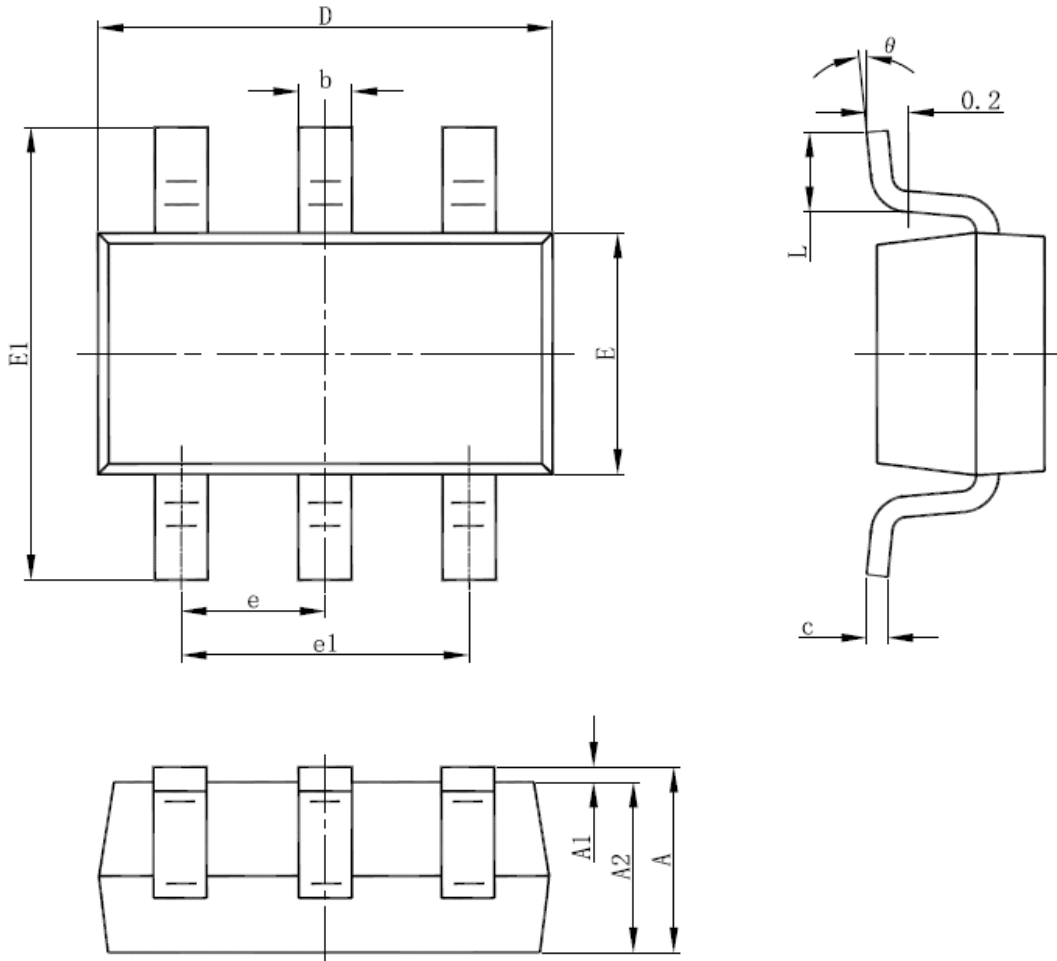
Naux: the auxiliary winding turns

● Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Under Voltage Lockout on VDD (UVLO), Over Temperature Protection (OTP), VCC and output Over Voltage Protection (OVP).

With On-Bright proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

At overload condition when FB input voltage exceeds power limit threshold value for more than Td_OLP, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit.

PACKAGE MECHANICAL DATA
SOT-23-6L PACKAGE OUTLINE DIMENSIONS


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
A2	0.900	1.300	0.035	0.051
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.800	3.020	0.110	0.119
E	1.500	1.726	0.059	0.068
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Revision History

File name	Date	Update information
OB_DOC_DS_GZ11A0	2016/08/31	First issue

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