

## **GENERAL DESCRIPTION**

OB6683 integrates a transition mode power factor correction (TM PFC) controller and a Quasi-Resonant (QR) controller in one chip. The PFC controller provides a cost effective solution for optimizing the power factor. The QR controller provides higher efficiency and lower EMI compared to conventional PWM system.

OB6683 provides high level integration and high performance than conventional PFC/PWM system. The built-in TM PFC controller optimizes power conversion efficiency with reduced system cost. The intelligent PFC switching ON and OFF, zero current detection and frequency limitation mechanism enable a better efficiency under any load conditions.

OB6683 features many built-in green functions to optimize power conversion efficiency at all power levels. This holds for QR operation at high power levels, as well as PFM operation at lower power levels, and 'Extended Burst Mode' operation at very low power or zero power (Standby) levels. At low power levels, OB6683 can turn off the PFC stage. In this way, low standby together with low system cost can be achieved.

The device is also integrated many functions of protection, such as X-CAP discharge, Brownin/out protection, VCC Under Voltage Lockout (UVLO), Cycle-by-Cycle Current Limiting for PFC and QR Stage (OCP), Output Over Voltage Protection for PFC and QR Stage (OVP), Open Loop Protection for PFC and QR Stage (OLP), Programmable Over Temperature Protection (OTP), Built-in Soft Start in QR Stage, VCC Over Voltage Protection, Gate Clamp, Pin Floating Protection, and External Latch Triggering, etc. Therefore it can protect the system from damage due to occasional failure.

OB6683 is offered in SOP-16 packages.

## FEATURES

- Integrated PFC Controller and QR Controller
- Transition Mode PFC Controller
- Multi-Mode Operation for QR Stage
- Line Voltage Compensation for QR Stage
- Enhanced Dynamic Response for PFC Stage
- PFC Light Load Turn Off Control
- Audio Noise Free Operation
- External Latch Triggering for Both Converters
- Minimum OFF time for Ringing Suppression
- Maximum ON Time Limit for QR Stage
- Built-in 4ms Soft Start for QR Stage
- Internal Leading Edge Blanking for QR Stage
- Internal Leading Edge Blanking for PFC Stage
- Built-in X-CAP Discharge

### PROTECTIONS

- Output Over Voltage Protection for PFC stage
- Output Over Voltage Protection for QR stage
- Output Diode Short Protection for QR stage
- VCC Over Voltage Protection
- Under Voltage Lockout with Hysteresis
- Over Load Protection for QR stage
  - Cycle-by-Cycle Current Limiting for PFC stage
  - Cycle-by-Cycle Current Limiting for QR stage
  - Brownout Protection (BOP)
  - Programmable Over Temperature Protection
  - Internal Over Temperature Protection

## APPLICATIONS

Offline AC/DC flyback converter for

- General LED Lighting
- LCD Monitor/TV/PC
- Notebook
- ACDC High Power Adapter
- Open Frame SMPS



# **TYPICAL APPLICATION**





## **GENERAL INFORMATION**

#### Pin Configuration

The pin map of OB6683 SOP16 package is shown as below.



### **Ordering Information**

Part Number	Description
OBEERSCOD	16 Pin SOP, Halogen free in
OB0003CGF	Tube
	16 Pin SOP, Halogen free in
UD0003CGPA	T&R

#### **Package Dissipation Rating**

<u> </u>		
Baakaga	R0JA	R0JC
Раскаде	(°C/W)	(℃/W)
SOP16	99	14

## **Marking Information**



## **Absolute Maximum Ratings**

Parameter	Value
HV input Voltage	-0.3 to 700V
VCC input Voltage	30V
FB Input Voltage	-0.3 to 7V
PRT Input Voltage	-0.3 to 7V
LATCH/OTP Input Voltage	-0.3 to 7V
COMP Input Input Voltage	-0.3 to 7V
PFCON/OFF Input Voltage	-0.3 to 7V
ZCD Input Voltage	-0.3 to 7V
PFCINV Input Voltage	-0.3 to 7V
TIMER Input Voltage	-0.3 to 7V
QRCS Input Voltage	-0.3 to 7V
PFCCS Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T <sub>J</sub>	<b>-40 to 150</b> ℃
Min/Max Storage Temperature T <sub>stg</sub>	<b>-55 to 150</b> ℃
Lead Temperature (Soldering, 10secs)	<b>260</b> ℃

**Note:** Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

### Recommended operating condition

Symbol	Parameter	Range
VCC	VCC Supply Voltage	12 to 25V







Y: Year Code

WW: Week Code (01-52)

ZZZ: Lot Code

P:Halogen-free

s: Internal code

## **TERMINAL ASSIGNMENTS**

Pin Num	Pin Name	I/O	Description
		-	Connected to the line input via resistors and diodes for startup and x-
1		I	cap discharge, this PIN allows the brownout detection as well.
2	NC		No connect.
		1	Feedback input pin. The PWM duty cycle of QR stage is determined by
3	ГВ	I	voltage level into this pin and the current-sense signal at QRCS pin
4	PRT		Zero current detection and over voltage protection for QR stage
5	LATCH/OTP	I/O	External latch protection pin.
6	COMP	I/O	Output of the error amplifier for PFC voltage loop compensation
7	PFCON/OFF	I/O	Threshold voltage setting for PFC ON/OFF loading control
8	ZCD		Zero current detection for PFC stage.
0		-	Inverting input of the error amplifier (EA). The information at the output
9	FFCINV	1	of the PFC stage is fed to the pin through a resistor divider.
10	TIMER	I/O	Timer setting for open loop protection and PFC light load turn off.
11	QRCS		QR stage current sense input pin.
12	PFCCS	Ι	PFC current sense input.
13	PFCGATE	0	PFC stage totem pole gate driver output.
14	QRGATE	0	QR stage totem pole gate driver output.
15	GND	Р	Ground
16	VCC	Ρ	Chip power supply pin.



# **BLOCK DIAGRAM**





# **ELECTRICAL CHARACTERISTICS**

### ( $T_A = 25^{\circ}C$ , VCC=20V if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit		
High Voltage Supply (HV pin)								
IHV1	High-Voltage Current Source for VCC startup	VCC =5V, Measure current into VCC	2			uA		
IHV2	High-Voltage Current Source for VCC startup	VCC=0.5V,Measure current into VCC			0.85	mA		
IHVXCAP	X-Cap Discharge Current			3		mA		
VBNI	Brown-in level	HV resistor=20k ohm		79		V		
VBNO	Brown-out level	HV resistor=20k ohm		70		V		
Supply Voltage (VC	CC pin)							
I_VCC_op	Operation current with switching	VDD=20V,FB=2V,measure I(VCC),when two gates switching		2.5		mA		
UVLO(ON)	VCC under voltage Lockout Enter		6.9	7.4	7.9	V		
UVLO(OFF)	VCC under voltage lockout exit		16.5	17.5	18.5	V		
VCC_OVP	VCC over voltage protection enter	Slowly ramp VCC, until no gate switching.	26.5	28	29.5	V		
TD_rst	Restart time for protection occurs			1.4		S		
PFCONOFF Voltag	e (PFCONOFF pin)		•	•		•		
I_PFCONOFF	Source current of PFCONOFF			100		uA		
V_PFCONOFF	PFCOFF voltage	R <sub>PFCONOFF</sub> =20K ohm		2.0		V		
<b>Over Temperature</b>	Protection (LATCH/OTP	pin)						
I_OTP	Output current of LATCH/OTP pin			100		uA		
VTH_OTP_in	OTP Enter Trip level			1.0		V		
V <sub>TH_OTP_off</sub>	OTP Exit Trip level			1.1		V		
On Chip OTP (Inter	rnal Thermal Shutdown)							
Tshutdown	OTP Level			150		°C		
Trecovery	OTP exit			125		°C		
PFC Section								
Error Amplifier								
Vinv	Voltage Feedback Input Threshold		2.46	2.50	2.54	V		
	Source current of PFCINV	VAC>180V			0.2	uA		
IIIV_SOUICe	Source current of PFCINV	VAC<150V		6		uA		
Gm	EA transconductance		170	200	230	uS		
	Max. EA output source							
	current under normal			20		uA		
lcomp	operation							
loomp	Max. EA output sink							
	current under normal		20		uA			
	operation							
Vcomp	Upper Clamp Voltage			5.2		V		
	Lower clamping voltage		0.85	0.95	1.05	V		
PFC MAX ON/ OFF	lime				T			
I on_ptc_max	Maximum on time		25	40	55	usec		



Toff of max	Maximum off time		40	60	80	lisec	
Current Sense Comparator (PEC CS pin)							
$\frac{1}{10000000000000000000000000000000000$							
Vth_OCP	Low AC Voltage input	VAC<150V		0.05		V	
	Figh AC voltage input	VAC>100V		0.45		V	
T_PFC_LEB	PFC leading edge			250		ns	
	blanking time						
Zero Current Detec	ction (ZCD pin)	F	1		1	1	
Vth_ZCD	ZCD demagnetization threshold voltage			1.2		V	
Vzcd_hys	ZCD detection			0.5		V	
SET PEC OFE debo	nysteresis voltage	ar)					
	PEC turn off dobounco				Τ		
Tpfc_off	time	R <sub>timerF</sub> =51K ohm		1		S	
PFC Over Voltage	Protection (PFC OVP)						
	INV threshold, PFC						
Vth_pfc_ovp	output over voltage		2.55	2.65	2.75	V	
	protection (OVP)						
Vpfc ovp hys	PFC OVP hysteresis			100		mV	
Gate Driver for PF	C (PFCDRIVER pin)		1		1	1	
VOL PEC	PEC OUT low level	lo = 30 mA			1	V	
VOL_ITO	PEC OUT high level	lo = 30  mA	7			V	
<u>von_</u> rro	PEC OUT clamping	10 = 30 IIIA	1			v	
V_Clamp_pfc	voltage	VCC=25V		11.7		V	
Tr_pfc	PFC_OUT rising time	CL= 1nF at PFC_OUT		80		nsec	
Tf_pfc	PFC_OUT falling time	CL= 1nF at PFC_OUT		20		nsec	
QR Section							
Feedback Input(FB	spin)						
VEB gain	VEBAACS			15		MM	
				4.0		V/V	
VFB Open	FB open loop voltage		4.5	5	5.5	V	
VFB_Open ZFB_IN	FB open loop voltage		4.5	4.5 5 2	5.5	V K Ohm	
VFB_Open ZFB_IN	FB open loop voltage Input impedance		4.5	4.5 5 2 1.45	5.5	V K Ohm	
VFB_Open ZFB_IN	FB open loop voltage Input impedance FB voltage in which		4.5	4.3 5 2 1.45	5.5	V K Ohm	
VFB_Open ZFB_IN VFB_pfm	FB open loop voltage Input impedance FB voltage in which system works in QR		4.5	4.5 5 2 1.45 ~	5.5	V K Ohm V	
VFB_Open ZFB_IN VFB_pfm	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode		4.5	4.5 5 2 1.45 ~ 2.45	5.5	V K Ohm V	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode		4.5	4.3 5 2 1.45 ~ 2.45 1.28	5.5	V K Ohm V V	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter		4.5	4.5 5 2 1.45 ~ 2.45 1.28	5.5	V K Ohm V V	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode		4.5	4.5 5 2 1.45 ~ 2.45 1.28 1.18	5.5	V K Ohm V V V	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L QR Current Sense	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode Comparator (QRCS pin)		4.5	4.3 5 2 1.45 ~ 2.45 1.28 1.18	5.5	V K Ohm V V V	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L QR Current Sense	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting		4.5	4.3 5 2 1.45 ~ 2.45 1.28 1.18	5.5	V K Ohm V V V	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L <b>QR Current Sense</b> V <sub>TH</sub> _OCP	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold		4.5	4.3 5 2 1.45 ~ 2.45 1.28 1.18	5.5	V K Ohm V V V	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L <b>QR Current Sense</b> V <sub>TH</sub> _OCP I_compensation	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS		4.5	4.3 5 2 1.45 ~ 2.45 1.28 1.18 0.5 100	5.5	V K Ohm V V V V	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L <b>QR Current Sense</b> V <sub>TH</sub> _OCP I_compensation T <sub>D</sub> _OC	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS QR OCP control delay	CL=1nF at QR_OUT	4.5	4.3 5 2 1.45 ~ 2.45 1.28 1.18 0.5 100	5.5	V K Ohm V V V V V uA nsec	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L <b>QR Current Sense</b> V <sub>TH</sub> _OCP I_compensation T <sub>D</sub> _OC	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS QR OCP control delay QB leading edge	CL=1nF at QR_OUT	4.5	4.5 5 2 1.45 ~ 2.45 1.28 1.18 0.5 100 100	5.5	V K Ohm V V V V U u A nsec	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L QR Current Sense V <sub>TH</sub> _OCP I_compensation T <sub>D</sub> _OC T_QR_LEB	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS QR OCP control delay QR leading edge blanking time	CL=1nF at QR_OUT	4.5	4.3 5 2 1.45 - 2.45 1.28 1.18 0.5 100 100 300	5.5	V K Ohm V V V V U U U U U U U U U U U N Sec	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L QR Current Sense V <sub>TH</sub> _OCP I_compensation T <sub>D</sub> _OC T_QR_LEB	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS QR OCP control delay QR leading edge blanking time	CL=1nF at QR_OUT	4.5	4.3 5 2 1.45 - 2.45 1.28 1.18 0.5 100 100 300	5.5	V K Ohm V V V V uA nsec nsec	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L <b>QR Current Sense</b> V <sub>TH</sub> _OCP I_compensation T <sub>D</sub> _OC T_QR_LEB <b>Demagnetization D</b>	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS QR OCP control delay QR leading edge blanking time	CL=1nF at QR_OUT	4.5	4.3 5 2 1.45 ~ 2.45 1.28 1.18 0.5 100 100 300	5.5	V K Ohm V V V V uA nsec nsec	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L <b>QR Current Sense</b> V <sub>TH</sub> _OCP I_compensation T <sub>D</sub> _OC T_QR_LEB <b>Demagnetization D</b>	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS QR OCP control delay QR leading edge blanking time <b>etection (PRT pin)</b> Demagnetization	CL=1nF at QR_OUT	4.5	4.3 5 2 1.45 ~ 2.45 1.28 1.18 0.5 100 100 300	5.5	V K Ohm V V V V V uA nsec nsec	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L <b>QR Current Sense</b> V <sub>TH</sub> _OCP I_compensation T <sub>D</sub> _OC T_QR_LEB <b>Demagnetization D</b> Voutput_ovp	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS QR OCP control delay QR leading edge blanking time <b>Demagnetization</b> comparator threshold voltage	CL=1nF at QR_OUT	4.5 	4.3 5 2 1.45 ~ 2.45 1.28 1.18 0.5 100 100 300	5.5	V K Ohm V V V V uA nsec nsec	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L <b>QR Current Sense</b> V <sub>TH</sub> _OCP I_compensation T <sub>D</sub> _OC T_QR_LEB <b>Demagnetization D</b> Voutput_ovp	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS QR OCP control delay QR leading edge blanking time <b>Detection (PRT pin)</b> Demagnetization comparator threshold voltage	CL=1nF at QR_OUT	4.5 	4.3 5 2 1.45 ~ 2.45 1.28 1.18 0.5 100 100 300	5.5	V K Ohm V V V V uA nsec nsec	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L QR Current Sense V <sub>TH</sub> _OCP I_compensation T <sub>D</sub> _OC T_QR_LEB Demagnetization D Voutput_ovp Td_output_ovp	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS QR OCP control delay QR leading edge blanking time <b>etection (PRT pin)</b> Demagnetization comparator threshold voltage Hysteresis for PRT OVP comparator	CL=1nF at QR_OUT	4.5	4.3 5 2 1.45 - 2.45 1.28 1.18 0.5 100 100 300 300	5.5	V K Ohm V V V V V uA nsec nsec v V Cycles	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L QR Current Sense V <sub>TH</sub> _OCP I_compensation T <sub>D</sub> _OC T_QR_LEB Demagnetization D Voutput_ovp Td_output_ovp	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS QR OCP control delay QR leading edge blanking time <b>etection (PRT pin)</b> Demagnetization comparator threshold voltage Hysteresis for PRT OVP comparator	CL=1nF at QR_OUT	4.5	4.3 5 2 1.45 - 2.45 1.28 1.18 0.5 100 100 300 3 3 7	5.5	V K Ohm V V V V V uA nsec nsec V V Cycles	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L QR Current Sense V <sub>TH</sub> _OCP I_compensation T <sub>D</sub> _OC T_QR_LEB Demagnetization D Voutput_ovp Td_output_ovp	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS QR OCP control delay QR leading edge blanking time <b>Petection (PRT pin)</b> Demagnetization comparator threshold voltage Hysteresis for PRT OVP comparator Suppression of the transformer ringing at	CL=1nF at QR_OUT	4.5	4.3 5 2 1.45 2.45 1.28 1.18 0.5 100 100 300 3 3 7	5.5	V K Ohm V V V V V uA nsec nsec V V Cycles	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L <b>QR Current Sense</b> V <sub>TH</sub> _OCP I_compensation T <sub>D</sub> _OC T_QR_LEB <b>Demagnetization D</b> Voutput_ovp Td_output_ovp	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS QR OCP control delay QR leading edge blanking time <b>Petection (PRT pin)</b> Demagnetization comparator threshold voltage Hysteresis for PRT OVP comparator Suppression of the transformer ringing at start of QR secondary	CL=1nF at QR_OUT	4.5	4.3 5 2 1.45 2.45 1.28 1.18 0.5 100 100 300 300 3 7 2.2	5.5	V K Ohm V V V V V uA nsec nsec V Cycles us	
VFB_Open ZFB_IN VFB_pfm Vth_burst_H Vth_burst_L <b>QR Current Sense</b> V <sub>TH</sub> _OCP I_compensation T <sub>D</sub> _OC T_QR_LEB <b>Demagnetization D</b> Voutput_ovp Td_output_ovp Td_ovp_blanking	FB open loop voltage Input impedance FB voltage in which system works in QR PFM mode The threshold exit burst mode The threshold enter burst mode <b>Comparator (QRCS pin)</b> internal current limiting threshold Only High AC flow into CS QR OCP control delay QR leading edge blanking time <b>Demagnetization</b> comparator threshold voltage Hysteresis for PRT OVP comparator Suppression of the transformer ringing at start of QR secondary stroke	CL=1nF at QR_OUT	4.5	4.3   5   2   1.45   ~   2.45   1.28   1.18   0.5   100   300   3   7   2.2	5.5	V K Ohm V V V V V uA nsec nsec V Cycles us	



V <sub>vally</sub>	Valley detection threshold			80		mV
Voutshort	The threshold of output short			0.75		V
Oscillator						
F _burst	Burst mode switching frequency			22		KHz
F_QR_max	Maximum QR frequency			130		KHz
F_QR_min	Minimum QR frequency			50		KHz
Ton_qr_max	Maximum on time			15		usec
QR Soft Start						
Tss	QR soft startup time			4.0		msec
QR Over Load Prot	tection (QR OLP)					
V <sub>TH</sub> _PL	Power Limiting FB Threshold Voltage			4.4		V
T <sub>D</sub> _PL	Power limiting Debounce Time			60		msec
Gate Driver for QR	(QR_OUT pin)					
VOL_QR	QR_OUT low level	lo = 30 mA			1	V
VOH_QR	QR_OUT high level	lo = 30 mA	7			V
V_Clamp_qr	QR_OUT clamping voltage	VCC=25V		11.7		V
Tr_qr	QR_OUT rising time	CL = 1nF at QR_OUT		200		nsec
Tf_qr	QR_OUT falling time	CL= 1nF at QR_OUT		50		nsec



# CHARACTERIZATION PLOTS



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## **OPERATION DESCRIPTION**

#### • GENERAL CONTROL AND FEATURE

# Integrated TM PFC Controller and QR Controller in One Chip

OB6683 integrates a transition mode power factor collection (TM PFC) controller and a quasi-resonant (QR) controller in one chip.

In TM PFC control, the inductor current is allowed to completely go to zero before the next switching cycle of the power MOSFET is initiated. Therefore, the reverse recovery loss of output boost diode is minimized. Also TM PFC can provide low harmonic distortion and high power factor.

Quasi-Resonant (QR) control can provide lower EMI and higher power conversion efficiency compared to conventional hard-switched converter with a fixed switching frequency.

The built-in advanced energy saving with high level protection features of OB6683 provide simple and cost effective solutions for the power supplies of 75 Watts or greater.

# Internal High-Voltage Startup Circuit and UVLO

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes too much power to meet the power saving requirement. OB6683 is implemented with a high-voltage startup circuit to minimize power loss on startup circuit. During a startup phase, a high voltage current source sinks current from AC Line or Neutral to provide the startup current and charge the VCC capacitor. The resistor connected to HV recommended for 20K.

An UVLO comparator is embedded to detect the voltage across VCC pin to ensure the supply voltage is high enough to power on the OB6683 and in addition to drive the power MOSFET.A hysteresis is provided to prevent the OB6683 shutdown by the voltage dip during startup

# Over Temperature Protection with Latch Shutdown (LATCH/OTP pin)

A NTC resistor in series with a regular resistor should be connected between LATCH/OTP pin and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal 100uA current source flowing through the resistors, the voltage at LATCH/OTP pin becomes lower at high temperature. The internal OTP circuit is triggered and shuts down the MOSFET when the sensed input voltage is lower than 1.0V. OTP is a latched shutdown.

#### External latch trip point

By externally forcing a level on pin LATCH/OTP (e.g.., with a signal coming from a temperature sensor) less than 1.0V, OB6683 can be permanently latched-off.

# • FUNCTIONAL DESCRIPTION for TM PFC Error Amplifier

Connected to a resistor divider from output line, the inverting input of the Error Amplifier (EA) is compared to an internal reference voltage (2.5V) to set the regulation on output voltage.

The EA output is externally connected for loop compensation. It is usually realized with a type II filter which connected between the ground and EA output. The system loop bandwidth is set below 20 Hz to suppress the AC ripple of the line voltage.

#### Zero Current Detection (ZCD pin)

OB6683 performs zero current detection (ZCD) by using an auxiliary winding of the PFC boost inductor in series with an external resistor. When the stored energy of the PFC boost inductor is fully released to the output, the voltage at ZCD pin decreases. When ZCD pin voltage falls below 1.2V, an internal ZCD comparator is triggered and a new PFC switching cycle is initiated following the ZCD triggering. If no zero current triggering signal is detected on ZCD pin, OB66683 will generate a restart signal in 60 usec (typ.) after the last PFC driver signal.

#### **Output Overvoltage Protection**

OB6683 offers two level OVP protection including dynamic OVP for output fast transient protection and static OVP for output stead-state protection.

When output voltage exceeds 424V which correspond to a INV voltage larger than 2.65V, the GATE output is turned off and OB6683 is disabled. Only when INV voltage reach below 2.55V, the operation of OB6566 is resumed.

When DOVP event lasts long enough, the Error Amplifier Output, COMP, will saturate and stay low. Static OVP comparator is activated and power MOSFET Gate is off when COMP voltage is dropped below 1V. Normal operation is resumed when Error Amplifier goes back to its linear region after output voltage drops.

# Current Sensing Comparator and Leading Edge Blanking

Cycle-by-cycle current limiting is provided in OB6583's peak current mode control. The switch current is detected by a sense resistor into the sense pin. The switch-on spike is blanked out via an internal leading edge blanking (LEB) circuit.



Another extra function of LEB is that it limits the system minimum on time, thus the THD of system at light load will be decreased.

The RS flip-flop ensures that only one single switch-on and switch-off pulse appears at the gate drive output during a given cycle..

#### PFC Gate Driver (PFCGATE Pin)

The output stage is designed to ensure zero cross-conduction current. This minimizes heat dissipation, increase efficiency, and enhance reliability. The output driver is also slew rate controlled to minimize EMI. The built-in 11.7V clamp at the gate output protects the MOSFET gate from high voltage stress.

#### • FUNCTIONAL DESCRIPTION for QR Multi-Mode Operation for QR

OB6683 integrates a multi-mode QR controller. The QR controller changes the mode of operation according to FB voltage, which reflects the line and load conditions, as shown in Fig.1.

■ Under normal operating conditions (FB>Vth2, Figure 1), the system operates in QR mode. The frequency varies depending on the line voltage and the load conditions. Therefore, the system may actually work in DCM when 130KHz frequency clamping is reached. System design should be optimized such that the operation frequency is within the range specified at full loading conditions and in universal AC line input range.

■ At light load condition (Vth1<VFB<Vth2, Figure 1), the system operates in PFM (pulse frequency modulation) mode for high power conversion efficiency. In PFM mode, the "ON" time in a switching cycle is fixed and the system modulates the frequency according to the load conditions. Generally, in flyback converter, the decreasing of loading results in voltage level decreasing at FB pin. The controller monitors the voltage level at FB and control the switching frequency. However, the valley switching characteristic is still preserved in PFM mode. That is, when loading decreases, the system automatically skip more and more valleys and the switching frequency is thus reduced. In such way, a smooth frequency foldback is realized and high power conversion efficiency is achieved.

■ At zero load or very light load conditions (VFB<Vth1), the system operates in On-Bright's proprietary "extended burst mode". In this condition, voltage at FB is below burst mode threshold level, Vth1. The Gate drive output switches only when VCC voltage drops below a preset level or FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss thus reduce the standby power consumption to the greatest extend. In extended burst mode, the switching frequency is fixed to 22KHz, in this way, possible audio noise is eliminated.



#### Figure 1

#### QR Demagnetization Detection (PRT pin)

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through PRT pin. This voltage features a flyback polarity. A new cycle starts when the power switch is activated, as shown in Fig.2. After the on time (determined by the QRCS voltage and FB), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately  $1/2\pi\sqrt{L_pC_d}$ , where  $L_p$  is the primary self inductance of the transformer and  $C_d$  is the capacitance on the drain node.



Figure 2



The typical detection level is fixed at 85mV at the PRT pin. Demagnetization is recognized by detection of a possible "valley" when the voltage at PRT is below 85mV in falling edge. PRT detection is suppressed during the ringing suppression time.

# QR Current Sensing and Leading Edge Blanking (QR\_CS pin)

Cycle-by-Cycle current limiting for the QR stage is offered in OB6683. The switch current is detected by a sense resistor into the QRCS pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state, the QR current limit comparator is disabled and cannot turn off the external MOSFET during the blanking period.

#### Built-in Soft Start for QR

The QR controller of OB6683 features a built-in 4ms soft start to soften the constraints occurring in the power supply during startup. It is activated after QR stage is enabled. As soon as QR stage begins to work after power on, the threshold voltage at QRCS pin is gradually increased from nearly zero to the maximum clamping level 0.5V in 4ms. Every system restart attempt is followed by a QR soft start sequence.

#### **Ringing Suppression Timer**

A ringing suppression timer Tsupp is implemented in the QR controller of OB6683. In normal operation, Tsupp starts when QRCS reaches the feedback voltage FB, the gate drive QRDRIVER is set to low. During Tsupp, gate drive QRDRIVER remains in low state and cannot turn power switch on again. The ringing suppression is necessary in applications where the transformer has a large leakage inductance, particularly at low output voltages or startup. In OB6683, the ringing suppression timer Tsupp is set to 2us internally.

#### Maximum Frequency Clamp in QR operation

According to the QR operation principle, the switching frequency is inversely proportional to the output power. Therefore, when the output power decreases, the switching frequency can become rather high without limiting. To meet EMI limit starting at 150KHz, the maximum switching frequency in OB6683 is internally limited to 130KHz.

#### **QR OCP Compensation**

A proprietary OCP compensation for QR stage is provided for better OCP performance in the universal input range. There is 100uA current flowing from QRCS pin at high AC input. In this way, OCP point difference between high line input and low line input is minimized by adjusting the resistor between QRCS and MOSFET source.

#### QR Output Over Voltage Protection (PRT pin)

An output over voltage protection is implemented by sensing the auxiliary winding voltage at PRT pin during the flyback phase. The auxiliary winding voltage is a well-defined replica of the output voltage. The QR OVP works by sampling the plateau voltage at PRT pin during the flyback phase, as shown in Fig.3. A 2 us internal delay (plateau sampling) guarantees a clean plateau, provided that the leakage inductance ringing has been fully damped.



If the sampled plateau voltage exceeds the OVP trip level (3.0V), an internal counter starts counting subsequent OVP events. If OVP events are detected in successive 7 cycles, the controller assumes a true OVP and it enters a latch off mode and stops all switching operations. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. If the output voltage exceeds the OVP trip level less than 7 successive cycles, the internal counter will be cleared and no fault is asserted.

#### QR Output Short Circuit Protection (PRT pin)

An output short circuit protection is implemented by sensing the auxiliary winding voltage at PRT pin during the flyback phase. The QR output short detection start working after delay 12mS when QR controller starts working. The QR output short protection works by sampling the plateau voltage at PRT pin during the flyback phase. If the sampled plateau voltage less than 0.75V ,the CS voltage is high than 0.45V, and FB is open , the controller assumes a true output short occurrence after successive 7 cycles and it enters restart mode and stops all switching operations. The special output short protection can minimize output short power consumption.

#### QR Over Load Operation (OLP)

When over load (for example, short circuit or open loop) in the QR stage occurs, the feedback current for QR FB pin is below minimum value



and a fault is detected. If this fault is present for more than 60ms, the controller enters an autorecovery soft burst mode. All pulses for PFC and QR are stopped, the controller will try to restart with the power on soft start after 1.4s. The SMPS enters the burst sequence and it resumes operation once the fault disappears.

#### **QR Gate Driver (QRGATE Pin)**

The QRGATE pin is connected to the gate of an external QR power switch with 1A capability. An internal 11.7V clamp is added for MOSFET gate protection at high VCC voltage. When VCC

voltage drops below UVLO(ON), the QRDRIVER pin is internally pull low to maintain the off state.

#### **PFC Shut Down**

With the decrease of load ,OB6683 can realize PFC shut down function by connecting a resistance Rpfc to the ground from the PFCONOFF pin in order to improve efficiency. The output current of critical shutdown PFC can be evaluated by the following formula:

$$I_{o\_shut}(\mathbf{A}) = 4.5 \times 10^{-3} \times \frac{R_{pfc}(k\Omega)}{R_{cs}(\Omega)} \times \frac{N_p}{N_s}$$



16-Pin Plastic SOP (SOP16)

# SOP16 PACKAGE OUTLINE DIMENSIONS







Symbol	Dimensions I	n Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
A	1.350	1.750	0.053	0.069	
A1	0.100	0.250	0.004	0.010	
A2	1.250	1.650	0.049	0.065	
b	0.310	0.510	0.012	0.020	
С	0.100	0.250	0.004	0.010	
D	9.800	10.400	0.386	0.409	
E	3.800	4.040	0.150	0.159	
E1	5.800	6.240	0.228	0.246	
е	1.270 (BSC)		0.050	(BSC)	
L	0.400	1.270	0.016	0.050	
θ	0°	8º	0°	8°	



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