GENERAL DESCRIPTION

OB6573 is a 8-pin active power factor correction (PFC) controller designed to operate in continuous conduction mode (CCM) with average current control. It provides near unity power factor for universal input line voltage (85VAC – 265VAC) with no need to sense the line input voltage. The IC allows major reductions in Bill of Materials (BOM) component count, PCB area and design time compared to traditional solutions. The switching frequency of OB6573 is trimmed and fixed internally at 65KHz. To achieve good EMI performance, the built-in frequency shuffling is provided. Both compensation for the voltage loop and the current loop are external to allow full user control. Fast 1.5A gate drive capability minimizes the need for external driver circuit.

OB6573 offers comprehensive protections to ensure safe system operation conditions including cycle by cycle over current protection(OCP), soft over current protection(SOCP), VCC under voltage lockout (UVLO), VCC clamping, open loop protection (OLP), programmable brownout protection and soft-start.

In addition, for low standby power requirements, OB6573 can be driven into standby mode with total current consumption of 200uA (typical), by pulling the VSENSE pin voltage below 0.5V.

FEATURES

- 8-Pin Solution without Sensing Line Voltage
- Average Current Continuous Control Mode
- Fixed 65KHz Frequency with Frequency Shuffling for Better EMI
- Wide-range Universal AC Input Voltage
- Very Low Shutdown Currents (Typical 200uA)
- Maximum Duty Cycle of 97%
- Trimmed Internal Reference
- Input Brown-out Protection
- Cycle by Cycle Over Current Limit
- Soft Over Current Protection
- Output Over Voltage Protection
- Open Loop Protection
- Enhanced Dynamic Response
- Soft Start
- VCC Under Voltage Lockout (UVLO)
- Pin to Pin Compatible with Industry Standard

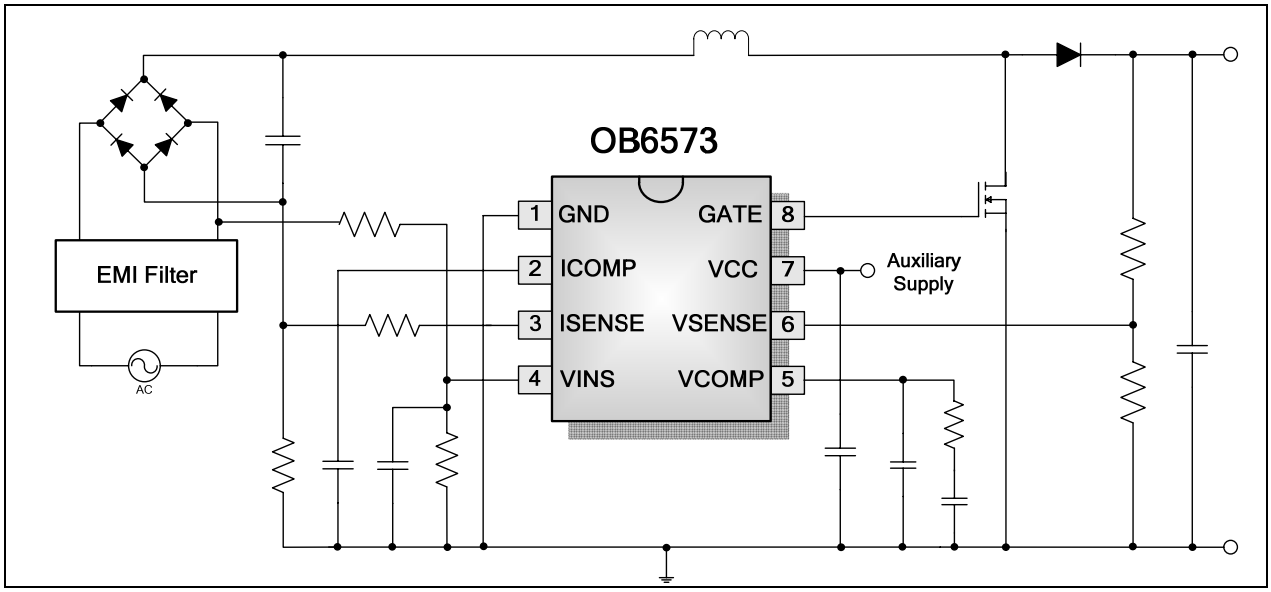
APPLICATIONS

CCM mode power factor correction for

- LCD /Flat TV
- Server and PC Power Supplies
- AC Adapters and other Off-line SMPS
- Telecom Rectifiers

OB6573 is offered in SOP-8 and DIP-8 packages

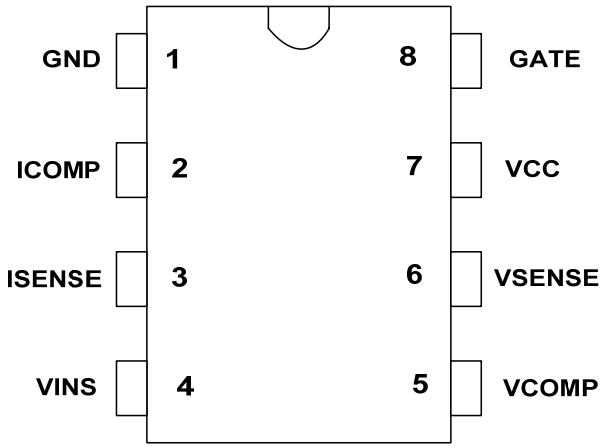
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The pin map of OB6573 in DIP8 and SOP8 package is shown as below.



Ordering Information

Part Number	Description
OB6573AP	DIP8, Pb-free
OB6573CP	SOP8, Pb-free
OB6573CPA	SOP8, Pb-free in Taping

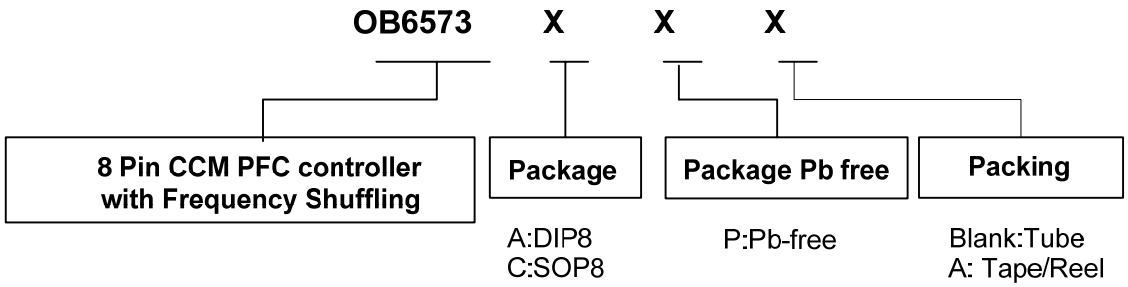
Package Dissipation Rating

Package	RθJA (℃/W)
DIP8	90
SOP8	150

Absolute Maximum Ratings

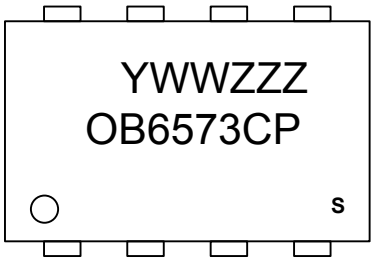
Parameter	Value
VCC Zener Clamp Voltage	33 V
VCC Clamp Continuous Current	15 mA
ICOMP Input Voltage	-0.3 to 7V
ISENSE Input Voltage	-0.3 to 7V
VINS Input Voltage	-0.3 to 7V
VCOMP Input Voltage	-0.3 to 7V
VSENSE Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-40 to 150 ℃
Min/Max Storage Temperature T_{stg}	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



Marking Information

SOP8



Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot Code
C:SOP8 Package
P:Pb-free Package
S:Internal Code(Optional)

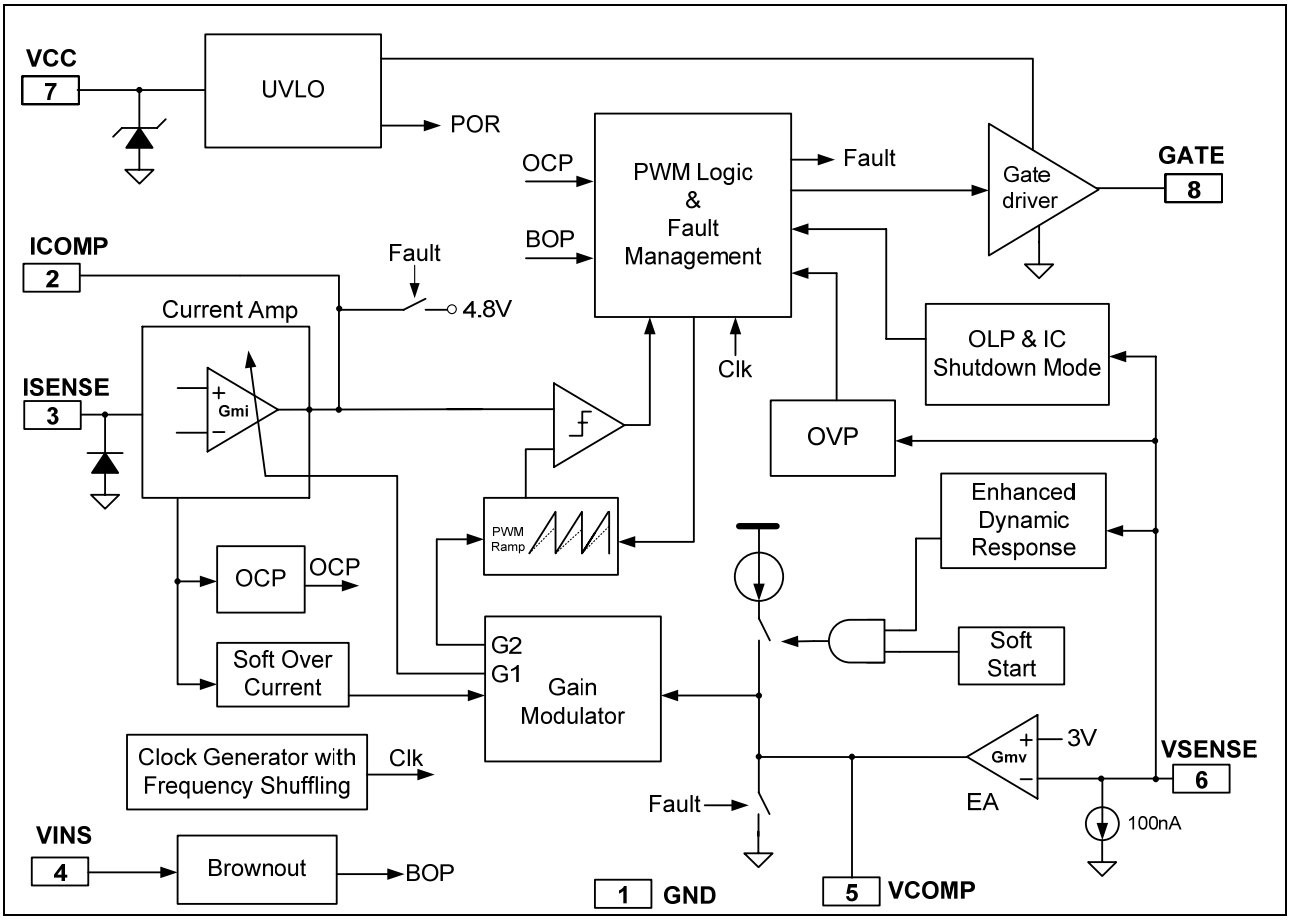
DIP8

Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot Code
A:DIP8 Package
P:Pb-free Package
S:Internal Code(Optional)

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	GND	P	Chip ground pin.
2	ICOMP	O	This pin is for low pass filter and compensation of PFC current control loop. A capacitor connected to GND provides averaging of the current sense signal.
3	ISENSE	I	This pin sources a current I_{SENSE} which is proportional to the average inductor current. The sense current I_{SENSE} is for cycle-by-cycle current limiting, soft over current protection (SOCP) and PFC duty cycle modulation.
4	VINS	I	Input brownout protection pin. Connects a resistor divider from the rectified main voltage to this pin, if the pin voltage drops below 0.8V and lasts for 50ms, PWM output will be disabled. When brownout is triggered, this pin will disable an internal current for brownout hysteresis programming.
5	VCOMP	O	Output of PFC error amplifier (EA). A compensation network is placed between VCOMP and GND to achieve stability of the voltage control loop and ensure high power factor and low THD.
6	VSENSE	I	Inverting input of the PFC error amplifier (EA). An external resistor-divider network connected from this pin to the PFC output voltage provides feedback sensing for output voltage regulation. An internal 100nA current source pulls VSENSE to GND for open loop protection (OLP).
7	VCC	P	Chip power supply input.
8	GATE	O	Gate driver output. A push-pull output stage is able to drive the external power MOSFET with peak current of 1.5A (source and sink). The max. GATE output voltage is clamped at 16V.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Max	Unit
VCC	VCC Supply Voltage	12	30	V
T_A	Operating Ambient Temperature	-20	85	°C

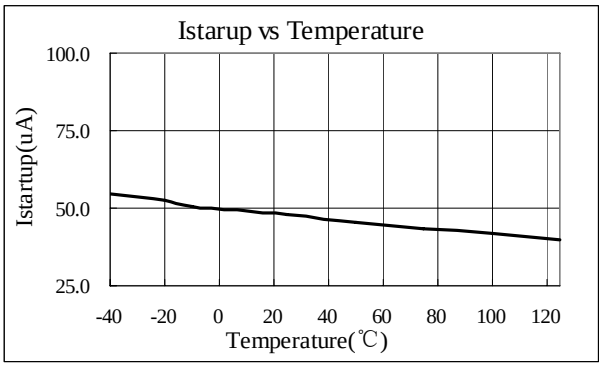
ELECTRICAL CHARACTERISTICS

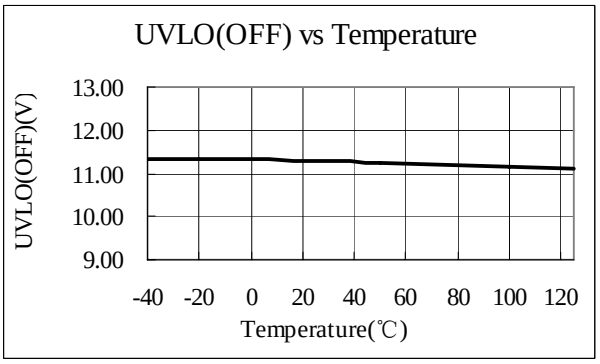
(TA = 25℃, VCC=15V, if not otherwise noted)

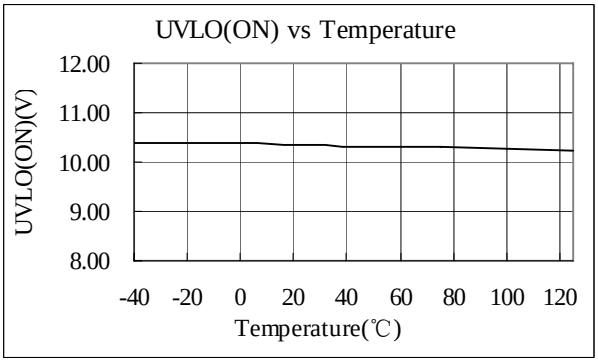
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VCC) Section						
UVLO(ON)	VCC under voltage lockout enter		9.4	10.2	10.8	V
UVLO(OFF)	VCC under voltage lockout exit		10.5	11.2	11.9	V
UVLO_hys	UVLO hysteresis		0.8	1	1.3	V
Istartup	VCC start up current	VCC=UVLO(OFF)-1V, Measure current into VCC		50	100	uA
Ion_load	Operation current	VSENSE=2.5V,GATE=4.7nF		6.8	10	mA
Istandby	Standby current	VSENSE=0.3V		200	400	uA
Vz	VCC zener clamp voltage	I(VCC) = 15 mA		33		V
PWM Section						
Duty	Duty cycle range			0-97		%
Toff_min	Minimum off time	ISENSE=0.1V	100	250	580	ns
Oscillator Section						
Fsw	Switching frequency		60	65	70	KHz
△Fsw	Frequency shuffling range / Base frequency		-5		+5	%
Fsw_r	Frequency shuffling repeatability			1		KHZ
Voltage Loop Section						
Gmv	EA transconductance gain		30	40	50	uS
Vea	EA reference voltage		2.92	3.00	3.08	V
Ivsense	VSENSE pin sink current	VSENSE=3V		100	500	nA
Isink_max	EA Maximum sink current under normal operation	VSENSE=4V, VCOMP=4V	20	30	40	uA
Isource_max	EA Maximum source current under normal operation	VCOMP=0V	20	30	40	uA
I_{SST}	Source current under soft start	VSENSE=2V,VCOMP=0V	20	30	40	uA
$V_{SST(exit)}$	VSENSE voltage at which soft start exits after power on soft start		2.75	2.85	2.95	V
V_{EDR}	VSENSE threshold below which enhanced dynamic response occurs		2.75	2.85	2.95	V
$I_{EDR(max)}$	Maximum source current under EDR operation	VCOMP=4V		170		uA
Current Loop Section						
Gmi	Transconductance gain		0.7	1.0	1.2	mS

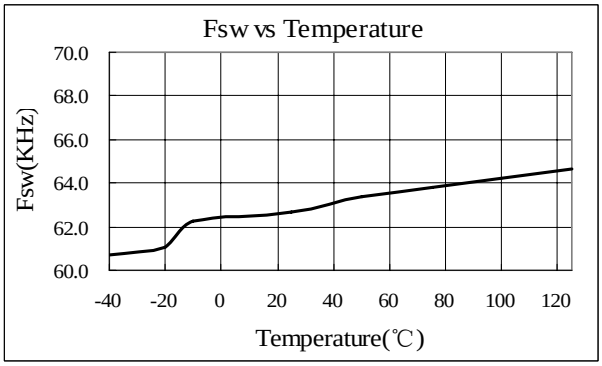
ICOMP_fault	ICOMP pin voltage during fault		4.0	4.8		V
System Protection Section						
V_{OLP}	VSENSE threshold, open loop protection (OLP)		0.40	0.50	0.60	V
V_{OVP}	VSENSE threshold, output over voltage protection (OVP)		3.08	3.15	3.22	V
I_{SOCP}	ISENSE pin sourcing current @ soft over current protection (SOCP)		90	100	110	uA
I_{OCP}	ISENSE pin sourcing current @ over current protection (OCP)			150		uA
$Vref_{BOP}$	VINS threshold, brownout protection threshold voltage		0.74	0.80	0.86	V
I_{BOP}	Brownout protection hysteresis current			2.0		uA
Tbop_debounce	Brownout debounce time			50		ms
Gate Drive Output Section						
VoL	Low Output Voltage	VCC=12V, Io=20mA			1.0	V
VoH	High Output Voltage	VCC=12V, Io=20mA	8.0			V
Tr	Rising Time	GATE=4.7nF, 2V~8V		60		ns
Tf	Falling Time	GATE=4.7nF, 8V~2V		50		ns
Vgate_clamp	GATE Output clamp voltage	VCC=25V		16		V
Iopk	Output peak current	GATE=4.7nF	1.5			A

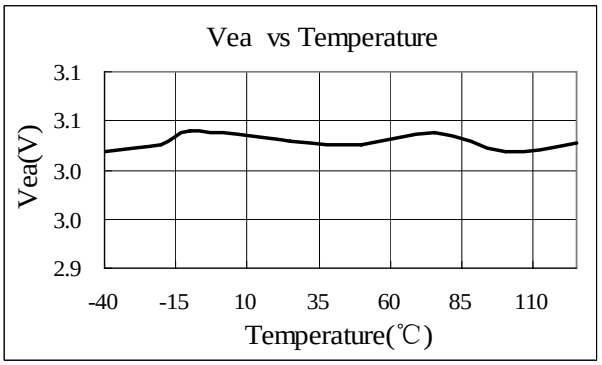
CHARACTERIZATION PLOTS











OPERATION DESCRIPTION

OB6573 is a 8-pin switch mode controller used in boost converters for power factor correction. It is designed to operate at a fixed frequency in continuous conduction mode (CCM) with average current control.

The IC operates with two loops: an inner current loop and an outer voltage loop. The inner current loop sustains the sinusoidal profile of the average input current based on the dependency of the PWM duty cycle on the input line voltage in order to determine the analogous input line current. Thus, the current loop uses the embedded input voltage signal to control the average input current to follow the input voltage. The outer voltage loop regulates the output DC bus voltage through the voltage error amplifier (EA). Depending on the line and load conditions, the voltage error amplifier establishes a voltage at VCOMP which determines the internal gain parameters for maintaining a low distortion steady-state input current wave-shape.

Under extremely light load conditions, the system may enter into discontinuous conduction mode (DCM) resulting in a higher harmonics. OB6573 specially optimizes the harmonic performance under DCM condition so as to meet Class-D requirement of IEC 1000-3-2.

- **Power Supply & UVLO**

The IC is recommended to be powered by an external auxiliary supply. In OB6573, an internal under voltage lockout (UVLO) block monitors the VCC voltage, as soon as it exceeds 11.2V and no fault conditions detected, the IC begins operating its gate driver and enters start-up state. When VCC voltage drops below 10.2V, the IC is off and only consumes typically 50uA current.

- **Soft Start**

Soft Start controls the rate of rise of the output voltage error amplifier (EA) in order to obtain a linear control of the increasing duty cycle as a function of time. During soft start a constant 30uA of current is sourced into the compensation components of VCOMP causing VCOMP pin voltage linearly ramp up until output voltage feedback VSENSE voltage is above 2.85V and soft start is ended. The soft start time is controlled by the VCOMP pin compensation components selected and is user programmable. Every restart attempt is followed by soft start sequence.

- **PFC Voltage Error Amplifier**

PFC Error Amplifier (EA) provides regulation for the PFC voltage loop. Connected to a resistor divider from PFC output, the inverting input of the EA (VSENSE pin voltage) is compared to an internal reference voltage (3V) to set the regulation on output voltage. The EA consists of a transconductance amplifier with a typical transconductance value of 40 uS. The sink and source capability of the EA is approximately 30uA during normal operation. By connecting a compensation network between VCOMP (EA output) and GND, PFC loop compensation is realized. The system loop bandwidth is set below 20 Hz to suppress the AC ripple of the line voltage. During UVLO, OLP, brownout etc. fault conditions, OB6573 pulls VCOMP pin to GND. After the fault conditions are released, soft start process takes over.

- **Pulse Width Modulator (PWM)**

OB6573 employs an average current control scheme in continuous conduction mode (CCM) to achieve the power factor correction. The PWM stage compares the ICOMP signal with an internal periodic ramp to generate a leading edge modulated output signal which is high whenever the ramp voltage exceeds the ICOMP voltage. The slope of the internal ramp is defined by a non-linear function of the internal VCOMP voltage. The PWM output signal always starts low at the beginning of each cycle, triggered by the internal clock. The output stays low for a minimum off time, T_{OFF}(min), after which the internal ramp rises linearly to intersect the ICOMP voltage. This intersection determines T_{OFF}, and hence D_{OFF}. Since for the boost type PFC system, the instantaneous PWM off duty cycle can be express as:

$$D_{OFF} = \frac{V_{IN}}{V_{OUT}}$$

The PWM generation described above guarantees that the instantaneous ICOMP voltage is proportional to D_{OFF}, and since the average inductor current I_{L_avg} is proportional to ICOMP voltage, it can be easily seen that

$$I_{L\_avg} \propto V_{ICOMP} \propto D_{OFF} = \frac{V_{IN}}{V_{OUT}} \propto V_{IN}$$

And since V_{IN} is sinusoidal wave-shape, the average input current I_{L_avg} is also sinusoidal in wave-shape, as illustrated in the equation above.

- **PFC Current Loop**

The current loop generates a signal which is proportional to the average inductor current. An external capacitor to GND is applied to the ICOMP pin for current loop compensation and current ripple filtering. The gain of the current loop averaging amplifier is determined by the internal VCOMP voltage. This gain is non-linear to accommodate the wide AC input range (85 – 265VAC) and wide loading variations. ICOMP pin is connected to 4.8V internally whenever the device is in a Fault or Shutdown Mode

- **OVP/EDR/Shutdown/OLP**

The feedback signal VSENSE represents the PFC output voltage and will be used in the output voltage regulation, Over voltage protection (OVP), Enhanced dynamic response (EDR), IC shutdown mode (Shutdown) and Open loop protection (OLP), as shown in Fig. 2.

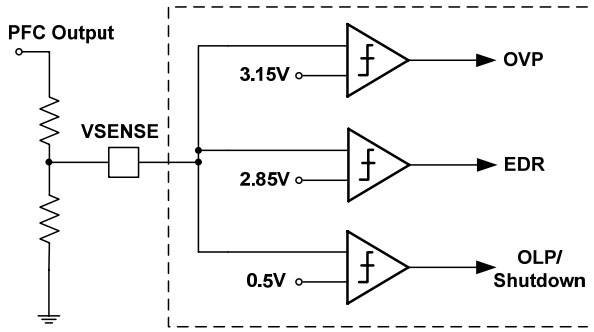


Figure 2

Output Over Voltage Protection (OVP)

Whenever VSENSE voltage higher than 3.15V (above the reference value by 5%), the over voltage protection OVP is activated and the gate PWM output is immediately disabled until VSENSE voltage fall below 3.15V. The trimmed accurate OVP threshold voltage enables the usage of a cost effective PFC bus capacitor with lower voltage rating (for example, 400V rating capacitor) for this application.

Enhanced Dynamic Response (EDR)

Given the low bandwidth of PFC voltage loop, the output voltage of PFC stages may exhibit excessive over or under-shoots because of abrupt load or input voltage variations (such as start-up duration). OB6573 provides enhanced dynamic response for the PFC loop by detecting VSENSE pin voltage. Whenever VSENSE pin voltage falls below 2.85V, voltage EA will source typical 170uA current to VCOMP, which raise VCOMP voltage rapidly. This change will affect PWM duty cycle directly, which results in a fast dynamic response for the PFC stage.

IC Shutdown Mode (Shutdown)

The IC shutdown mode is initiated by pulling the VSENSE pin below 0.5V (typ.). In this mode, OB6573 draws a very low quiescent supply current (typical 200uA). This feature helps to meet stringent standby specifications.

Open Loop Protection (OLP)

If feedback loop is abnormal, such as VSENSE is shorted to ground or upper voltage feedback resistor is open, VSENSE pin will be pulled low by internal 100nA current source, the IC will then enter into shutdown mode.

- **SOCP/OCP**

OB6573 senses the inductor current by the current sense scheme in Fig.2. The device maintains ISENSE pin to be approximately zero voltage and detects the current sourcing into ISENSE pin for Soft Over Current Protection (SOCP) against an overload on the output and cycle-by-cycle current limit (OCP) against inductor saturation.

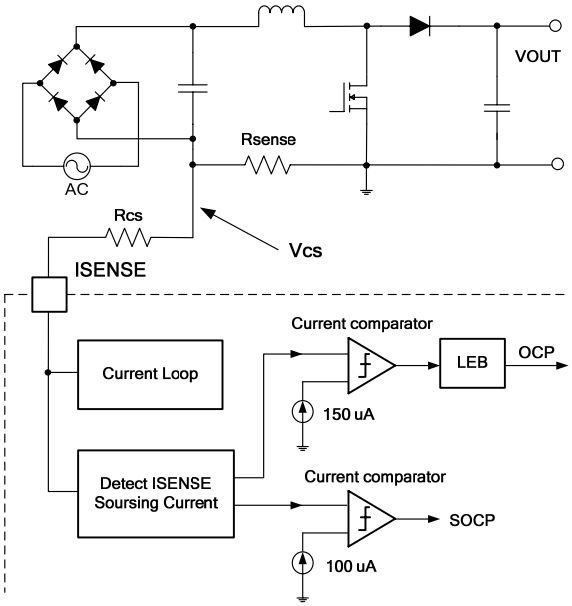


Figure 2

Soft Over Current Protection (SOCP)

When the sourcing current to ISENSE pin reaches I_{SOCP} (100uA typical), the soft over current protection (SOCP) will be active to limit output power. This is a soft control as it does not directly turn off the gate driver. It acts on the control loop to

result in a reduced PWM duty cycle.
In OB6573, the maximum inductor current I_{L_MAX} is designed to be a function of R_{CS} and R_{SENSE} , which can be approximated as:

$$I_{L\_MAX} \approx \frac{R_{CS}}{R_{SENSE}} \times I_{SOCP}$$

It is recommended that R_{CS} is set to be 6.8K Ohm.

Over Current Protection (OCP)

When the sourcing current to ISENSE pin reaches I_{OCP} (150uA typical), over current protection (OCP) is active and gate output is immediately turned off. An internal leading edge blanking (LEB) circuit improves noise immunity against false triggering.

- **Non-linear Gain Modulator**

The VCOMP pin voltage is used to set the current amplifier gain and the internal PWM ramp slope via built-in non-linear gain modulator. The non-linear gain modulator is related to the current and voltage loop stability and is specially designed to support the wide input voltage range (85 – 265VAC) and wide loading range.

- **Frequency Shuffling for EMI Improvement**

Frequency shuffling method can soften the EMI signature by spreading the energy in the vicinity of the main switching component, thus it can ease the system design in meeting stringent EMI requirement. In OB6573, the magnitude of shuffling lies in the ranged of ±5% of the main switching frequency (65KHz).

- **Programmable Brownout Protection**

By monitoring the level on pin VINS during normal operation, the controller protects the SMPS against low main condition. Fig.3 illustrates brownout protection implementation in OB6573. An internal 2uA current source is for brownout hysteresis window programming. The other 2uA source current is for VINS pin floating protection. When VINS level falls below 0.8V and lasts for about 50ms, the controller stops pulsing until this level goes back and resumes operation. By adjusting the resistor divider connected between the high input voltage and this pin, start and stop levels are programmable.

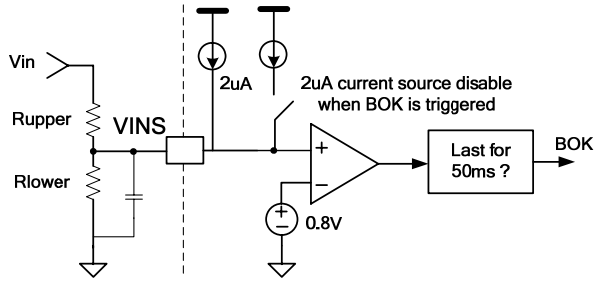


Figure 3

$$V_{BOP}(AC) = \frac{1}{\sqrt{2}}[(\frac{0.8}{Rlower} - 4\times10^{-6}) \times Rupper + 0.8]$$

$$V_{BOP\_HYS}(AC) = \sqrt{2} \times 10^{-6} \times Rupper$$

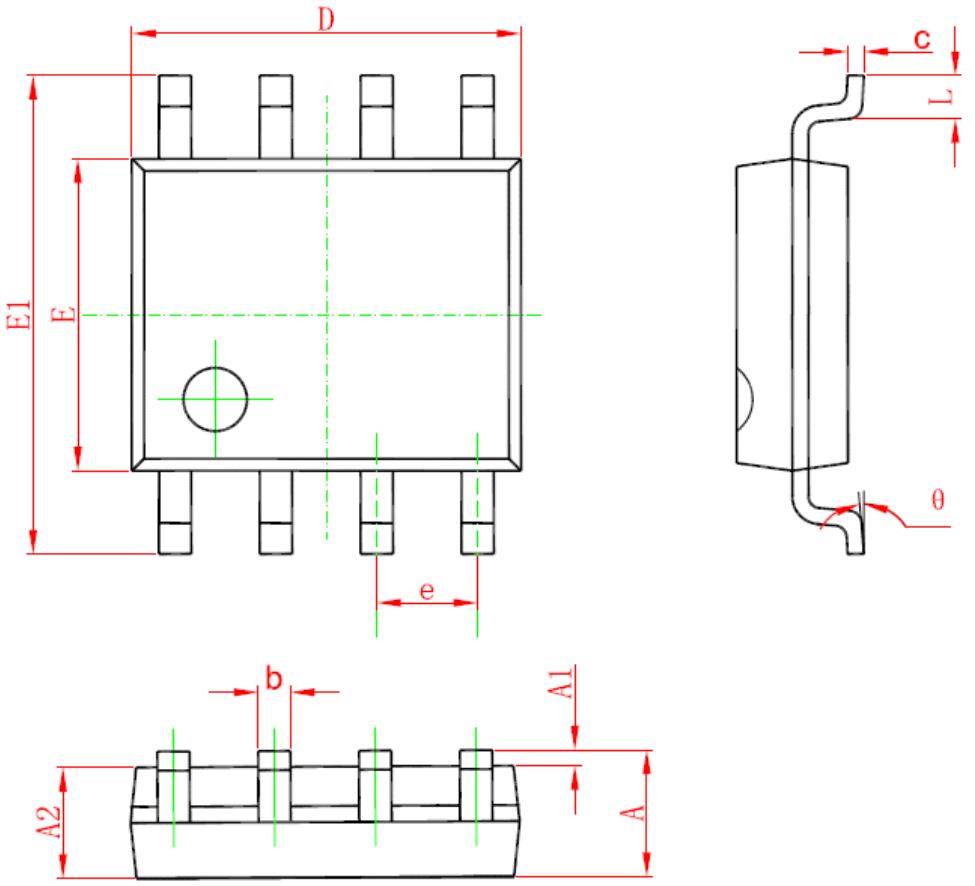
V_{BOP}(AC) is line brownout protection voltage;
V_{BOP_HYS}(AC) is line brownout hysteresis voltage.

- **Gate Driver**

The output of OB6573 (GATE pin) is fed by a totem pole MOSFET driver with 1.5A capability. An internal 16V clamp is added for MOSFET gate protection at high VCC voltage. When VCC voltage drops below UVLO(ON), the GATE pin is internally pull low to maintain the off state.

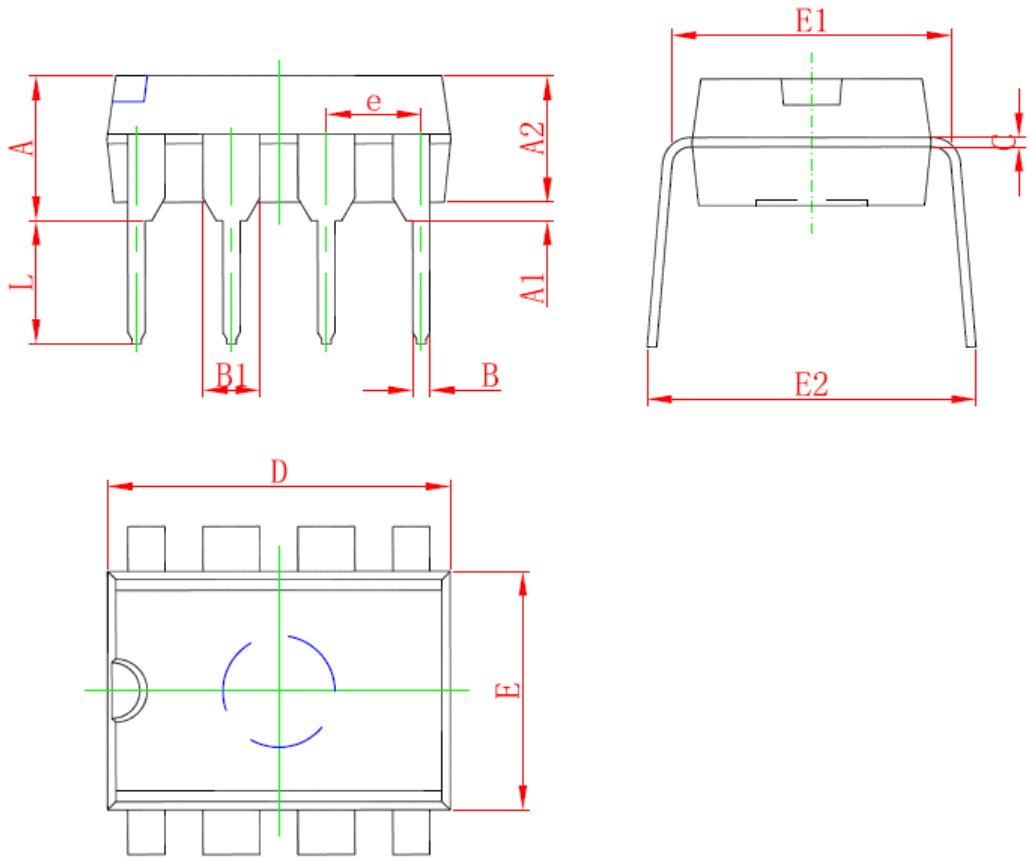
PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

DIP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	5.334	0.146	0.210
A1	0.381		0.015	
A2	2.921	4.953	0.115	0.195
B	0.350	0.650	0.014	0.026
B1	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.096	7.112	0.240	0.280
E1	7.320	8.255	0.288	0.325
e	2.540 (BSC)		0.1 (BSC)	
L	2.921	3.810	0.115	0.150
E2	7.620	10.920	0.300	0.430

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