



# NX7002BKXB

60 V, dual N-channel Trench MOSFET

30 June 2015

Product data sheet

## 1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010B-6 (SOT1216) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Logic-level compatible
- Leadless ultra small and ultra thin SMD plastic package 1.1 x 1.0 x 0.37 mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

## 4. Quick reference data

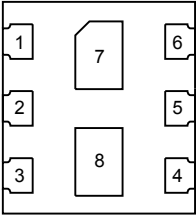
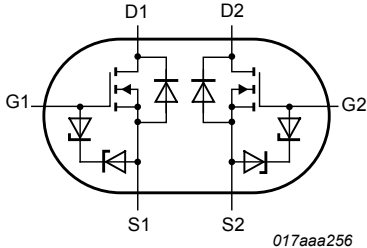
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	-	60	V
V <sub>GS</sub>	gate-source voltage			-20	-	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>sp</sub> = 25 °C		-	-	330	mA
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C	[1]	-	-	260	mA
Static characteristics (per transistor)							
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 200 mA; T <sub>j</sub> = 25 °C		-	2.2	2.8	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm<sup>2</sup>.



5. Pinning information

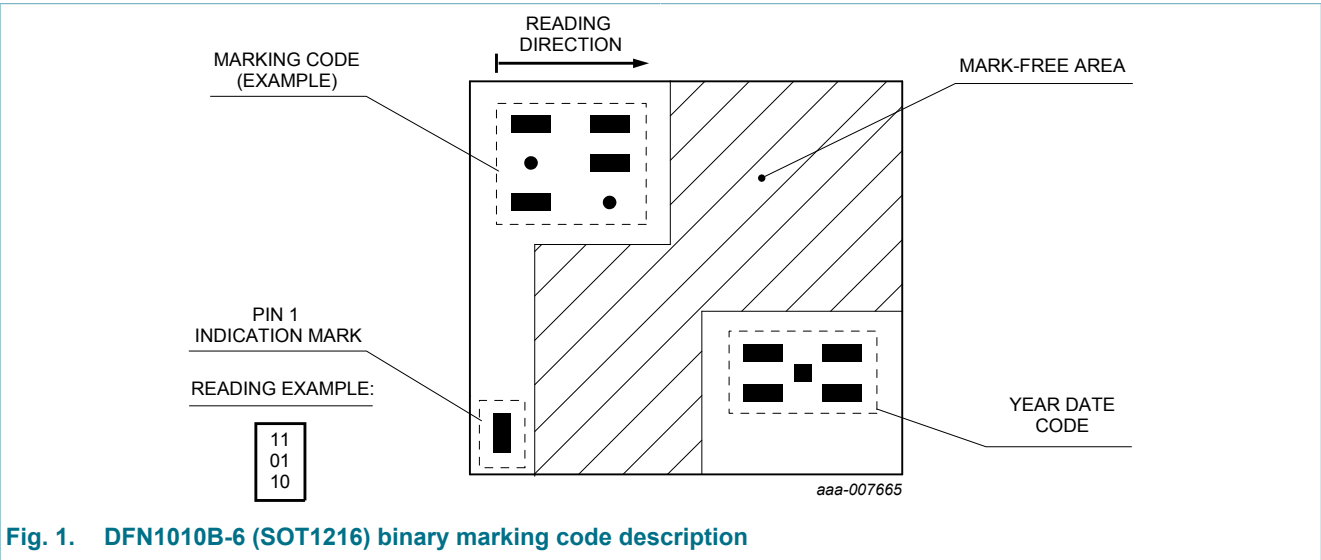
Table 2. Pinning information					
Pin	Symbol	Description	Simplified outline	Graphic symbol	
1	S1	source TR1	 <p>Transparent top view <b>DFN1010B-6 (SOT1216)</b></p>	 <p>017aaa256</p>	
2	G1	gate TR1			
3	D2	drain TR2			
4	S2	source TR2			
5	G2	gate TR2			
6	D1	drain TR1			
7	D1	drain TR1			
8	D2	drain TR2			

6. Ordering information

Table 3. Ordering information			
Type number	Package		
	Name	Description	Version
NX7002BKXB	DFN1010B-6	DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1216

7. Marking

Table 4. Marking codes	
Type number	Marking code
NX7002BKXB	00 01 01



## 8. Limiting values

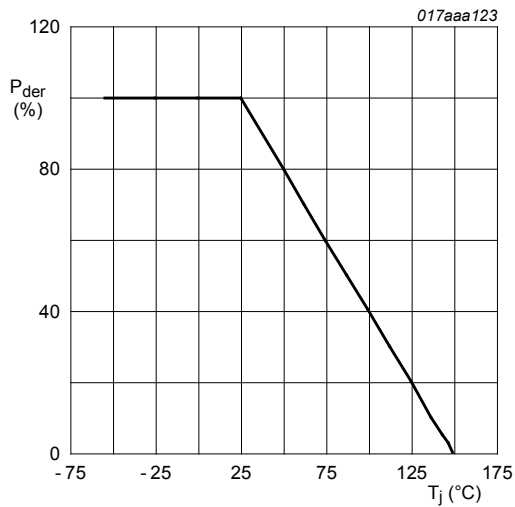
**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	60	V
V <sub>GS</sub>	gate-source voltage			-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>sp</sub> = 25 °C		-	330	mA
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C	[1]	-	260	mA
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 100 °C	[1]	-	170	mA
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	0.8	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	285	mW
			[1]	-	407	mW
		T <sub>sp</sub> = 25 °C		-	4032	mW
Source-drain diode						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	0.2	A
Per device						
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

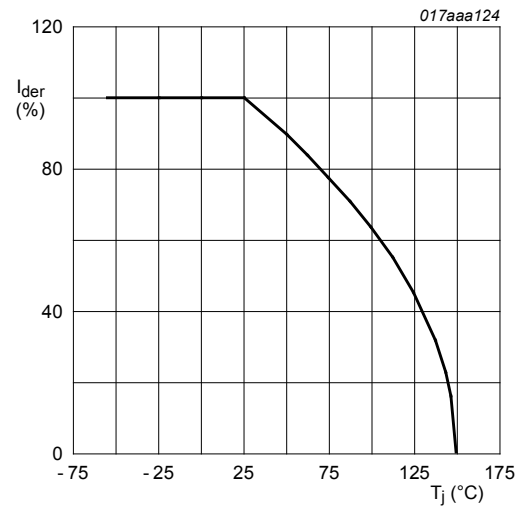
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain  $1\text{ cm}^2$ .

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



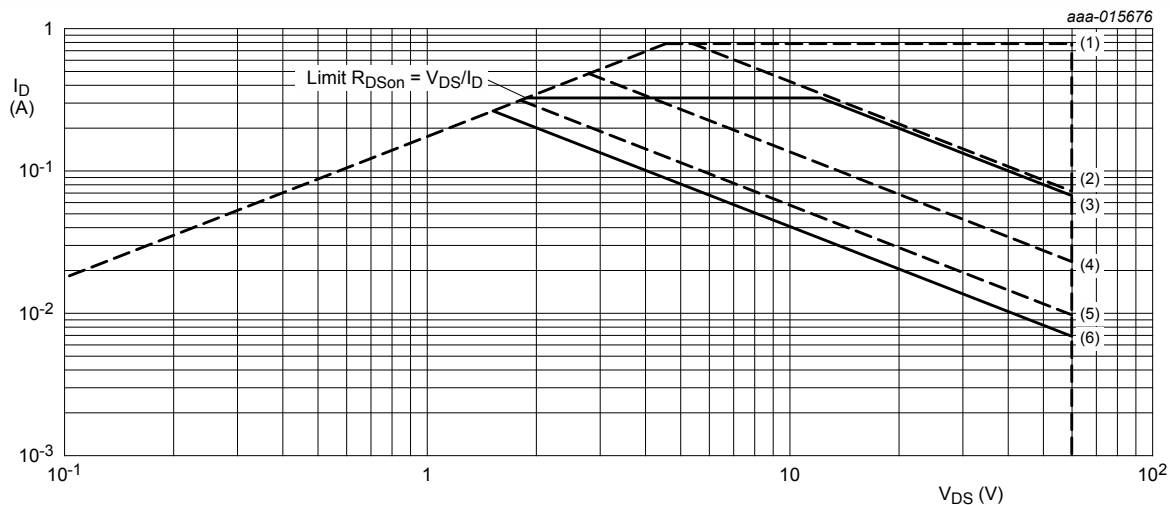
**Fig. 2. MOSFET transistor: Normalized total power dissipation as a function of junction temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$



**Fig. 3. MOSFET transistor: Normalized continuous drain current as a function of junction temperature**

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$



$I_{DM}$  = single pulse

(1)  $t_p = 10 \mu\text{s}$

(2)  $t_p = 1 \text{ ms}$

(3) DC;  $T_{sp} = 25^{\circ}\text{C}$

(4)  $t_p = 10 \text{ ms}$

(5)  $t_p = 100 \text{ ms}$

(6) DC;  $T_{amb} = 25^{\circ}\text{C}$ ; drain mounting pad  $1 \text{ cm}^2$

**Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage**

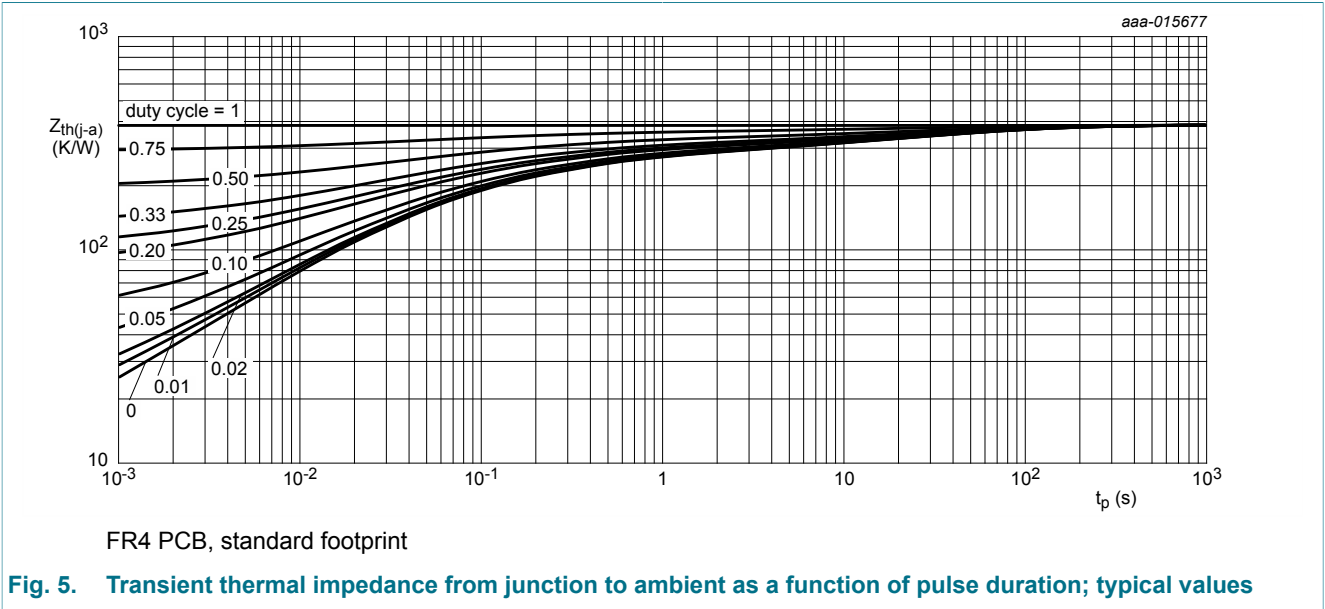
9. Thermal characteristics

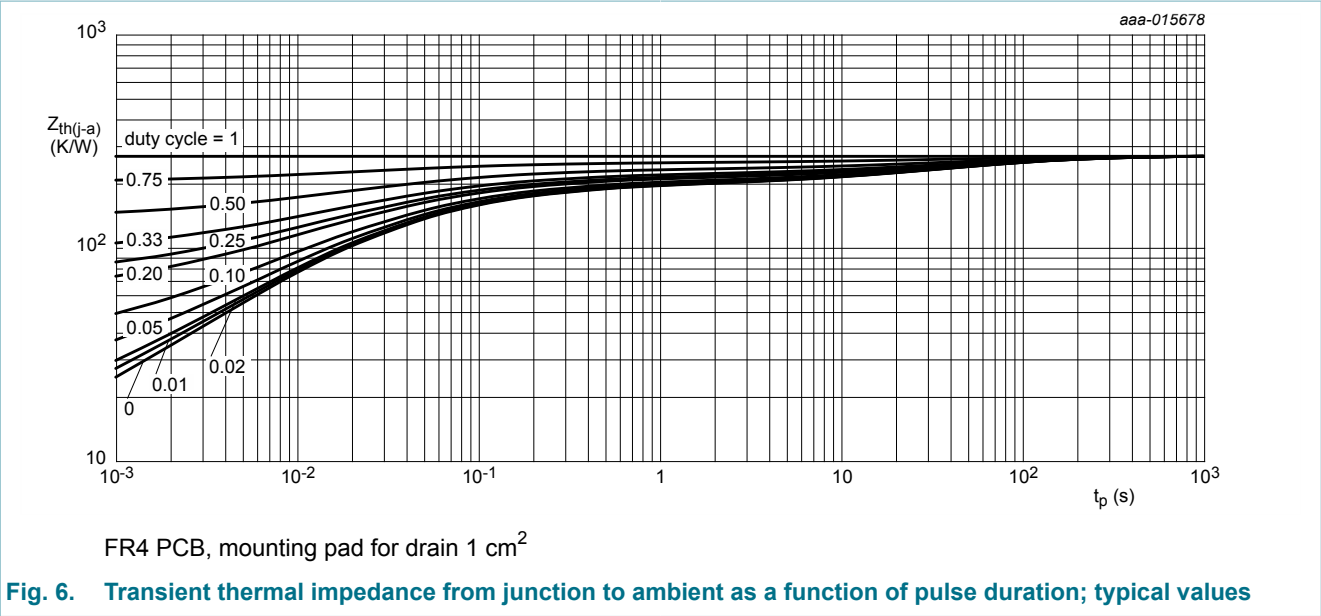
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	276	307	K/W
			[2]	-	381	438	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point			-	27	31	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm<sup>2</sup>.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.





## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics (per transistor)							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		60	-	-	V
V <sub>GSth</sub>	gate-source threshold voltage	I <sub>D</sub> = 250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C		1.1	1.6	2.1	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 60 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	10	μA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-10	μA
		V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	1	μA
		V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-1	μA
		V <sub>GS</sub> = 5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	0.3	μA
		V <sub>GS</sub> = -5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-0.3	μA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 200 mA; T <sub>j</sub> = 25 °C		-	2.2	2.8	Ω
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 200 mA; T <sub>j</sub> = 150 °C		-	4.5	5.7	Ω
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 200 mA; T <sub>j</sub> = 25 °C		-	2.5	3.2	Ω
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 200 mA; T <sub>j</sub> = 25 °C		-	600	-	mS
R <sub>G</sub>	gate resistance	f = 1 MHz		-	2.5	-	Ω
Dynamic characteristics (per transistor)							
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = 30 V; I <sub>D</sub> = 200 mA; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C		-	1	-	nC
Q <sub>GS</sub>	gate-source charge			-	0.12	-	nC
Q <sub>GD</sub>	gate-drain charge			-	0.18	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 10 V; f = 1 MHz; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	23.6	-	pF
C <sub>oss</sub>	output capacitance			-	4.6	-	pF
C <sub>rss</sub>	reverse transfer capacitance			-	3	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 50 V; I <sub>D</sub> = 200 mA; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C		-	4.7	-	ns
t <sub>r</sub>	rise time			-	4.3	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	6.9	-	ns
t <sub>f</sub>	fall time			-	2.9	-	ns
Source-drain diode (per transistor)							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 200 mA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	0.87	1.2	V

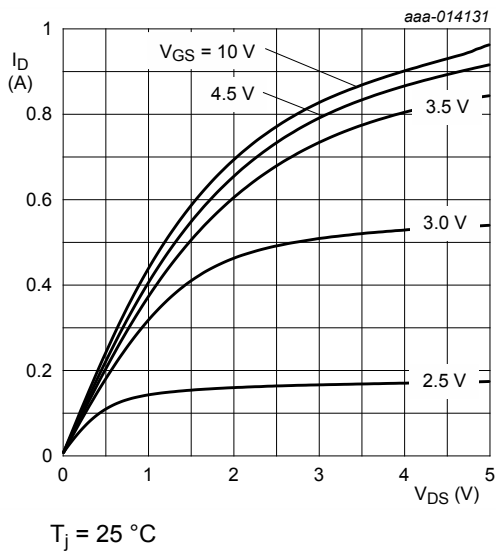


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

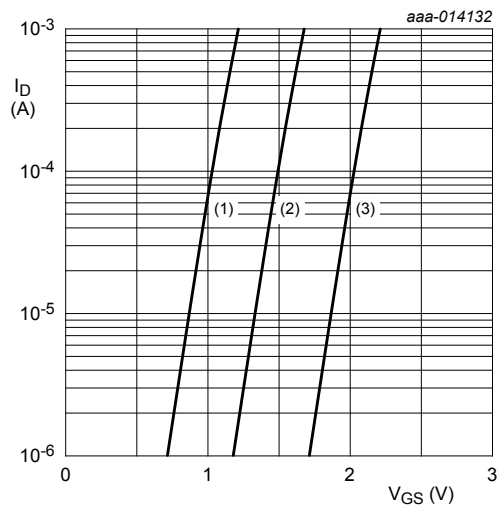


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

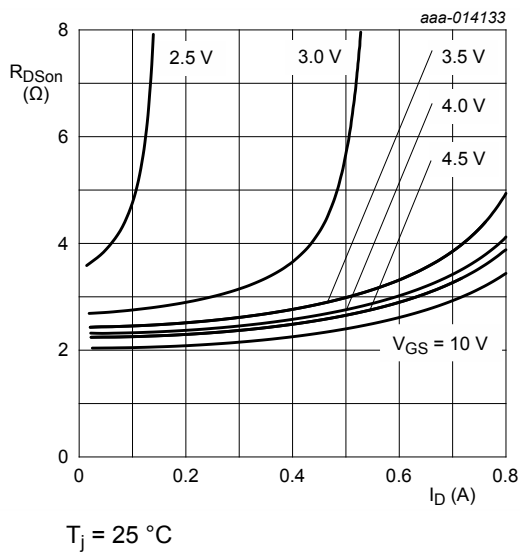


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

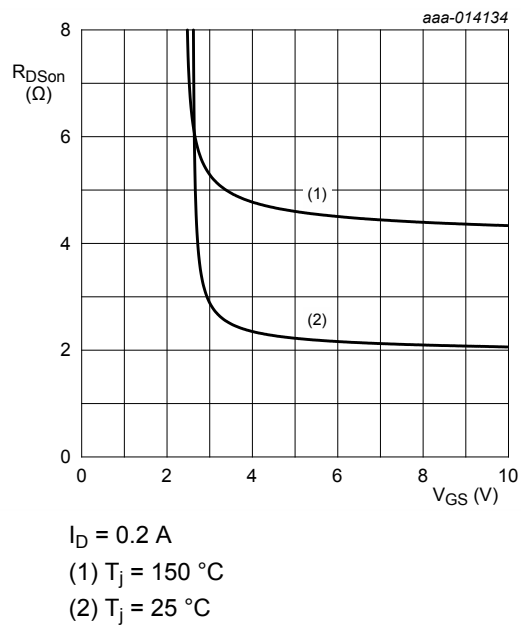


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



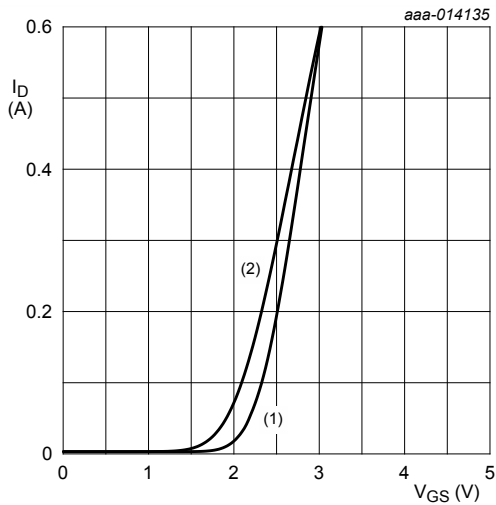


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

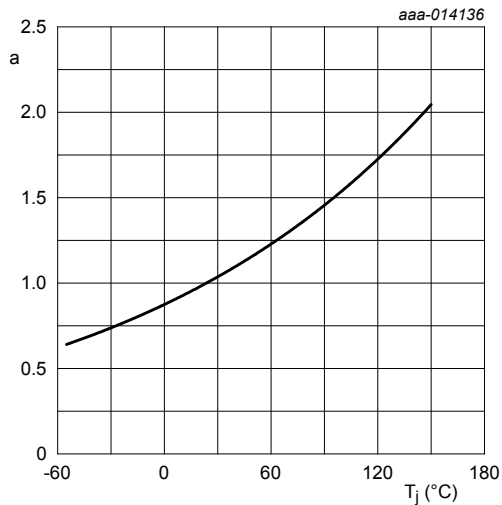


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

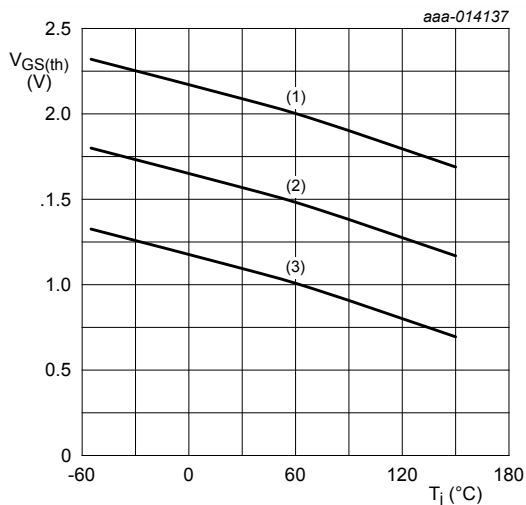


Fig. 13. Gate-source threshold voltage as a function of junction temperature

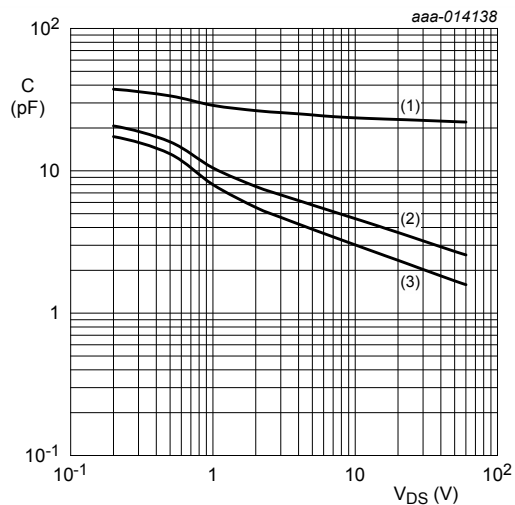


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

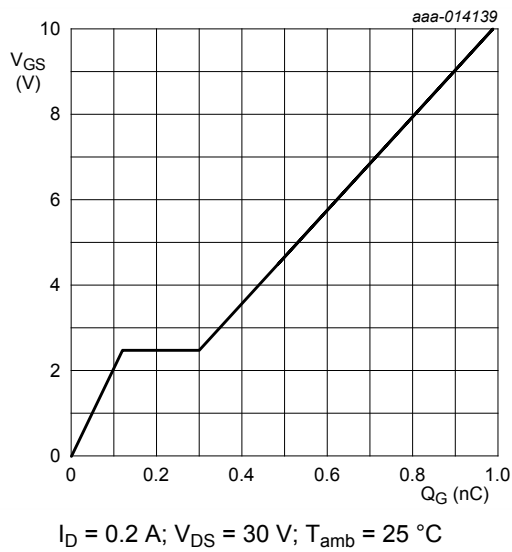


Fig. 15. Gate-source voltage as a function of gate charge; typical values

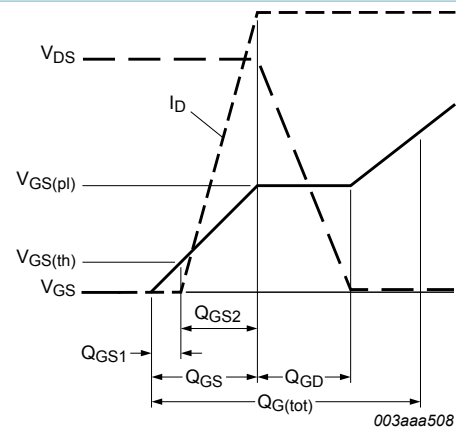
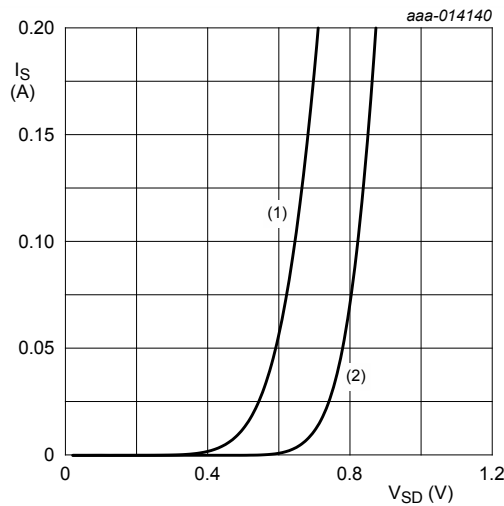


Fig. 16. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0\text{ V}$   
(1)  $T_j = 150\text{ }^{\circ}\text{C}$   
(2)  $T_j = 25\text{ }^{\circ}\text{C}$

Fig. 17. Source current as a function of source-drain voltage; typical values

## 11. Test information

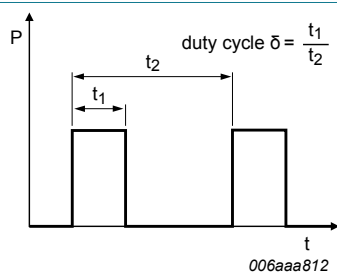
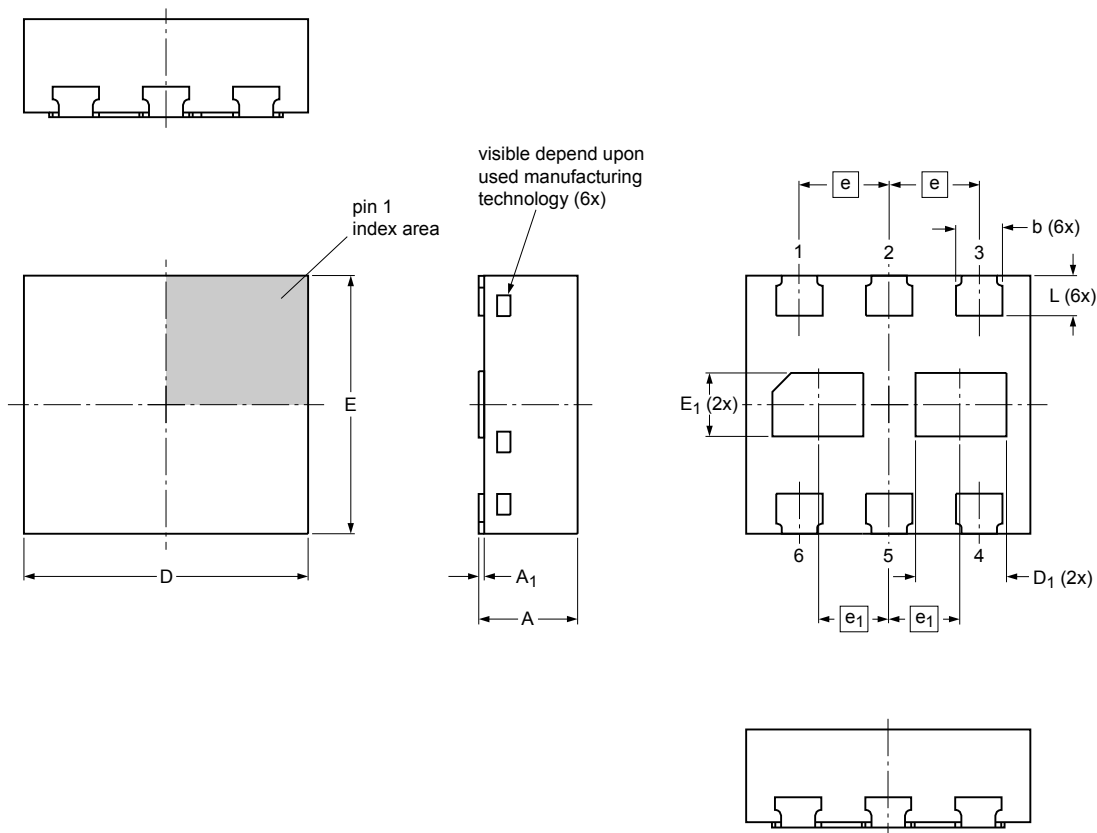


Fig. 18. Duty cycle definition

12. Package outline

DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads;  
6 terminals; body: 1.1 x 1.0 x 0.37 mm

SOT1216



Dimensions (mm are the original dimensions)

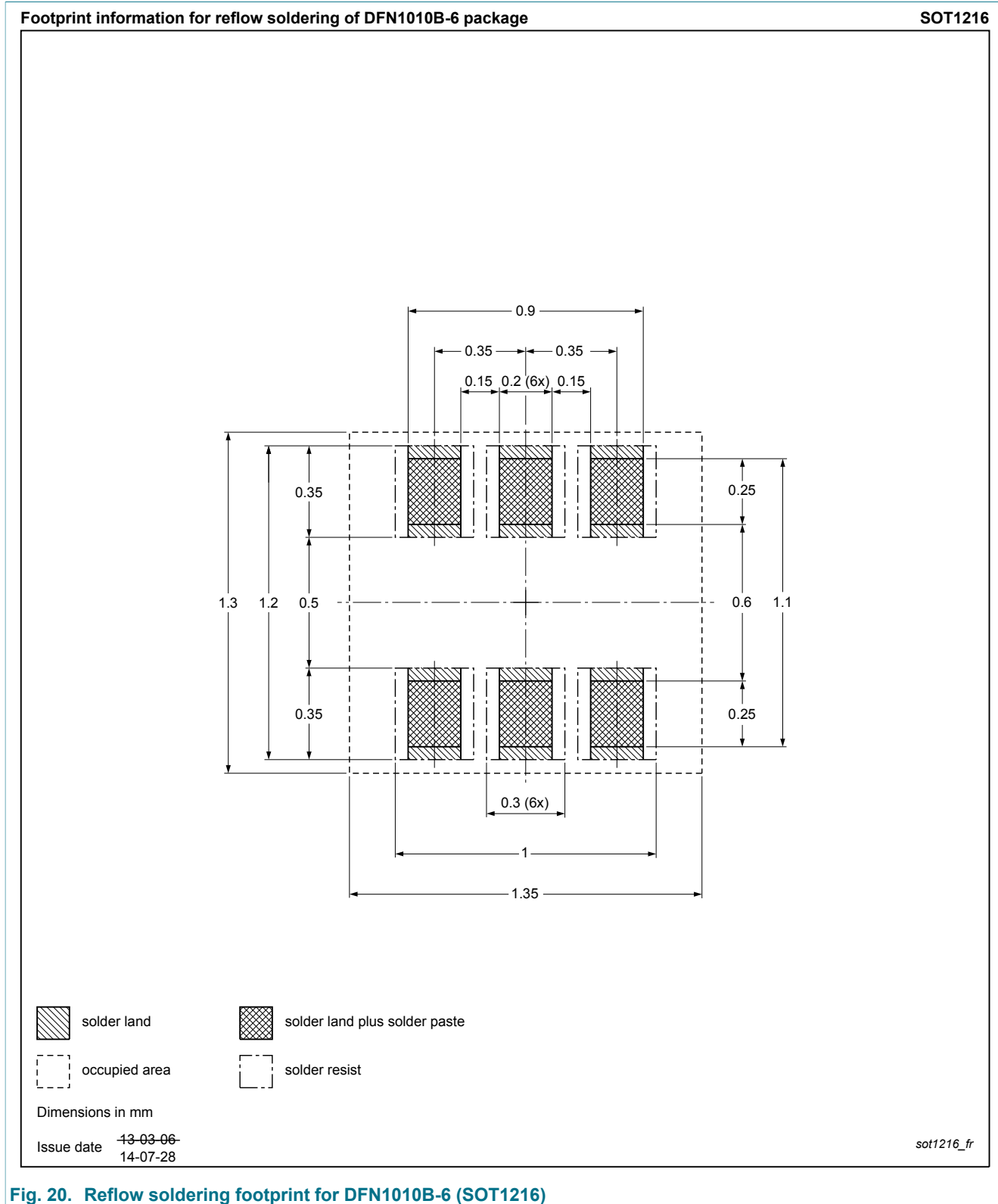
Unit	A	A <sub>1</sub>	b	D	D <sub>1</sub>	E	E <sub>1</sub>	e	e <sub>1</sub>	L
mm	min 0.34		0.15	1.05	0.32	0.95	0.22			0.125
	nom 0.37		0.18	1.10	0.35	1.00	0.25	0.35	0.275	0.155
	max 0.40	0.04	0.23	1.15	0.40	1.05	0.30			0.205

Note  
1. Dimension A is including plating thickness.

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1216						13-03-05 13-03-06

Fig. 19. Package outline DFN1010B-6 (SOT1216)

## 13. Soldering



**Fig. 20. Reflow soldering footprint for DFN1010B-6 (SOT1216)**

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NX7002BKXB v.2	20150630	Product data sheet	-	NX7002BKXB v.1
Modification:	<ul style="list-style-type: none"><li>Change of binary marking code position</li></ul>			
NX7002BKXB v.1	20141210	Product data sheet	-	-

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### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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