

NX3DV42

Dual high-speed USB 2.0 double-pole double-throw analog switch

Rev. 3.1 — 20 October 2016

Product data sheet

1. General description

The NX3DV42 is a double-pole double-throw analog switch suitable for use as an analog or digital multiplexer/demultiplexer. Its wide bandwidth and low bit-to-bit skew allows the NX3DV42 to pass high-speed differential signals with good signal integrity. Its high channel to channel crosstalk rejection results in minimal noise interference. The bandwidth is wide enough to pass high-speed USB 2.0 differential signals (480 Mb/s). It consists of two switches, each with two independent input/outputs (HSDn+ and HSDn-) and a common input/output (D+ or D-). One digital input (S) is used to select the switch position. When pin OE is HIGH, the switches are turned off. Schmitt trigger action at the select input (S) and output enable input (OE) makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 3.0 V to 4.3 V.

2. Features and benefits

- Supply voltage range from 3.0 V to 4.3 V
- 4 Ω typical ON resistance
- 7.3 pF typical ON capacitance
- 950 MHz typical bandwidth or data frequency
- Low crosstalk of -30 dB at 240 MHz
- Break-before-make switching
- ESD protection:
 - ◆ HBM JESD22-A114F Class 3A exceeds 4000 V
 - ◆ CDM AEC-Q100-011 revision B exceeds 1000 V
 - ◆ HBM exceeds 12000 V for power to GND protection
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Specified from -40 °C to +125 °C

3. Applications

- Cell phone, PDA, digital camera and notebook
- LCD monitor, TV and set-top box



4. Ordering information

Table 1. Ordering information

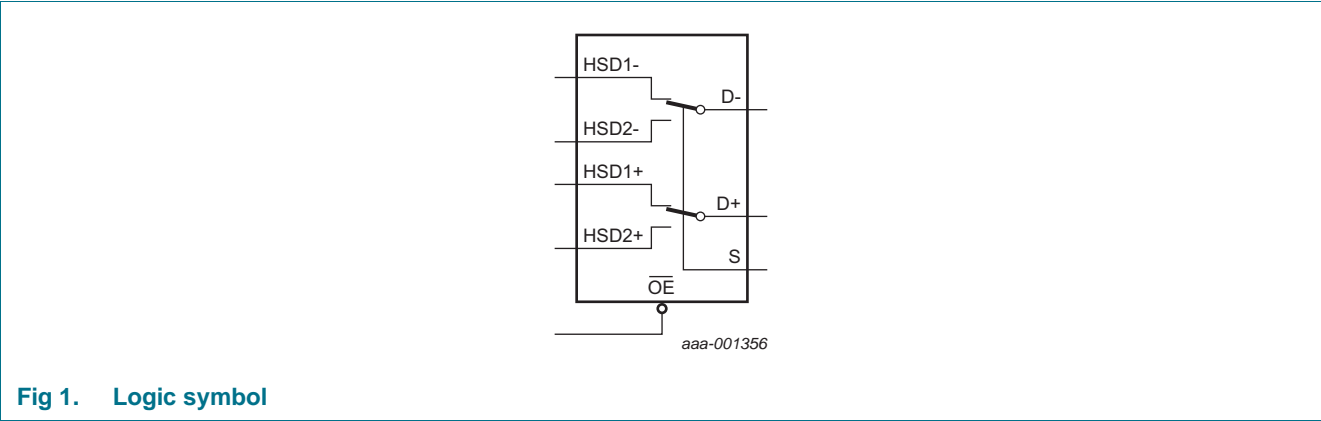
Type number	Package			
	Temperature range	Name	Description	Version
NX3DV42GU	−40 °C to +125 °C	XQFN10	plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm	SOT1160-1
NX3DV42GU10	−40 °C to +125 °C	XQFN10	plastic extremely thin small outline package; no leads; 10 terminals; body 1.3 x 1.6 x 0.5 mm	SOT1337-1
NX3DV42GU33	−40 °C to +125 °C	X2QFN10	plastic extremely thin small outline package; no leads; 10 terminals; body 1.3 x 1.6 x 0.33 mm	SOT1430-1

5. Marking

Table 2. Marking

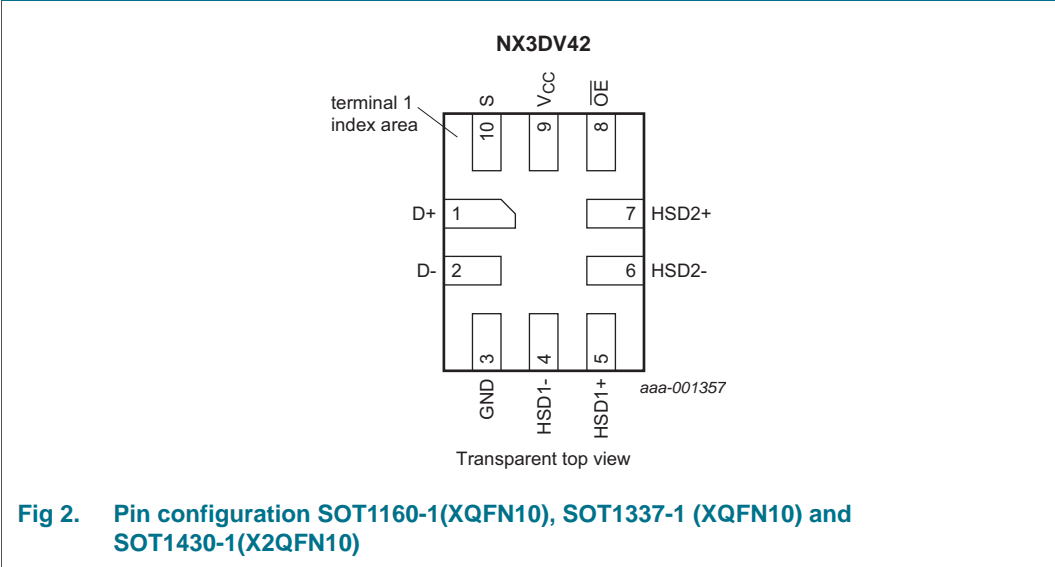
Type number	Marking code
NX3DV42GU	x4
NX3DV42GU10	x4
NX3DV42GU33	x4

6. Functional diagram



7. Pinning information

7.1 Pinning



7.2 Pin description

Table 3. Pin description

Symbol	SOT1160-1, SOT1337-1, SOT1430-1	Description
HSD1–, HSD2–	4, 6	independent input or output
HSD1+, HSD2+	5, 7	independent input or output
D+, D–	1, 2	common output or input
GND	3	ground (0 V)
$\overline{\text{OE}}$	8	output enable input (active LOW)
S	10	select input
V _{CC}	9	supply voltage

8. Functional description

Table 4. Function table^[1]

Input		Channel on
S	$\overline{\text{OE}}$	
L	L	HSD1+ and HSD1–
H	L	HSD2+ and HSD2–
X	H	switch off

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+5.5	V
V_I	input voltage	pins S and \overline{OE} [1]	-0.5	+5.5	V
V_{SW}	switch voltage		-0.5	+5.5	V
I_{IK}	input clamping current	$V_I < -0.5$ V	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V	-50	-	mA
I_{SW}	switch current		-	± 100	mA
I_{CC}	supply current		-	+50	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] For XQFN10 package: above 100 °C derate linearly with 4 mW/K.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		3.0	4.3	V
V_I	input voltage	pins S and \overline{OE}	0	4.5	V
V_{SW}	switch voltage	[1]	0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C

[1] To avoid sinking GND current from terminals D+ and D- when switch current flows in terminals HSDn+ and HSDn-, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals D+ and D-, no GND current will flow from terminals HSDn+ and HSDn-. In this case, there is no limit for the voltage drop across the switch.

11. Static characteristics

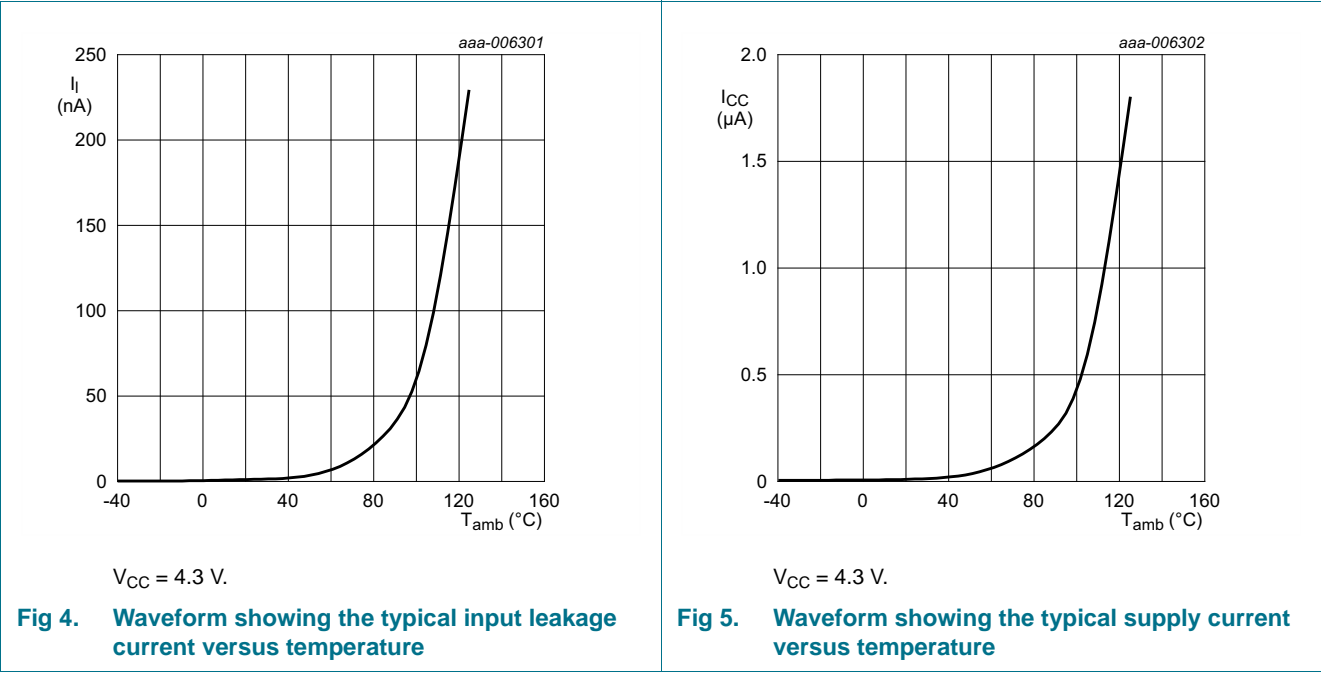
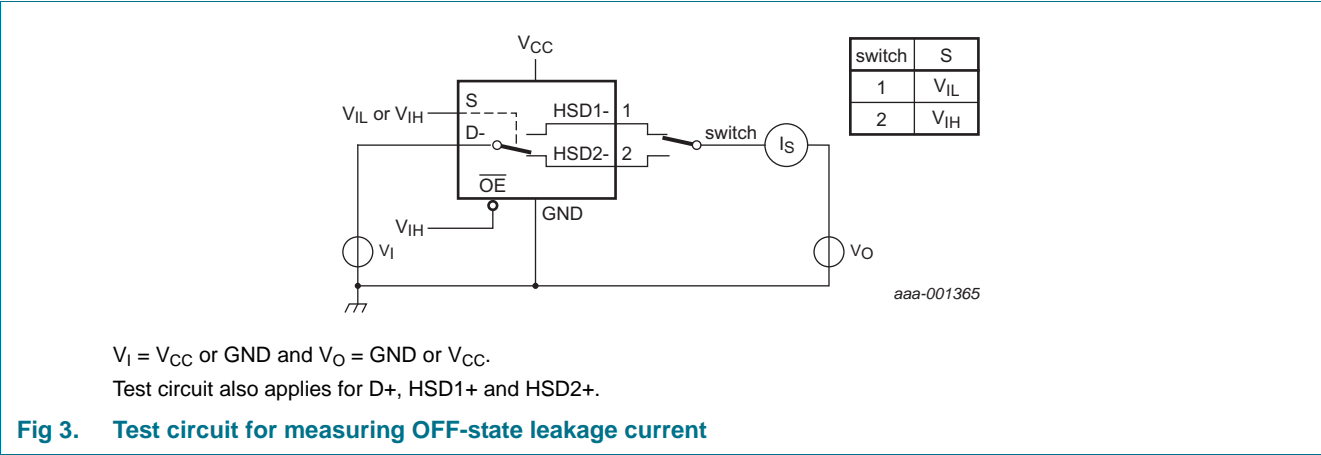
Table 7. Static characteristics

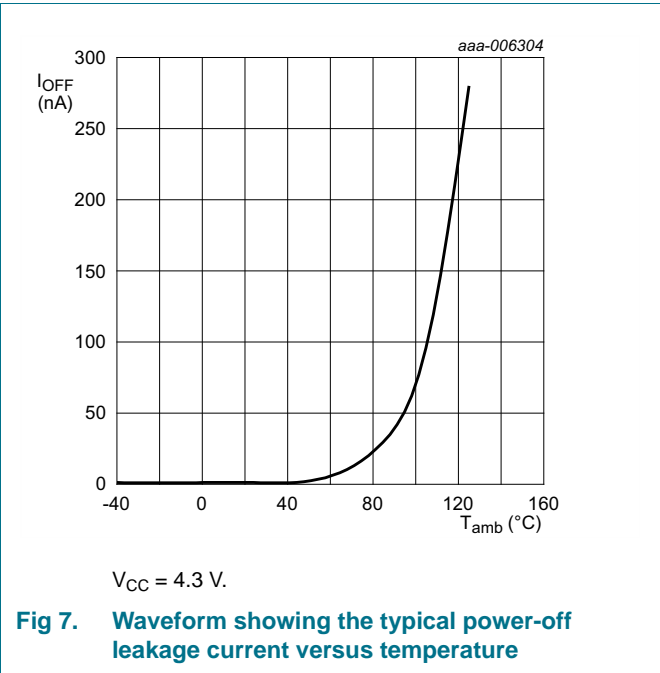
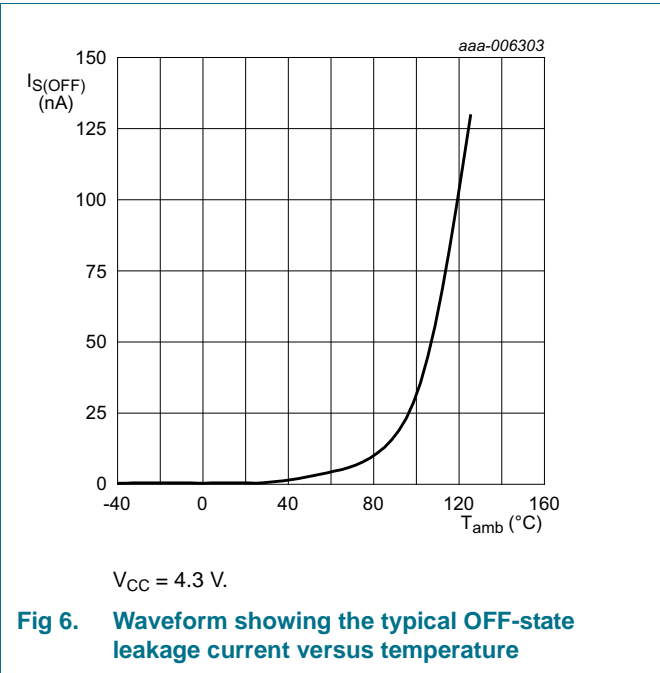
At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T _{amb} = –40 °C to +85 °C			T _{amb} = –40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 3.0 V to 3.6 V	1.3	-	-	1.3	-	V
		V _{CC} = 4.3 V	1.7	-	-	1.7	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 3.0 V to 3.6 V	-	-	0.5	-	0.5	V
		V _{CC} = 4.3 V	-	-	0.7	-	0.7	V
V _{IK}	input clamping voltage	V _{CC} = 3.0 V; I _I = –18 mA	-	-	–1.2	-	–1.2	V
I _I	input leakage current	pins S and $\overline{\text{OE}}$; V _I = GND to 4.3 V; V _{CC} = 4.3 V; see Figure 4	-	-	±1	-	±10	μA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 4.3 V; see Figure 3 and Figure 6	-	-	±1	-	±2	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 4.3 V; V _{CC} = 0 V; see Figure 7	-	-	±1	-	±10	μA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{CC} = 4.3 V; V _{SW} = GND or V _{CC} ; see Figure 5	-	-	1	-	10	μA
ΔI _{CC}	additional supply current	V _I = 2.6 V; V _{CC} = 4.3 V; V _{SW} = GND or V _{CC}	-	-	10	-	10	μA
		V _I = 1.8 V; V _{CC} = 4.3 V; V _{SW} = GND or V _{CC}	-	-	15	-	15	μA
C _I	input capacitance	pins S and OE	-	1.0	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance	pins HSDn+ and HSDn–; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	2.8	-	-	-	pF
C _{S(ON)}	ON-state capacitance	pins D+ and D–; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	7.3	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

11.1 Test circuit and graphs





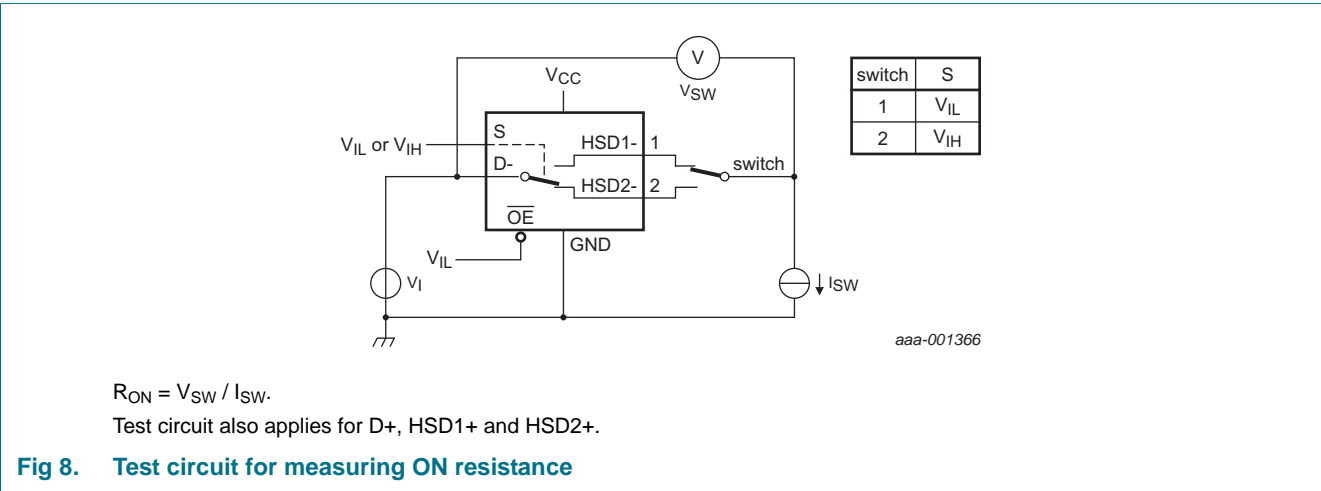
11.2 ON resistance

Table 8. ON resistance
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_amb = -40 °C to +85 °C			T_amb = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
R_ON	ON resistance	V_I = 0.4 V; I_SW = 8 mA; see Figure 8						
		V_CC = 3.0 V	-	3.9	6.5	-	10	Ω
ΔR_ON	ON resistance mismatch between channels	V_I = 0.4 V; I_SW = 8 mA [2]						
		V_CC = 3.0 V	-	0.65	-	-	-	Ω

- [1] Typical values are measured at T_amb = 25 °C.
[2] Measured at identical V_CC, temperature and input voltage.

11.3 ON resistance test circuit



12. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	T _{amb} = –40 °C to +85 °C			T _{amb} = –40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	HSDn+ to D+ or HSDn– to D– or D+ to HSDn+ or D– to HSDn–; see Figure 9 ^{[2][3]}						
		V _{CC} = 3.3 V	-	0.25	-	-	-	ns
t _{en}	enable time	S or $\overline{\text{OE}}$ to D+ or D–; see Figure 10 ^[4]						
		V _{CC} = 3.0 V to 3.6 V	-	11.2	30	-	40	ns
t _{dis}	disable time	S or $\overline{\text{OE}}$ to D+ or D–; see Figure 10 ^[5]						
		V _{CC} = 3.0 V to 3.6 V	-	3.9	25	-	30	ns
t _{b-m}	break-before-make time	see Figure 11 ^[3]						
		V _{CC} = 3.0 V to 3.6 V	2.0	5.9	-	2.0	-	ns
t _{sk(p)}	pulse skew time	see Figure 9						
		V _{CC} = 3.0 V to 3.6 V ^[3]	-	20	-	-	-	ps
t _{jit}	jitter time	R _L = 50 Ω; C _L = 5 pF; t _r , t _f = 500 ps (10 % to 90 %) at 480 Mbs (PRBS = 2 ¹⁵ – 1) ^[3]	-	200	-	-	-	ps

[1] Typical values are measured at T_{amb} = 25 °C, C_L = 5 pF and V_{CC} = 3.3 V.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Guaranteed by design.

[4] t_{en} is the same as t_{PZH}.

[5] t_{dis} is the same as t_{PHZ}.

12.1 Waveforms and test circuits

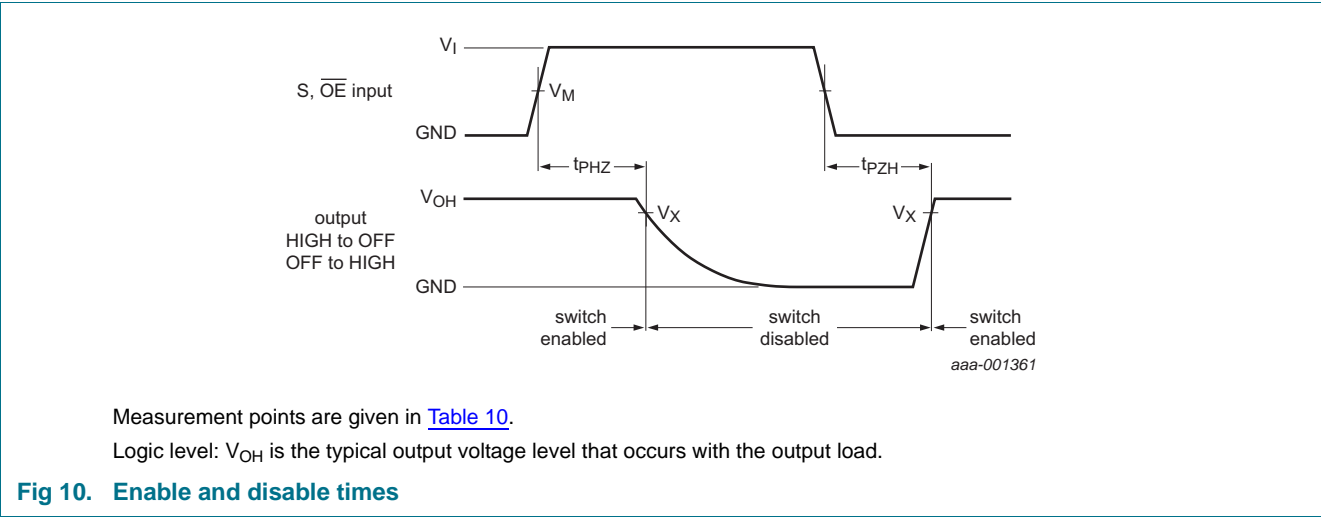
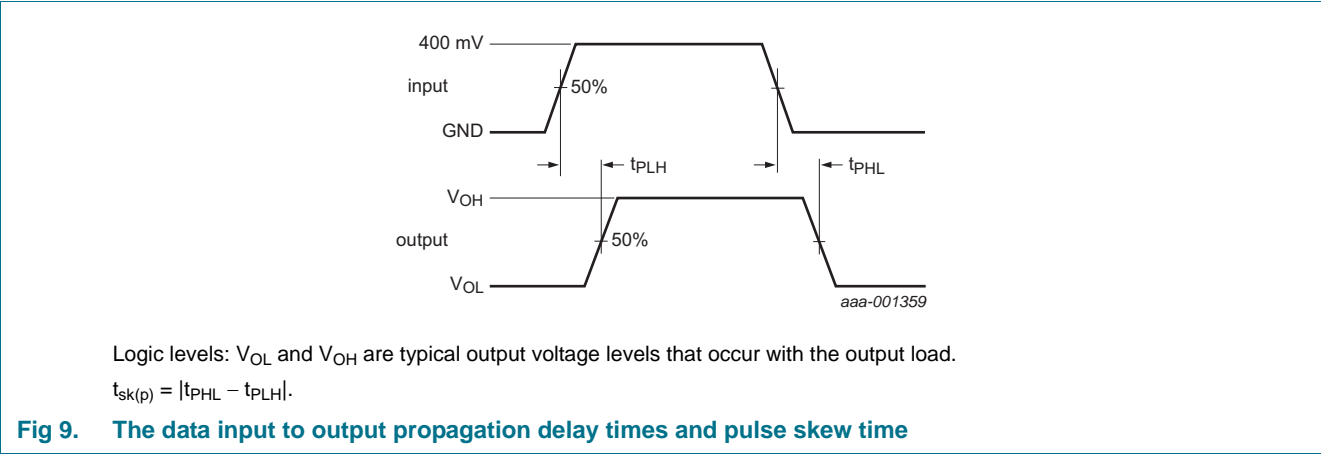
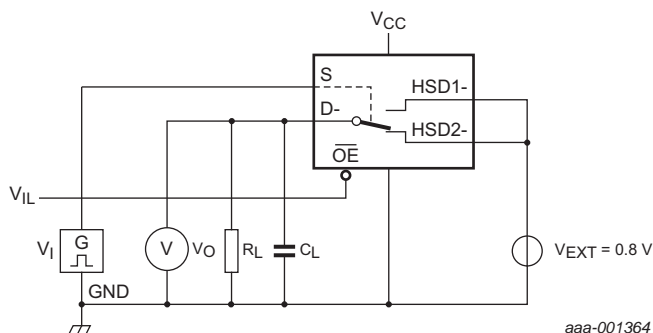
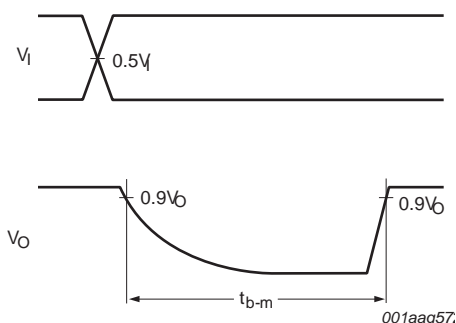


Table 10. Measurement points

Supply voltage	Input		Output
V_{CC}	V_M	V_I	V_X
3.0 V to 3.6 V	$0.5V_{CC}$	V_{CC}	$0.9V_{OH}$



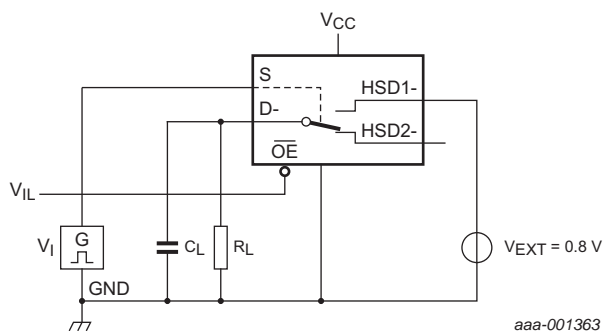
a. Test circuit.



b. Input and output measurement points.

Test circuit also applies for D+, HSD1+ and HSD2+.

Fig 11. Test circuit for measuring break-before-make timing



Test circuit also applies for D+, HSD1+ and HSD2+.

Test data is given in [Table 11](#).

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

V_I may be connected to S or \overline{OE} .

Fig 12. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load	
V _{CC}	V _I	t _r , t _f	C _L	R _L
3.0 V to 3.6 V	V _{CC}	≤ 2.5 ns	5 pF	50 Ω

12.2 Additional dynamic characteristics

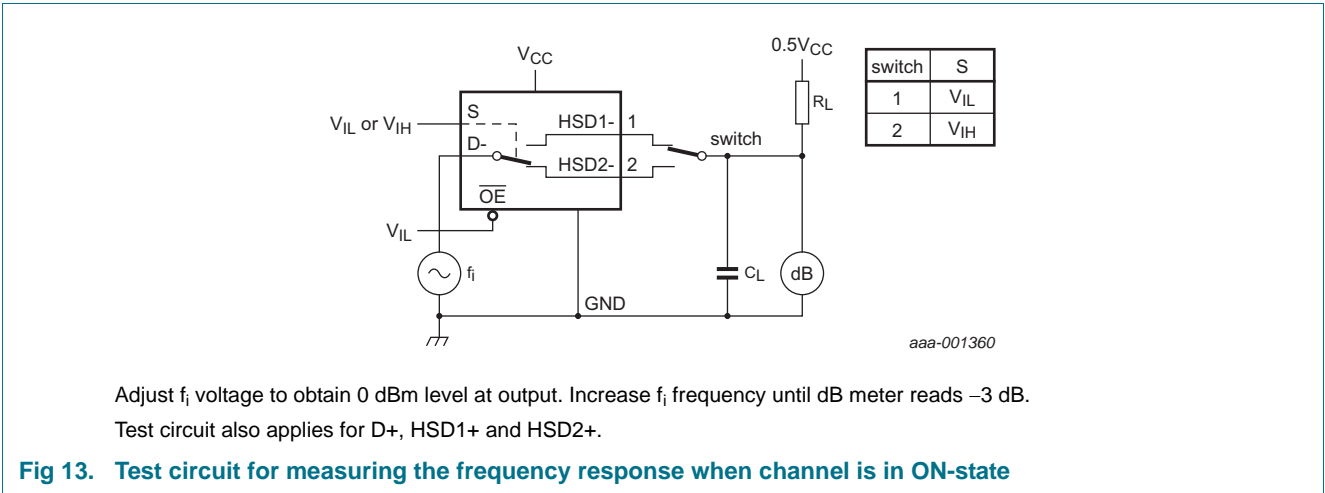
Table 12. Additional dynamic characteristics

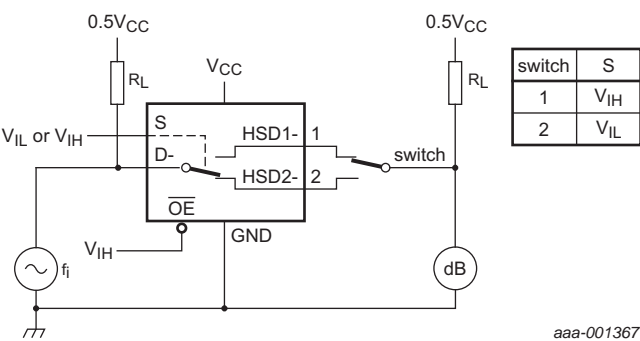
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); t_r = t_f < 2.5 ns.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			Unit
			Min	Typ ^[2]	Max	
f _(-3dB)	–3 dB frequency response	R _L = 50 Ω; see Figure 13 ^[1]				
		C _L = 0 pF; V _{CC} = 3.0 V to 3.6 V	-	950	-	MHz
		C _L = 5 pF; V _{CC} = 3.0 V to 3.6 V	-	450	-	MHz
α _{iso}	isolation (OFF-state)	f _i = 240 MHz; R _L = 50 Ω; see Figure 14 ^[1]				
		V _{CC} = 3.0 V to 3.6 V	-	–30	-	dB
Xtalk	crosstalk	between switches; f _i = 240 MHz; R _L = 50 Ω; see Figure 15 ^[1]				
		V _{CC} = 3.0 V to 3.6 V	-	–30	-	dB

- [1] f_i is biased at 0.5V_{CC}.
- [2] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

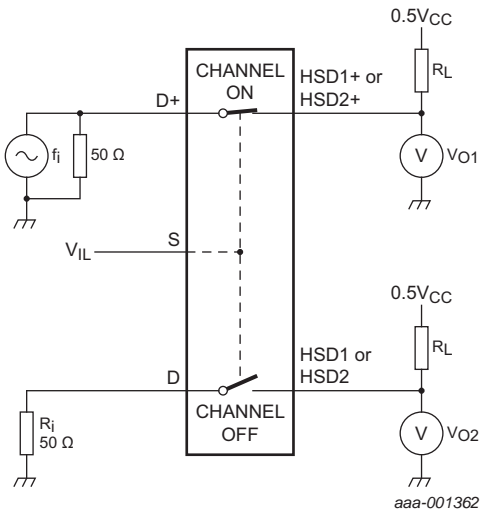
12.3 Test circuits





Adjust f_i voltage to obtain 0 dBm level at input.
Test circuit also applies for D+, HSD1+ and HSD2+.

Fig 14. Test circuit for measuring isolation (OFF-state)



$20 \log_{10} (V_{O2}/V_{O1})$ or $20 \log_{10} (V_{O1}/V_{O2})$.

Fig 15. Test circuit for measuring crosstalk between switches

13. Package outline

XQFN10: plastic, extremely thin quad flat package; no leads;
10 terminals; body 1.40 x 1.80 x 0.50 mm

SOT1160-1

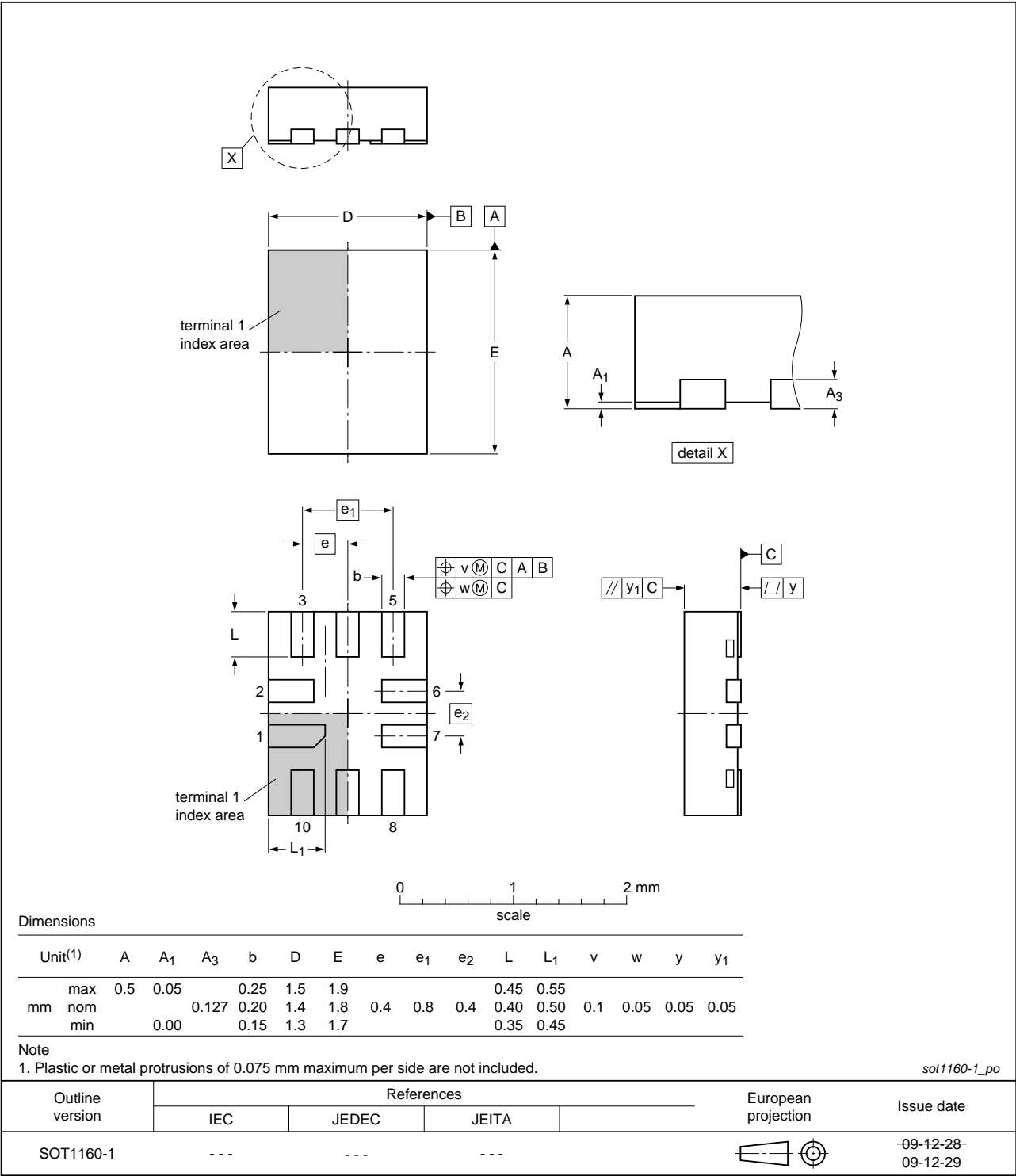


Fig 16. Package outline SOT1160-1 (XQFN10)

XQFN10: plastic extremely thin small outline package; no leads; 10 terminals; body 1.3 x 1.6 x 0.5 mm SOT1337-1

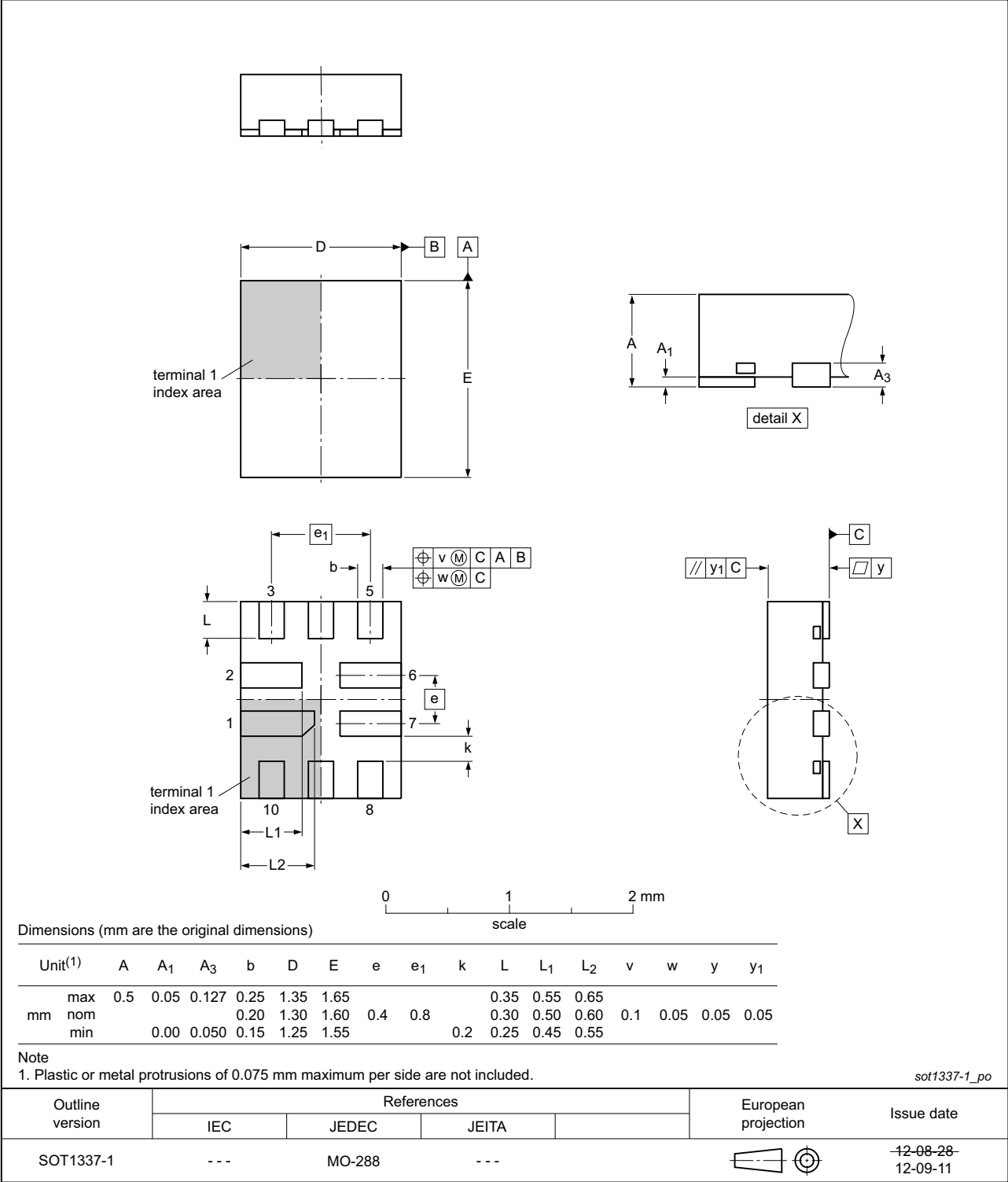


Fig 17. Package outline SOT1337-1 (XQFN10)

X2QFN10: plastic extremely thin small outline package; no leads; 10 terminals; body 1.6 x 1.3 x 0.33 mm

SOT1430-1

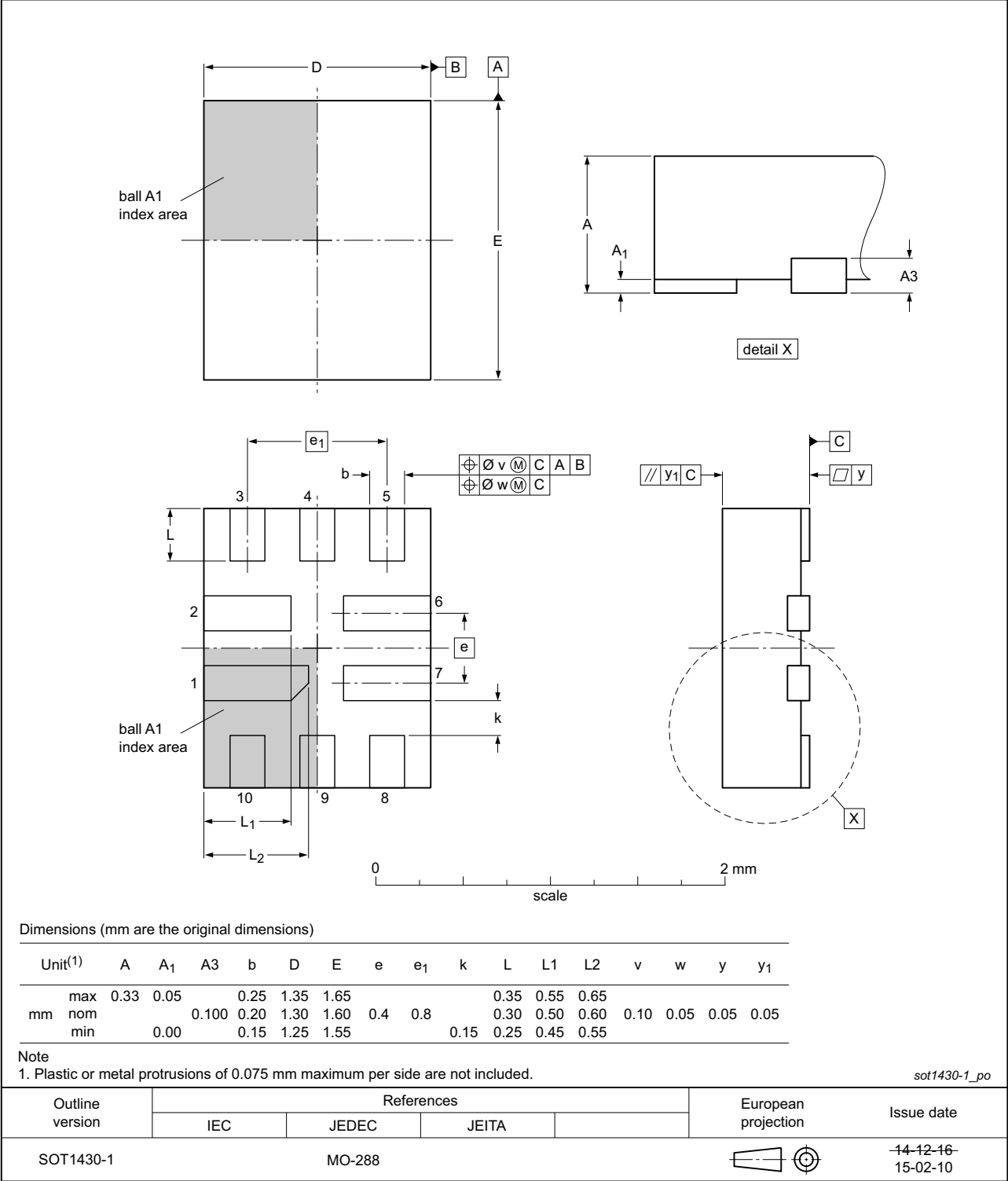


Fig 18. Package outline X2QFN10

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
LCD	Liquid Crystal Display
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3DV42 v.3.1	20161020	Product data sheet	-	NX3DV42 v.3
Modifications:	<ul style="list-style-type: none"> Added NX3DV42GU33 Removed NX3DV42GM 			
NX3DV42 v.3	20130213	Product data sheet	-	NX3DV42 v.2
Modifications:	<ul style="list-style-type: none"> Values added for $T_{amb} = +125\text{ °C}$ throughout the data sheet. Type number NX3DV42GU10 added (Table 1). Marking code for type number NX3DV42GU10 added (Table 2). Package outline drawing SOT1337-1 added (Figure 17). 			
NX3DV42 v.2	20120618	Product data sheet	-	NX3DV42 v.1
Modifications:	<ul style="list-style-type: none"> Package outline drawing SOT1049-2 changed to SOT1049-3 (Figure 17). 			
NX3DV42 v.1	20120103	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 20 October 2016

Document identifier: NX3DV42