

# MOSFET – Power, Single P-Channel

–40 V, 13.5 mΩ, –53 A

## Product Preview NVTYS014P04M8L

### Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	−40	V
Gate-to-Source Voltage			$V_{GS}$	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 4)	Steady State	$T_C = 25^{\circ}\text{C}$	$I_D$	−53	A
		$T_C = 100^{\circ}\text{C}$		−39	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)	Steady State	$T_C = 25^{\circ}\text{C}$	$P_D$	88	W
		$T_C = 100^{\circ}\text{C}$		44	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 4)	Steady State	$T_A = 25^{\circ}\text{C}$	$I_D$	−10.4	A
		$T_A = 100^{\circ}\text{C}$		−7.3	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 25^{\circ}\text{C}$	$P_D$	3.1	W
		$T_A = 100^{\circ}\text{C}$		1.6	
Pulsed Drain Current	$T_A = 25^{\circ}\text{C}, t_p = 10\ \mu\text{s}$		$I_{DM}$	210	A
Operating Junction and Storage Temperature Range			$T_J, T_{stg}$	−55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)			$I_S$	50.6	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			$T_L$	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Drain) (Notes 1, 2, 4)	$R_{\theta JC}$	2.47	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	38.7	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Assumes heat-sink sufficiently large to maintain constant case temperature independent of device power.
3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

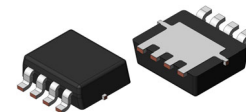
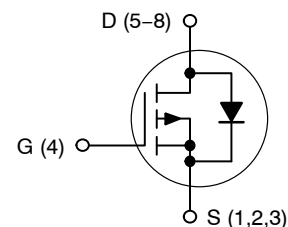


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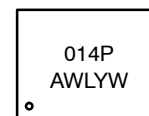
$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
–40 V	13.5 mΩ @ –10 V	–53 A
	20 mΩ @ –4.5 V	

### P-Channel MOSFET



LFPK8  
3.3x3.3  
CASE 760AD

### MARKING DIAGRAM



014P = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue product without notice.

# NVTYS014P04M8L

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	-40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			21.6		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = -40\text{ V}$			-1.0	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -420\text{ }\mu\text{A}$	-1		-3	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-4.5		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -25\text{ A}$		10.5	13.5	m $\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -20\text{ A}$		14.6	20	

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 100\text{ KHz}, V_{DS} = -25\text{ V}$		1690		pF
Output Capacitance	$C_{oss}$			595		
Reverse Transfer Capacitance	$C_{rss}$			23		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10\text{ V}, V_{DS} = -20\text{ V}, I_D = -25\text{ A}$		27		nC
Threshold Gate Charge	$Q_{G(TH)}$			2.0		
Gate-to-Source Charge	$Q_{GS}$			4.5		
Gate-to-Drain Charge	$Q_{GD}$			8		

### SWITCHING CHARACTERISTICS, $V_{GS} = -10\text{ V}$ (Note 6)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -10\text{ V}, V_{DS} = -20\text{ V}, I_D = -25\text{ A}, R_G = 6\text{ }\Omega$		8		ns
Rise Time	$t_r$			4		
Turn-Off Delay Time	$t_{d(off)}$			126		
Fall Time	$t_f$			48		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -25 A	T <sub>J</sub> = 25°C		-0.9	-1.25	V
			T <sub>J</sub> = 175°C		-0.73		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = -25 A		38		ns	
Charge Time	t <sub>a</sub>			19			
Discharge Time	t <sub>b</sub>			20			
Reverse Recovery Charge	Q <sub>RR</sub>				26	40	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

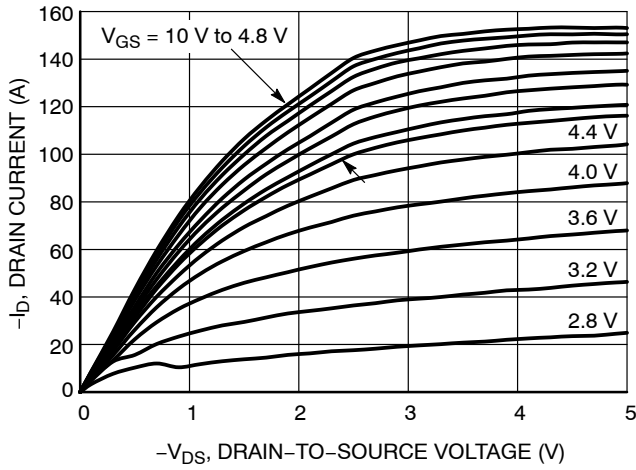


Figure 1. On-Region Characteristics

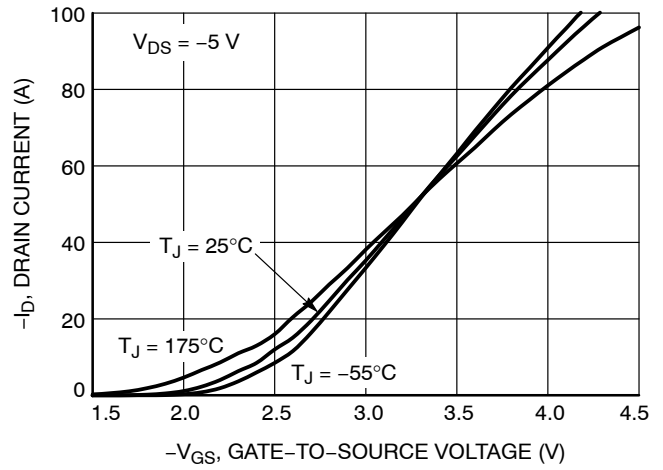


Figure 2. Transfer Characteristics

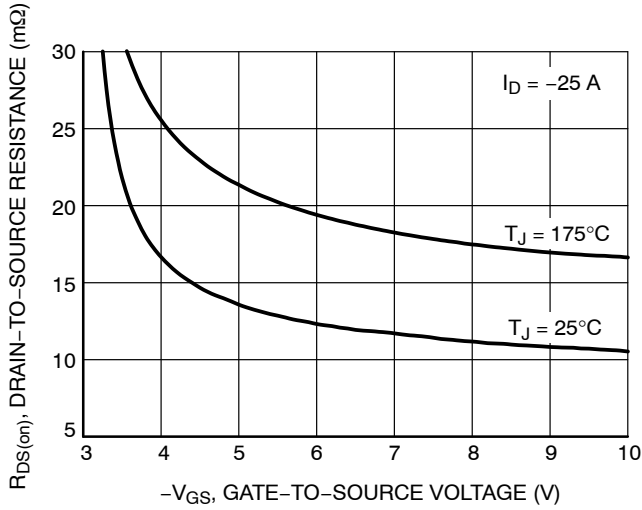


Figure 3. On-Resistance vs. Gate-to-Source Voltage

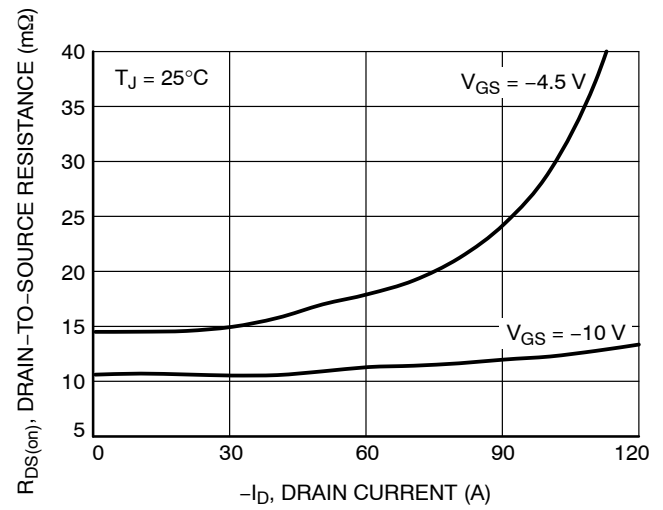


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

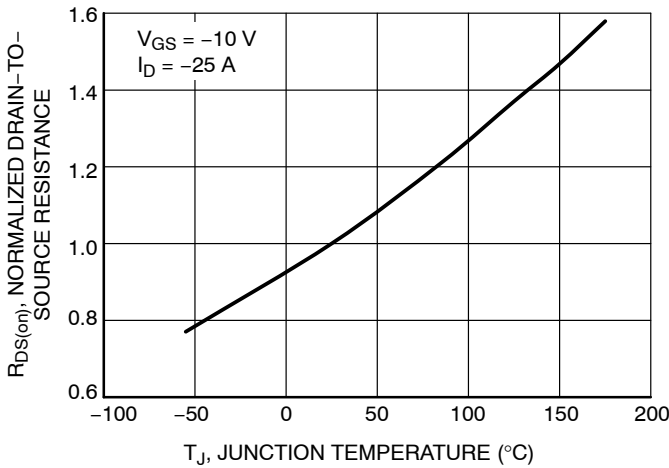


Figure 5. On-Resistance Variation with Temperature

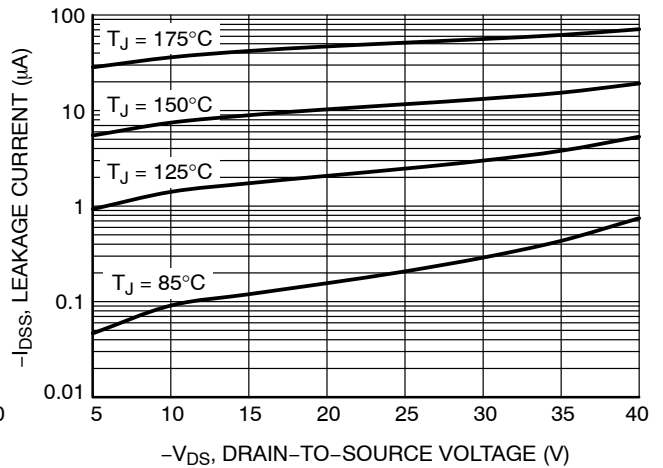


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

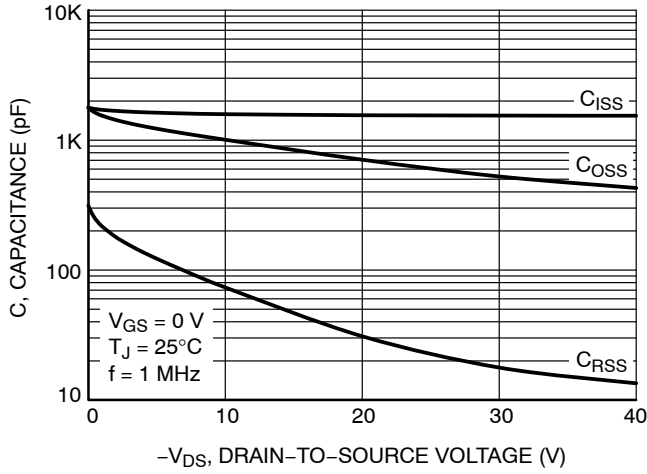


Figure 7. Capacitance Variation

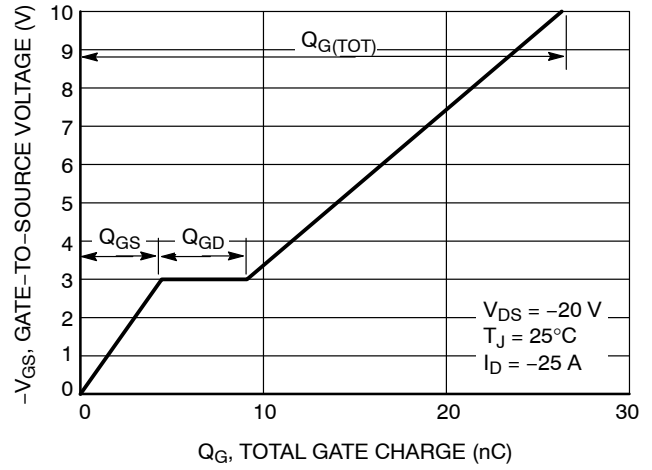


Figure 8. Gate-to-Source Voltage vs. Total Charge

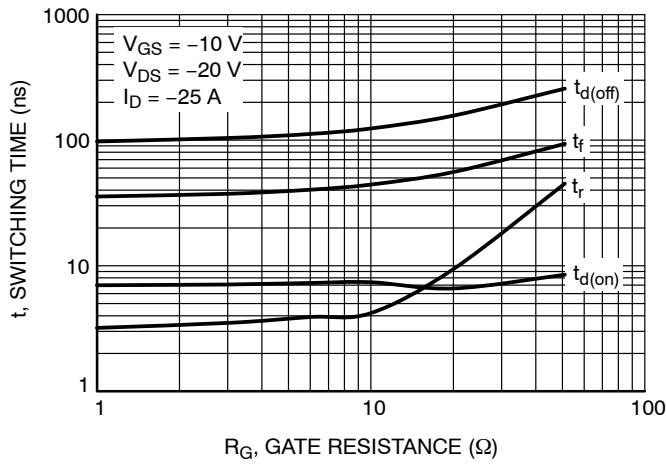


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

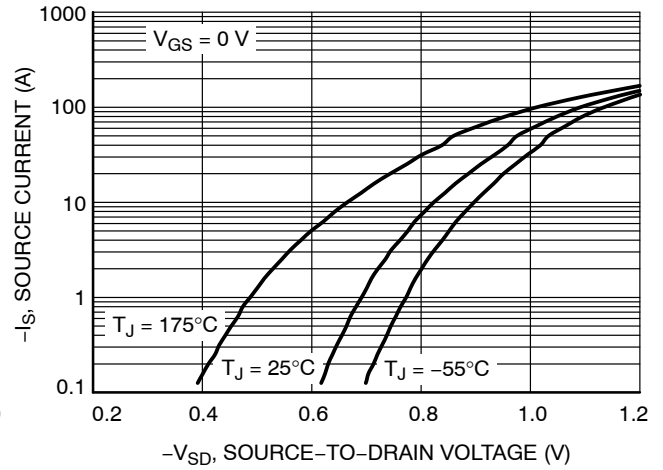


Figure 10. Diode Forward Voltage vs. Current

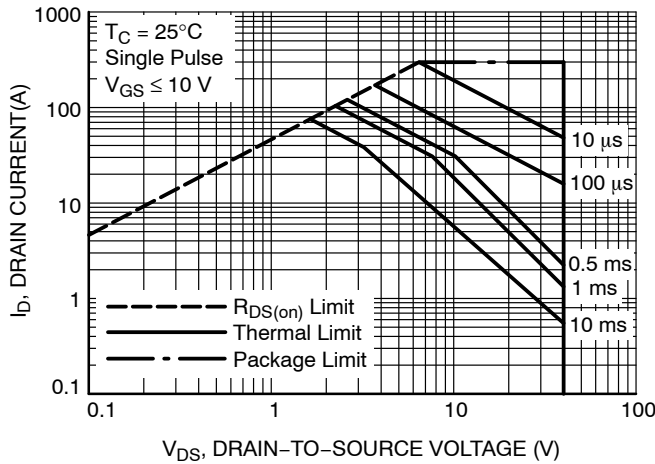


Figure 11. Maximum Rated Forward Biased Safe Operating Area

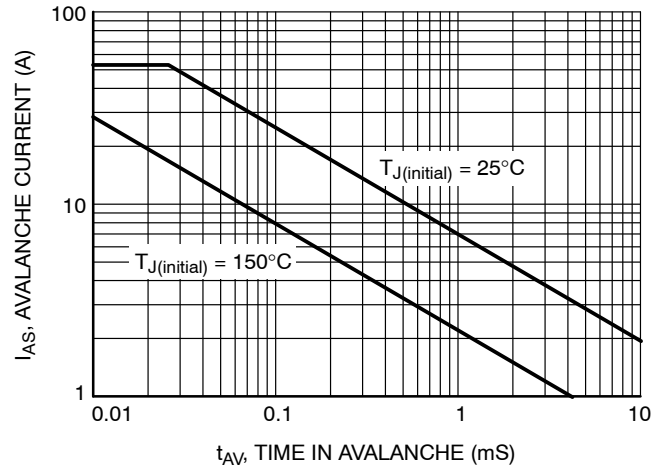
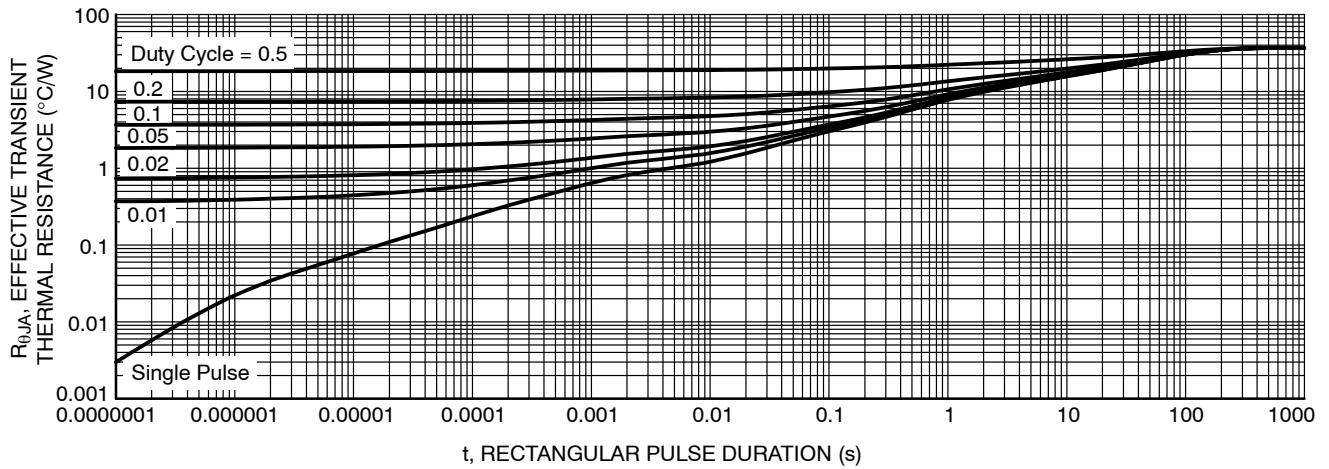


Figure 12. Maximum Drain Current vs. Time in Avalanche

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## TYPICAL CHARACTERISTICS



**Figure 13. Thermal Response**

### DEVICE ORDERING INFORMATION

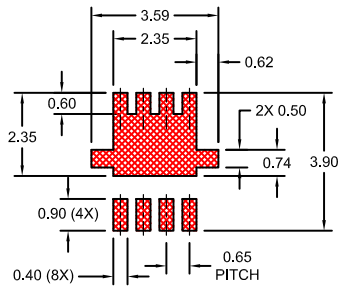
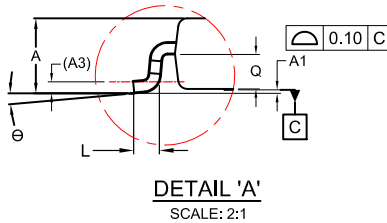
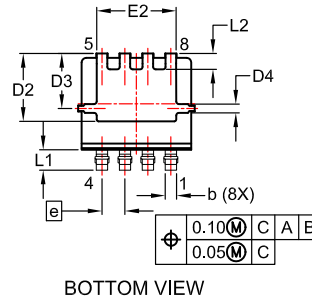
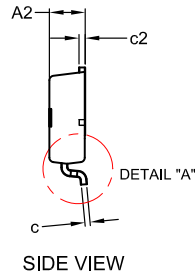
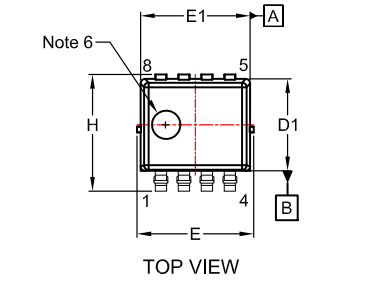
Device	Marking	Package	Shipping <sup>†</sup>
NVTYS014P04M8LWTWG	014P	LFPK33	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NVTYS014P04M8L

## PACKAGE DIMENSIONS

### LFPAK8 3.3x3.3, 0.65P CASE 760AD ISSUE E




#### LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR  
PB-FREE STRATEGY AND SOLDERING DETAILS,  
PLEASE DOWNLOAD THE ON SEMICONDUCTOR  
SOLDERING AND MOUNTING TECHNIQUES  
REFERENCE MANUAL, SOLDERM/D.

#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS OR BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.95	1.05	1.15
A1	0.00	0.05	0.10
A2	0.95	1.00	1.05
A3	0.15 REF		
b	0.27	0.32	0.37
c	0.12	0.17	0.22
c2	0.12	0.17	0.22
D1	2.50	2.60	2.70
D2	1.82	1.92	2.02
D3	1.46	1.56	1.66
D4	0.20	0.25	0.30
E	3.20	3.30	3.40
E1	3.00	3.10	3.20
E2	2.15	2.25	2.35
e	0.65 BSC		
H	3.20	3.30	3.40
L	0.25	0.37	0.50
L1	0.48	0.58	0.68
L2	0.35	0.45	0.55
Q	0.45	0.50	0.55
theta	0°	4°	8°

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