

MOSFET - Power, Single N-Channel

100 V, 26 mΩ, 28 A

NVTF5027N10MCL

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVTF5027N10MCL – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	100	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^{\circ}\text{C}$	I_D	28	A
		$T_C = 100^{\circ}\text{C}$		20	
Power Dissipation $R_{\theta JC}$ (Note 1)		$T_C = 25^{\circ}\text{C}$	P_D	46	W
		$T_C = 100^{\circ}\text{C}$		23	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	7.4	A
		$T_A = 100^{\circ}\text{C}$		5.2	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		$T_A = 25^{\circ}\text{C}$	P_D	3.1	W
		$T_A = 100^{\circ}\text{C}$		1.6	
Pulsed Drain Current	$T_A = 25^{\circ}\text{C}$, $t_p = 10\text{ }\mu\text{s}$		I_{DM}	119	A
Operating Junction and Storage Temperature Range			T_J , T_{stg}	-55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	35	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 1.3\text{ A}$)			E_{AS}	414	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 1)	$R_{\theta JC}$	3.3	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	47.7	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.

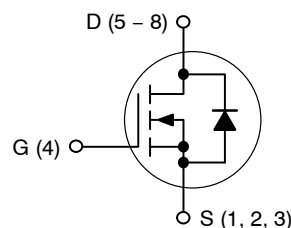


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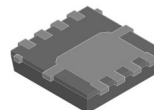
www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	26 mΩ @ 10 V	28 A
	35 mΩ @ 4.5 V	

N-Channel

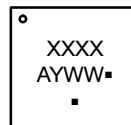
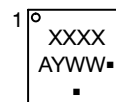


WDFN8
(μ8FL)
CASE 511AB



WDFNW8
(μ8FL WF)
CASE 515AN

MARKING DIAGRAMS



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVTFS027N10MCL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			53		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 38\text{ }\mu\text{A}$	1		3	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-6		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 7\text{ A}$		21	26	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$		28	35	
Forward Transconductance	g_{FS}	$V_{DS} = 10\text{ V}, I_D = 7\text{ A}$		25		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$		800		pF
Output Capacitance	C_{OSS}			300		
Reverse Transfer Capacitance	C_{RSS}			4		
Gate Resistance	R_G			0.41		Ω
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 50\text{ V}; I_D = 7\text{ A}$		5.5		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}; I_D = 7\text{ A}$		11.5		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}; I_D = 7\text{ A}$		1.3		nC
Gate-to-Source Charge	Q_{GS}			2.1		
Gate-to-Drain Charge	Q_{GD}			1.2		
Plateau Voltage	V_{GP}			2.5		V

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 7\text{ A}$		7.4		ns
Rise Time	t_r			2		
Turn-Off Delay Time	$t_{d(OFF)}$			19		
Fall Time	t_f			2.9		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 7\text{ A}, T_J = 25^\circ\text{C}$		0.84	1.3	V
		$V_{GS} = 0\text{ V}, I_S = 7\text{ A}, T_J = 125^\circ\text{C}$		0.73		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 3\text{ A}$		28		ns
Reverse Recovery Charge	Q_{RR}			17		nC
Charge Time	t_a			13.9		ns
Discharge Time	t_b			14.2		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

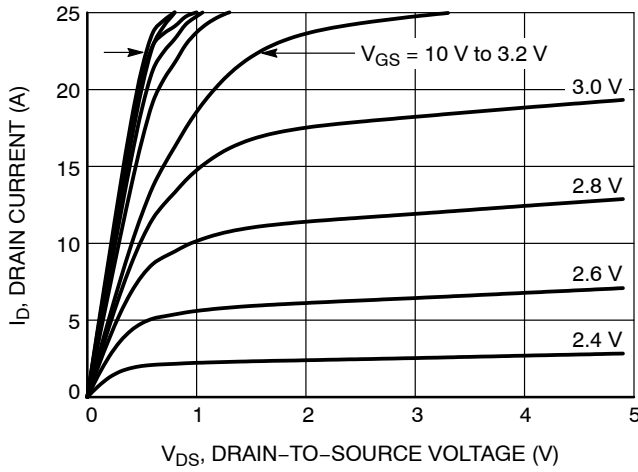


Figure 1. On-Region Characteristics

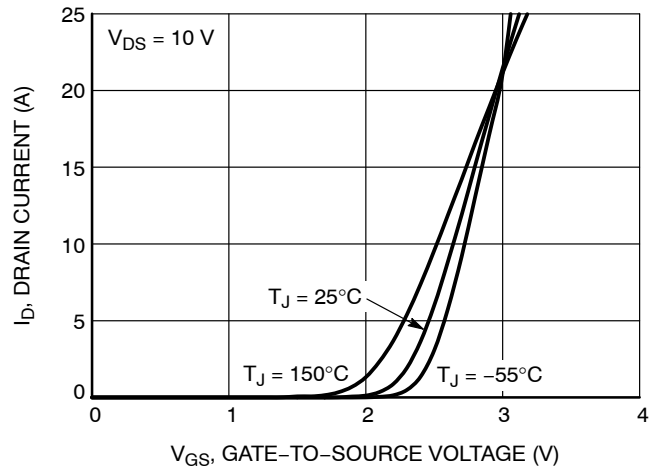


Figure 2. Transfer Characteristics

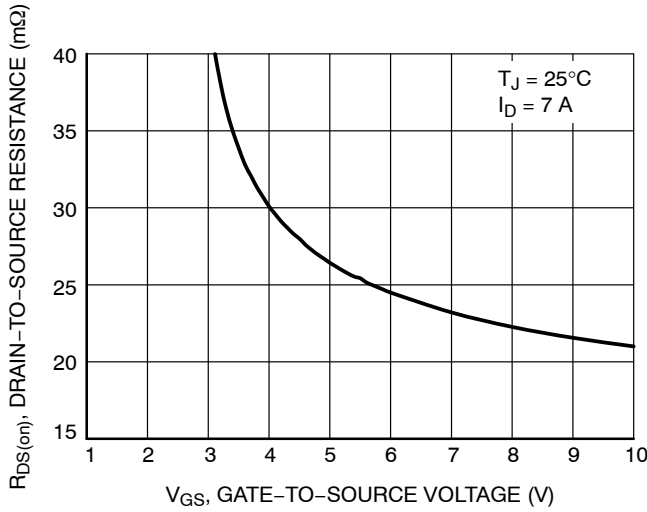


Figure 3. On-Resistance vs. Gate-to-Source Voltage

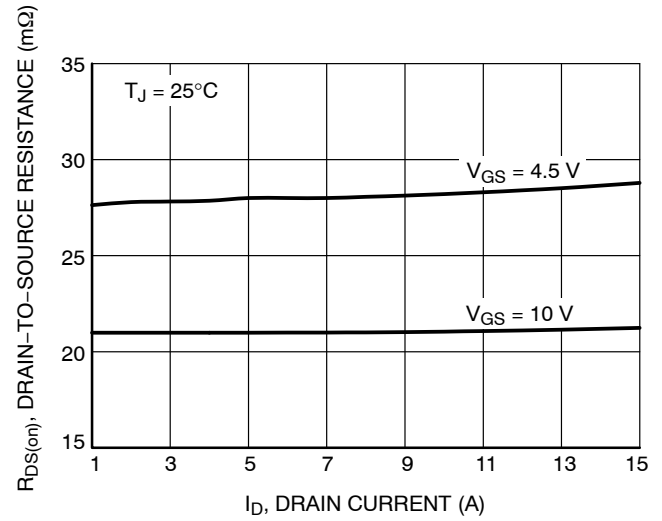


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

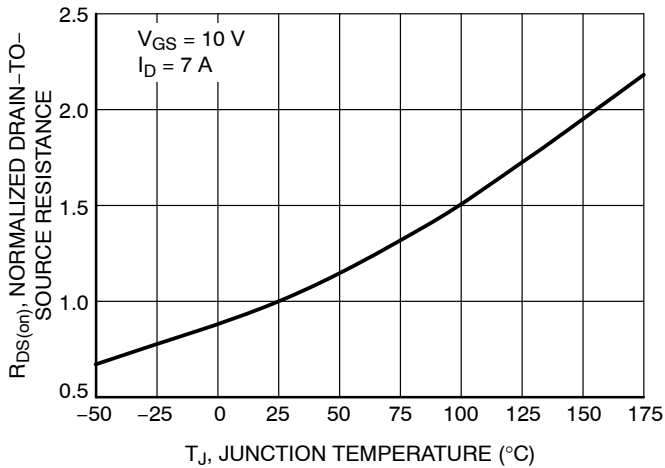


Figure 5. On-Resistance Variation with Temperature

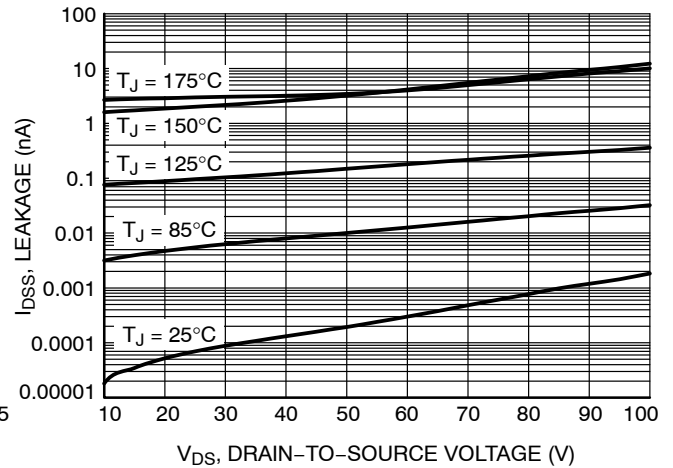


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

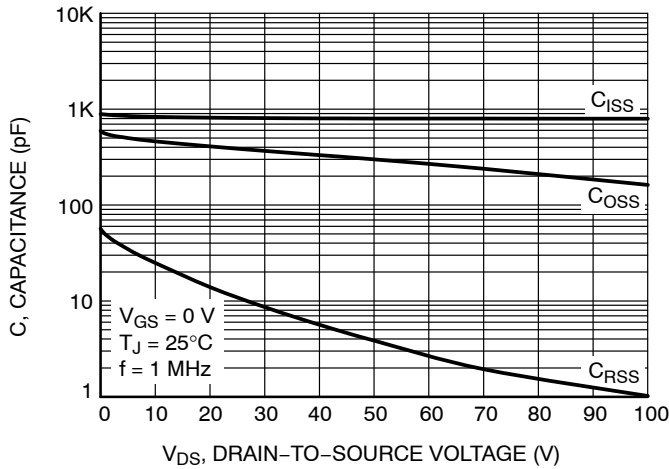


Figure 7. Capacitance Variation

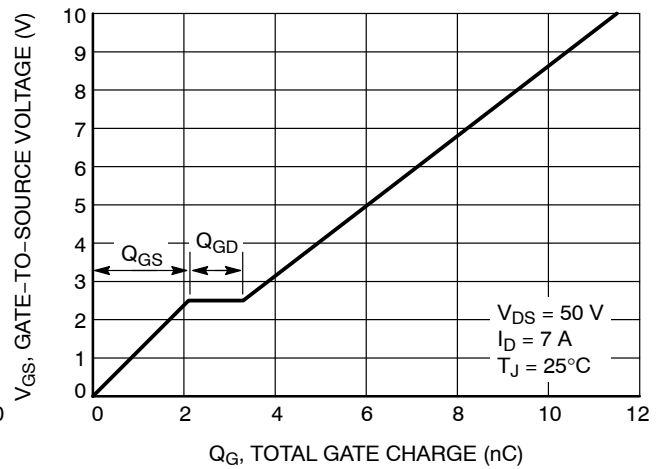


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

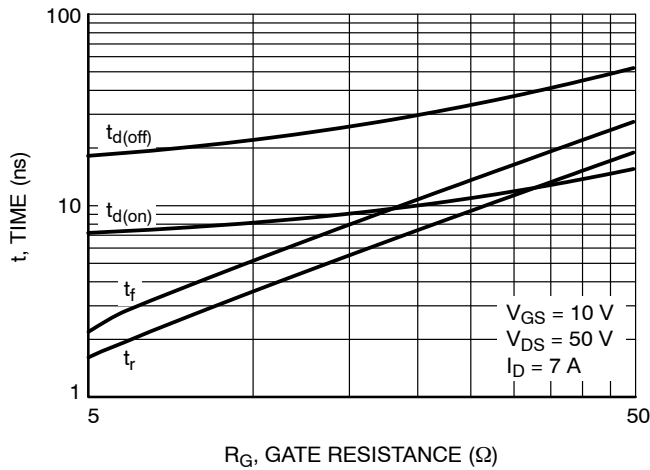


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

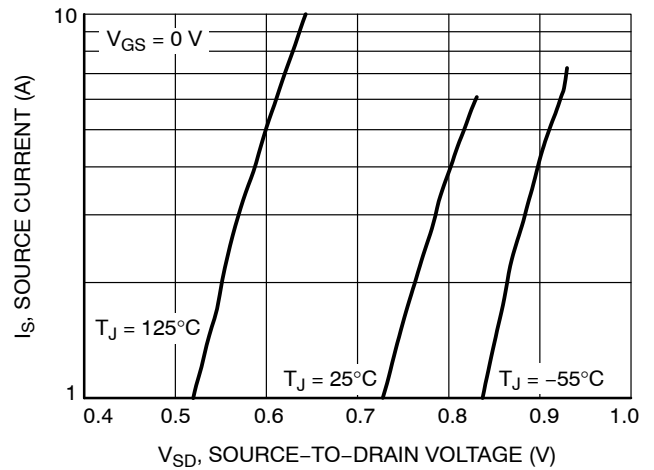


Figure 10. Diode Forward Voltage vs. Current

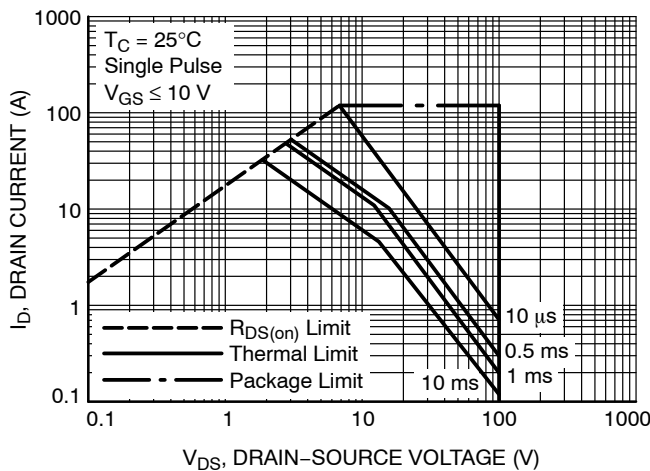


Figure 11. Safe Operating Area

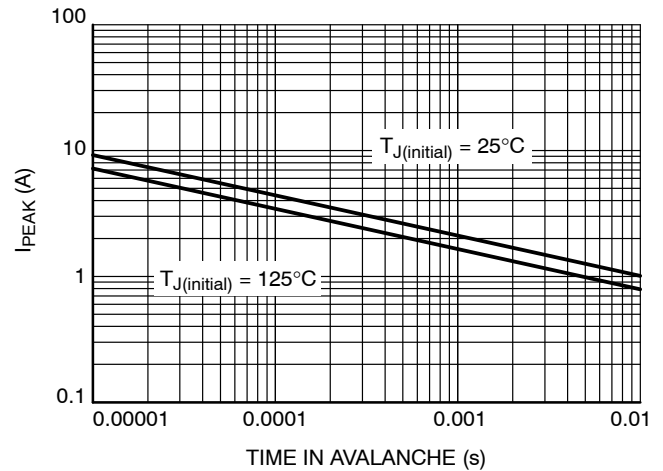


Figure 12. Maximum Drain Current vs. Time in Avalanche

NVTFS027N10MCL

TYPICAL CHARACTERISTICS

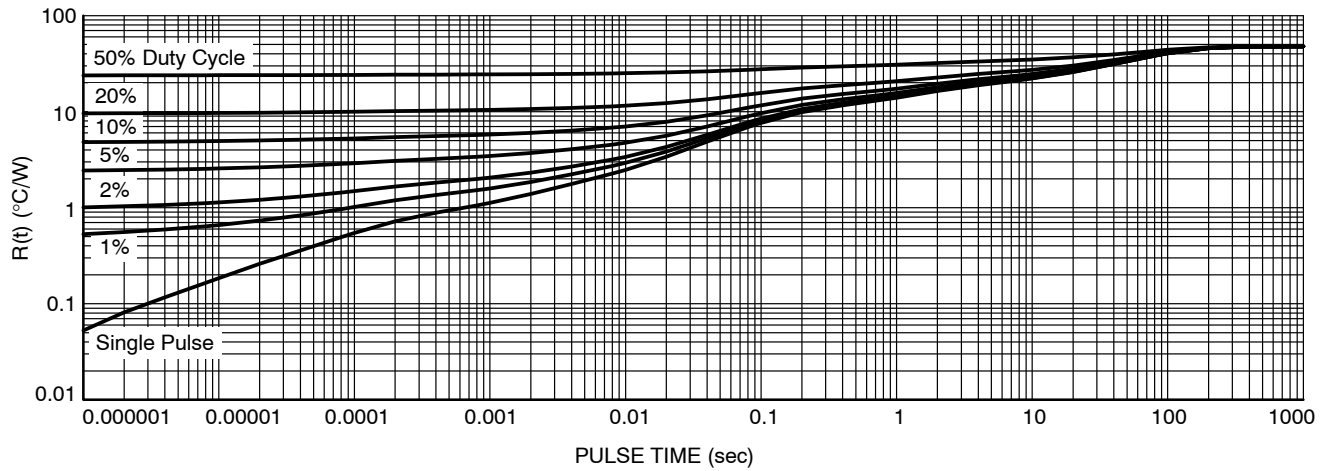


Figure 13. Thermal Response

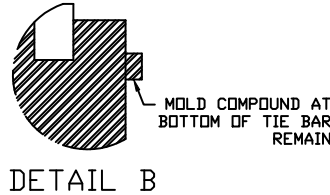
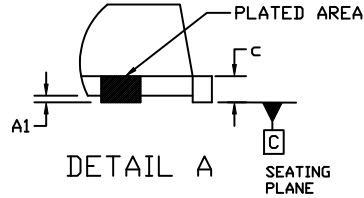
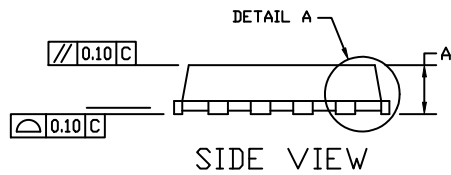
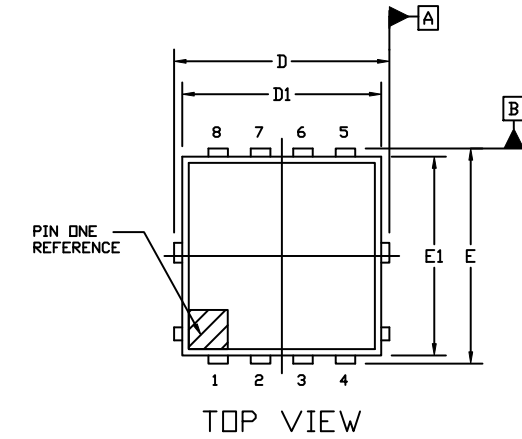
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVTFS027N10MCLTAG	27L1	WDFN8 (Pb-Free)	1500 / Tape & Reel
NVTFWS027N10MCLTAG	27W1	WDFN8 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

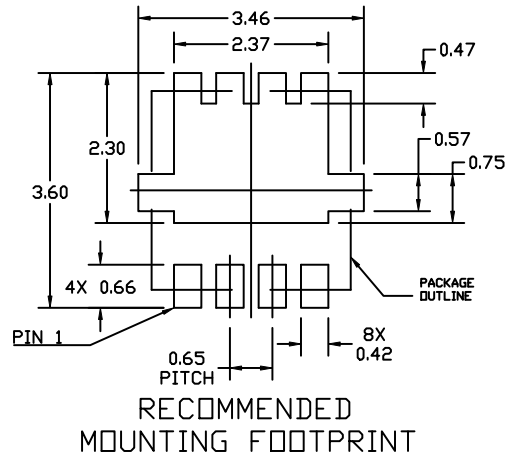
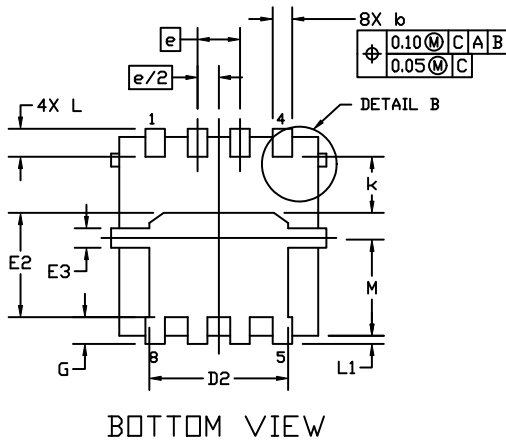
WDFNW8 3.3x3.3, 0.65P (Full-Cut μ 8FL WF)
CASE 515AN
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60



- * For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

