

# MOSFET - Power, Single N-Channel, T10, STD Gate, SO8FL

80 V, 13.8 mΩ, 35 A

## NVMFWS014N08X

### Features

- Low  $Q_{RR}$ , Soft Recovery Body Diode
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Motor Drives
- Automotive 48 V System

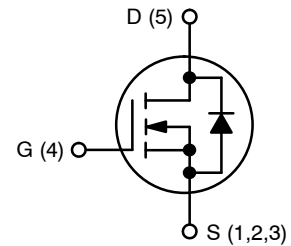
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	80	V
Gate-to-Source Voltage	DC $V_{GS}$	$\pm 20$	V
Continuous Drain Current (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	35 A
		$T_C = 100^\circ\text{C}$	25
Power Dissipation (Note 1)	$T_C = 25^\circ\text{C}$ $P_D$	35	W
Pulsed Drain Current	$T_C = 25^\circ\text{C}$ , $t_p = 100 \mu\text{s}$ $I_{DM}$	126	A
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	60	A
Single Pulse Avalanche Energy (Note 3) ( $I_{PK} = 20 \text{ A}$ )	$E_{AS}$	20	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

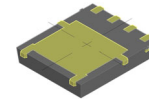
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using a 1 in<sup>2</sup>, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3.  $E_{AS}$  is based on started  $T_J = 25^\circ\text{C}$ , rated  $I_{AS}$ ,  $V_{DD} = 64 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ , 100% avalanche tested.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	13.8 mΩ @ $V_{GS} = 10 \text{ V}$	35 A

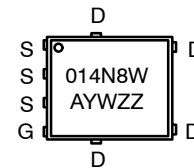


N-CHANNEL MOSFET



DFNW5 (SO-8FL)  
CASE 507BA

### MARKING DIAGRAM



014N8W = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

# NVMFWS014N08X

## THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4.3	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	38	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$ . Referenced to $25^\circ\text{C}$		32		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80\text{ V}, T_J = 25^\circ\text{C}$			1.0	$\mu\text{A}$
		$V_{DS} = 80\text{ V}, T_J = 125^\circ\text{C}$			250	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

### ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}, T_J = 25^\circ\text{C}$		12	13.8	m $\Omega$
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 32\text{ }\mu\text{A}, T_J = 25^\circ\text{C}$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 32\text{ }\mu\text{A}$		-7.5		mV/°C
Forward Transconductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 6\text{ A}$		20		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$		565		pF
Output Capacitance	$C_{OSS}$			165		
Reverse Transfer Capacitance	$C_{RSS}$			2.5		
Output Charge	$Q_{OSS}$			12		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DD} = 40\text{ V}; I_D = 6\text{ A}$		7.9		
Threshold Gate Charge	$Q_{G(TH)}$			1.7		
Gate-to-Source Charge	$Q_{GS}$			2.6		
Gate-to-Drain Charge	$Q_{GD}$			1.2		
Gate Plateau Voltage	$V_{GP}$			4.7		V
Gate Resistance	$R_G$	$f = 1\text{ MHz}$		1.5		$\Omega$

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 64\text{ V},$ $I_D = 6\text{ A}, R_G = 2.5\text{ }\Omega$		11		ns
Rise Time	$t_r$			3.6		
Turn-Off Delay Time	$t_{d(OFF)}$			16		
Fall Time	$t_f$			3.3		

### SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 6\text{ A}, T_J = 25^\circ\text{C}$		0.81	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 6\text{ A}, T_J = 125^\circ\text{C}$		0.65		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI/dt = 1000\text{ A}/\mu\text{s},$ $I_S = 6\text{ A}, V_{DD} = 64\text{ V}, T_J = 25^\circ\text{C}$		17		ns
Charge Time	$t_a$			8		
Discharge Time	$t_b$			9		
Reverse Recovery Charge	$Q_{RR}$			70		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

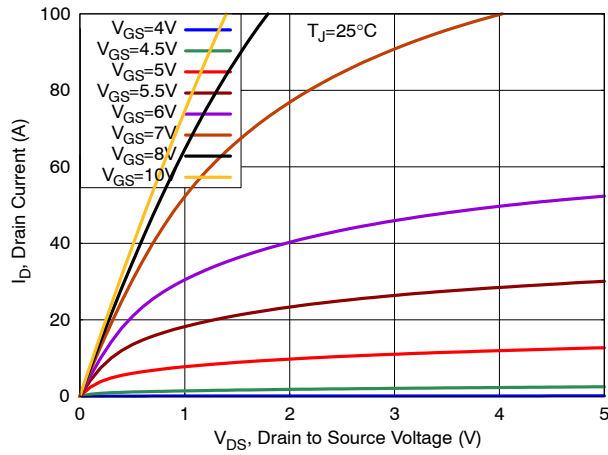


Figure 1. On-Region Characteristics

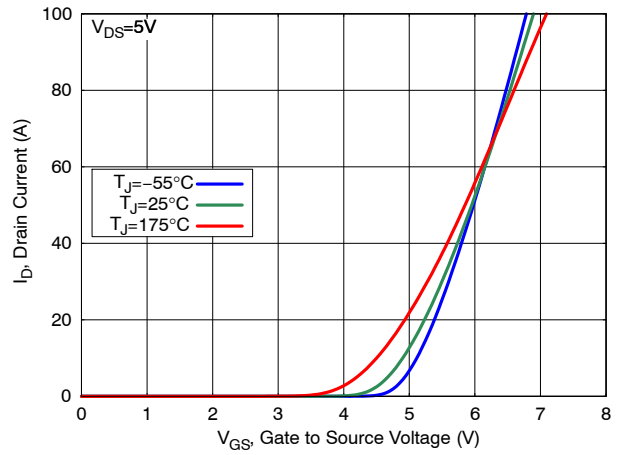


Figure 2. Transfer Characteristics

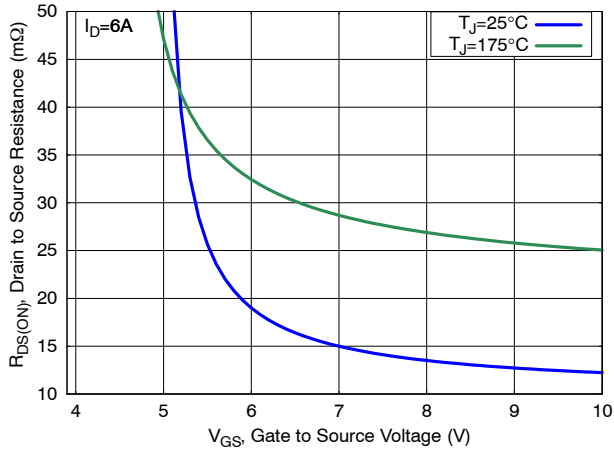


Figure 3. On-Resistance vs. Gate Voltage

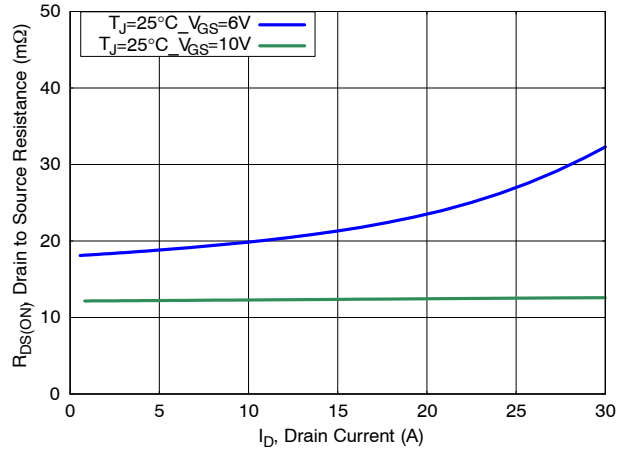


Figure 4. On-Resistance vs. Drain Current

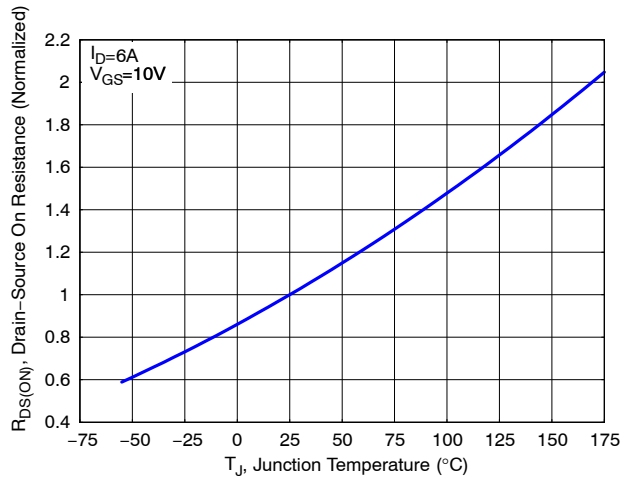


Figure 5. Normalized ON Resistance vs. Junction Temperature

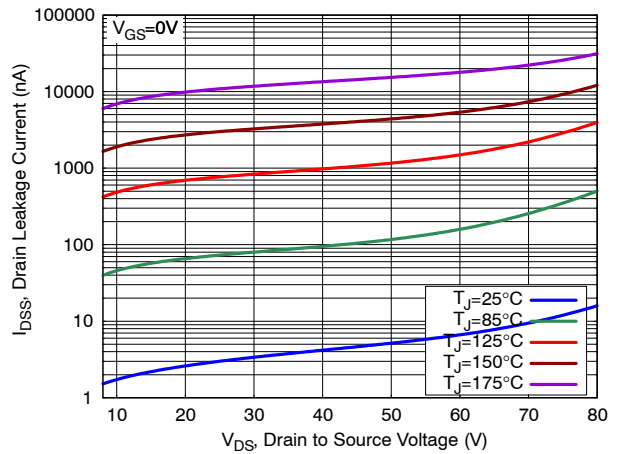


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

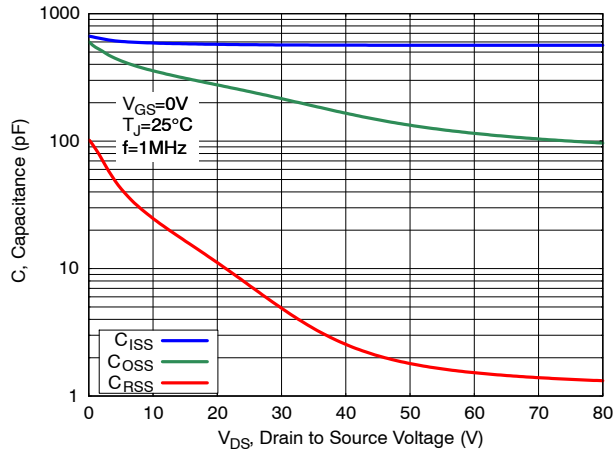


Figure 7. Capacitance Characteristics

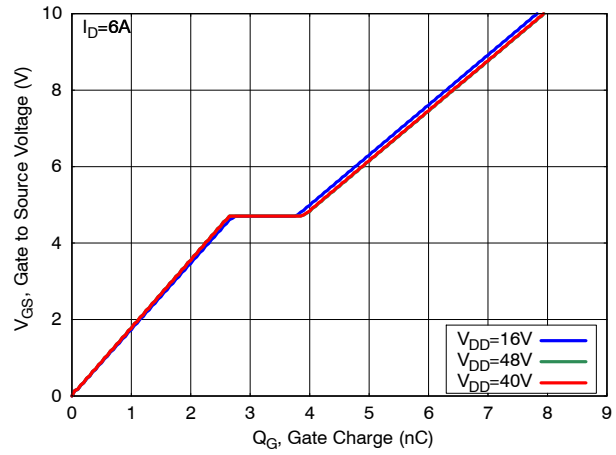


Figure 8. Gate Charge Characteristics

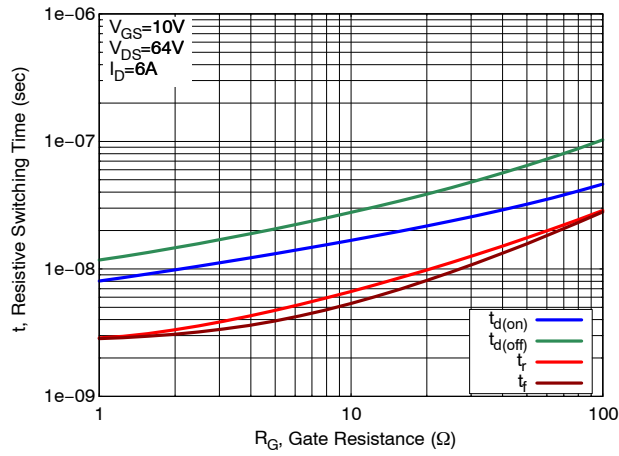


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

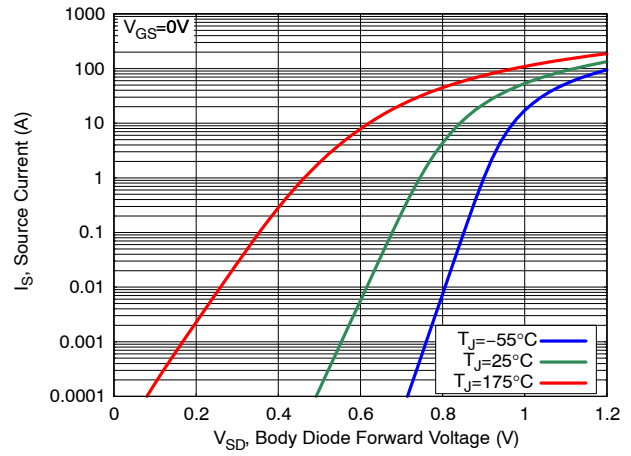


Figure 10. Diode Forward Characteristics

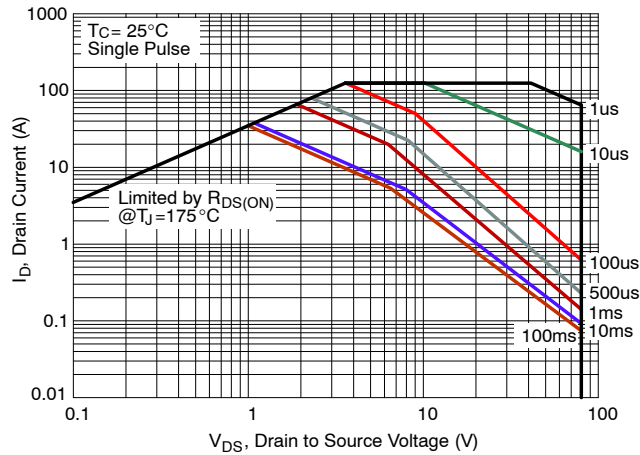


Figure 11. Safe Operating Area (SOA)

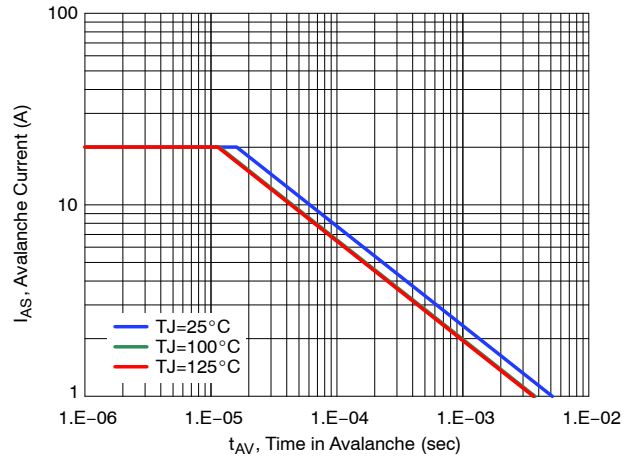


Figure 12. Avalanche Current vs. Pulse Time (UIS)

# NVMFWS014N08X

## TYPICAL CHARACTERISTICS

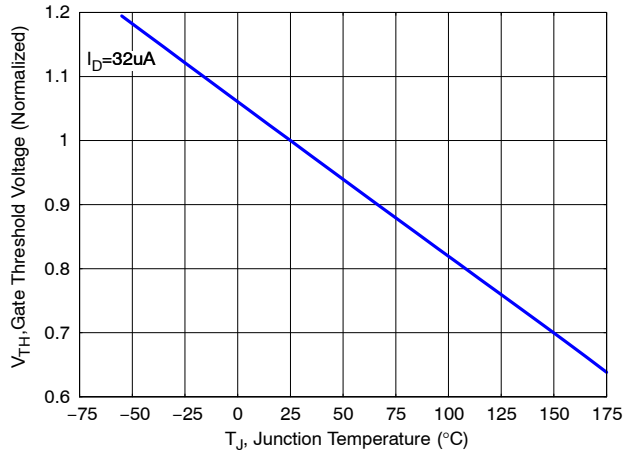


Figure 13. Gate Threshold Voltage vs. Junction Temperature

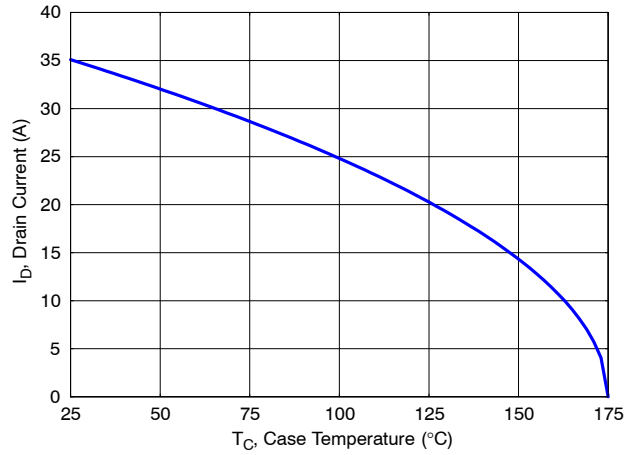


Figure 14. Maximum Current vs. Case Temperature

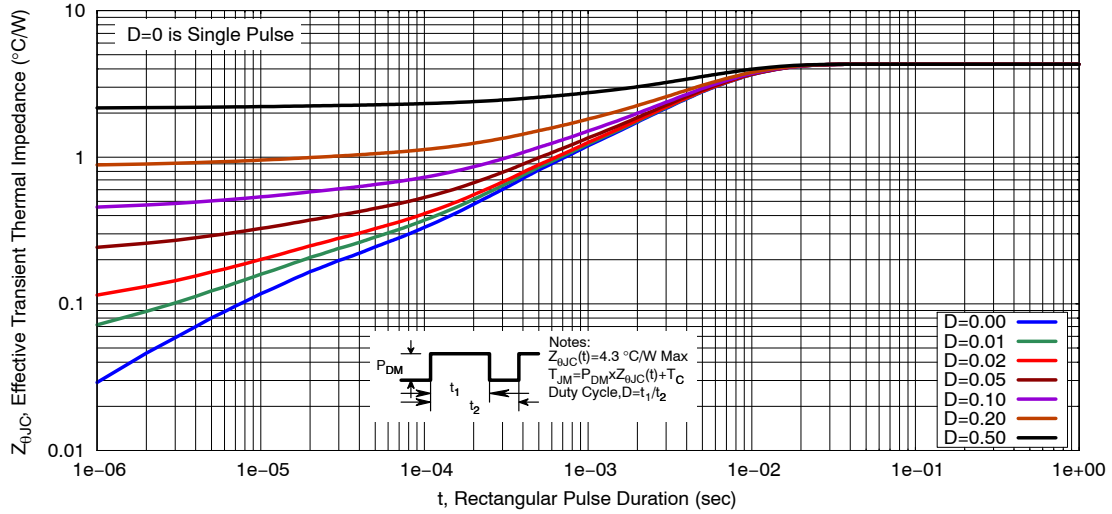


Figure 15. Transient Thermal Response

## DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFWS014N08XT1G	014N8W	DFNW5 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## REVISION HISTORY

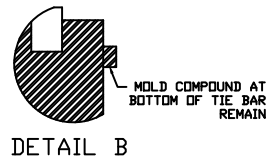
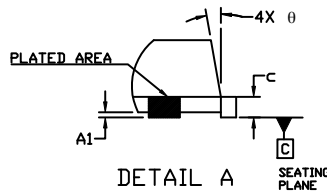
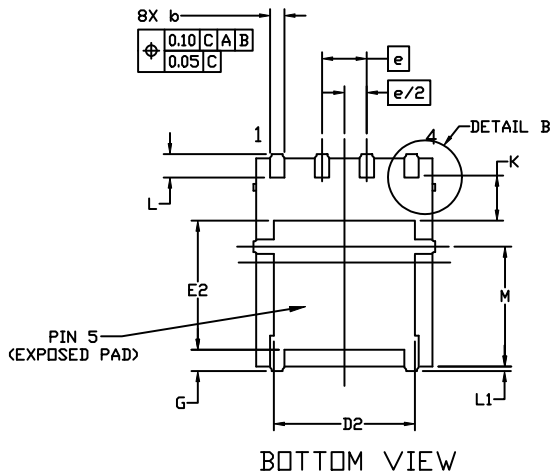
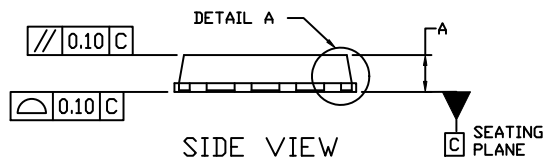
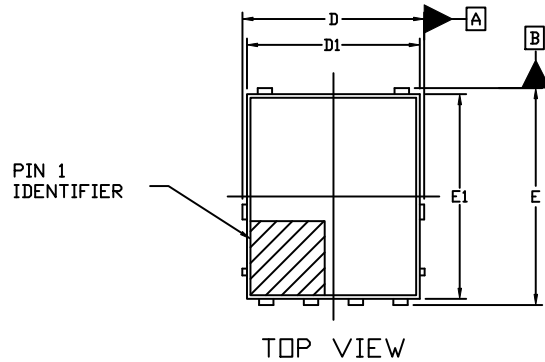
Revision	Description of Changes	Date
0	Complete redo from all new provided FIT source files	6/13/2025

PACKAGE DIMENSIONS

DFNW5 5x6 (FULL-CUT SO8FL WF)

CASE 507BA

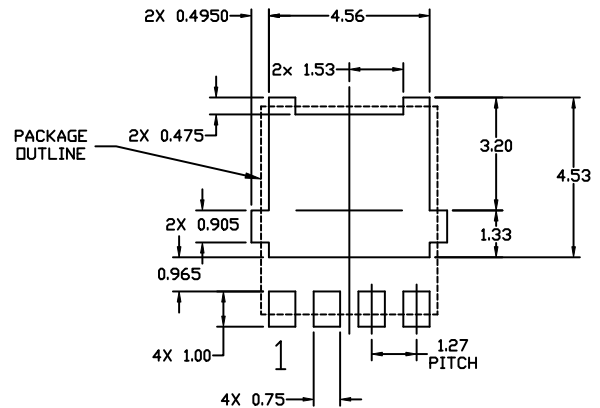
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



RECOMMENDED  
MOUNTING FOOTPRINT

- \* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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