

# MOSFET – Power, Single N-Channel

100 V, 3.9 mΩ, 138 A

NVMFWS004N10MC

## Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free, Beryllium Free and are RoHS Compliant

## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	100	V
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>θJC</sub> (Note 1)	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub>	138	A
		T <sub>C</sub> = 100°C		98	
Power Dissipation R <sub>θJC</sub> (Note 1)	Steady State	T <sub>C</sub> = 25°C	P <sub>D</sub>	164	W
		T <sub>C</sub> = 100°C		82	
Continuous Drain Current R <sub>θJA</sub> (Notes 1, 2)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	21	A
		T <sub>A</sub> = 100°C		15	
Power Dissipation R <sub>θJA</sub> (Notes 1, 2)	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub>	3.8	W
		T <sub>A</sub> = 100°C		1.9	
Pulsed Drain Current	T <sub>A</sub> = 25°C, t <sub>p</sub> = 10 μs		I <sub>DM</sub>	900	A
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	–55 to +175	°C
Source Current (Body Diode)			I <sub>S</sub>	126	A
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = 9.2 A)			E <sub>AS</sub>	536	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

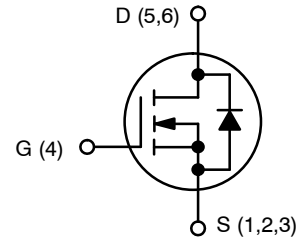
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL RESISTANCE RATINGS

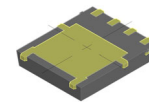
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 1)	$R_{\theta JC}$	0.91	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using 1 in<sup>2</sup> pad size, 2 oz. Cu pad.

$V_{(BR)DS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	3.9 mΩ @ 10 V	138 A

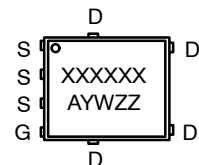


N-CHANNEL MOSFET



DFN5  
(SO8FL WF)  
CASE 507BA

## MARKING DIAGRAM



- A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

## ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

# NVMFWS004N10MC

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\text{ }\mu\text{A}$ , ref to $25^\circ\text{C}$		56		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}$	$T_J = 25^\circ\text{C}$		1	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

### ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 270\text{ }\mu\text{A}$	2		4	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 250\text{ }\mu\text{A}$ , ref to $25^\circ\text{C}$		-9.1		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 48\text{ A}$		3.3	3.9	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 10\text{ V}, I_D = 48\text{ A}$		120		S

### CHARGES & CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$		3600		pF
Output Capacitance	$C_{OSS}$			1700		
Reverse Transfer Capacitance	$C_{RSS}$			30		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 48\text{ A}$		48		nC
Threshold Gate Charge	$Q_{G(TH)}$			11		
Gate-to-Source Charge	$Q_{GS}$			18		
Gate-to-Drain Charge	$Q_{GD}$			8		
Plateau Voltage	$V_{GP}$			5.2		V

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 48\text{ A}, R_G = 6\text{ }\Omega$		25		ns
Rise Time	$t_r$			18		
Turn-Off Delay Time	$t_{d(OFF)}$			39		
Fall Time	$t_f$			13		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 48\text{ A}$	$T_J = 25^\circ\text{C}$		0.84	1.3	V
			$T_J = 125^\circ\text{C}$		0.73		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di/dt = 100\text{ A}/\mu\text{s}, I_S = 24\text{ A}$		65			ns
Reverse Recovery Charge	$Q_{RR}$			73			nC
Charge Time	$t_S$			30			ns
Discharge Time	$t_D$			35			ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

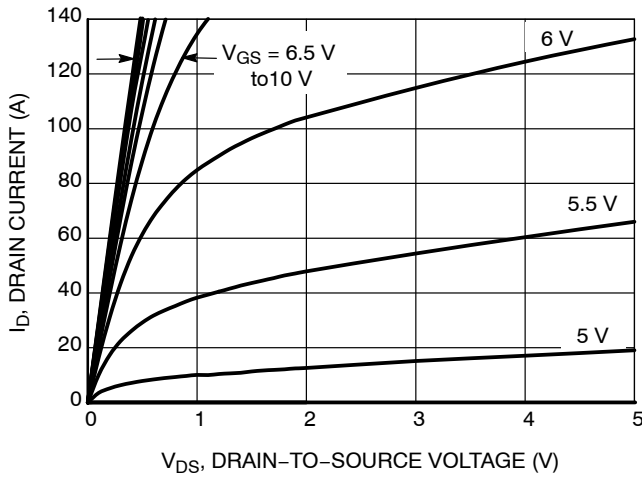


Figure 1. On-Region Characteristics

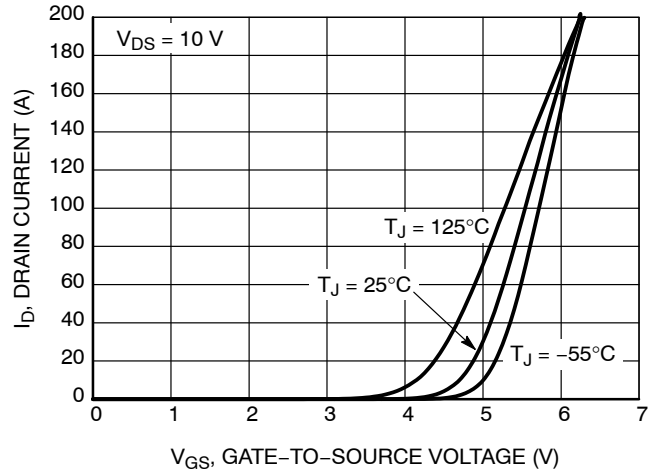


Figure 2. Transfer Characteristics

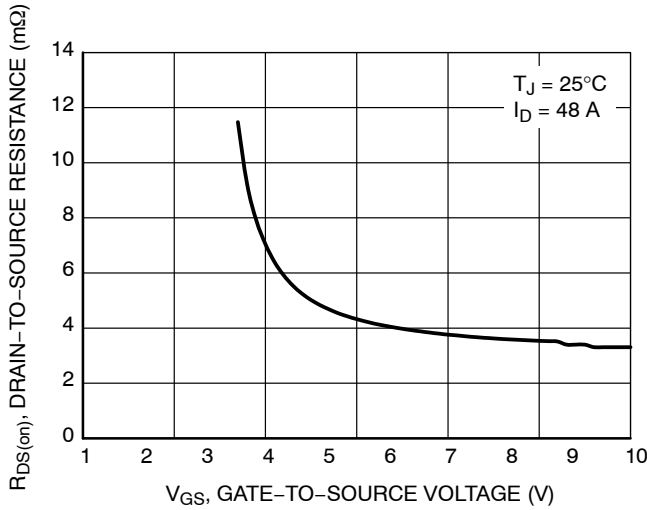


Figure 3. On-Resistance vs. Gate-to-Source Voltage

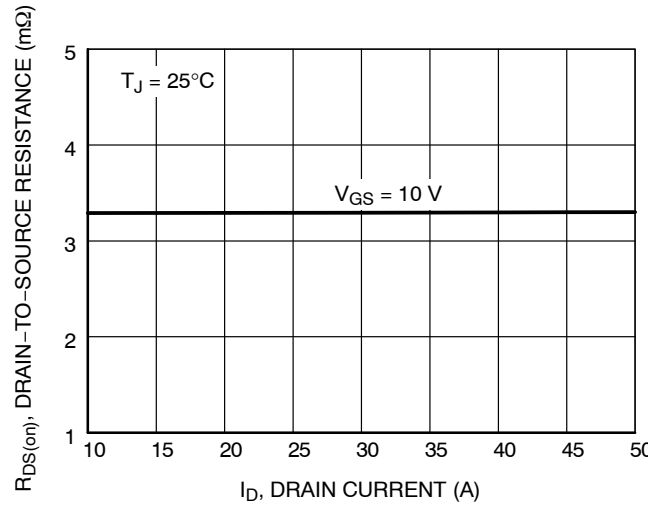


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

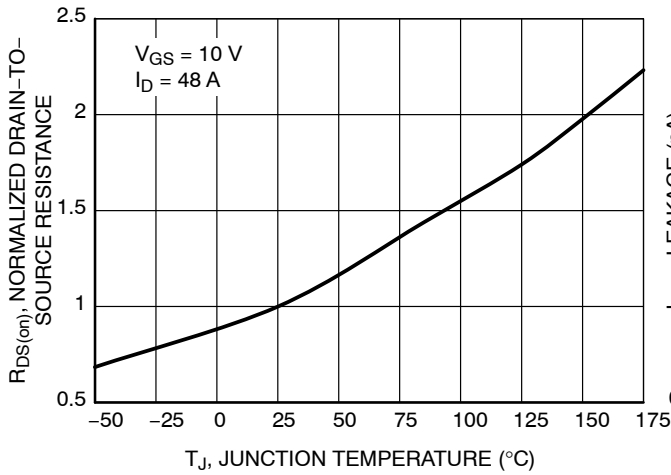


Figure 5. On-Resistance Variation with Temperature

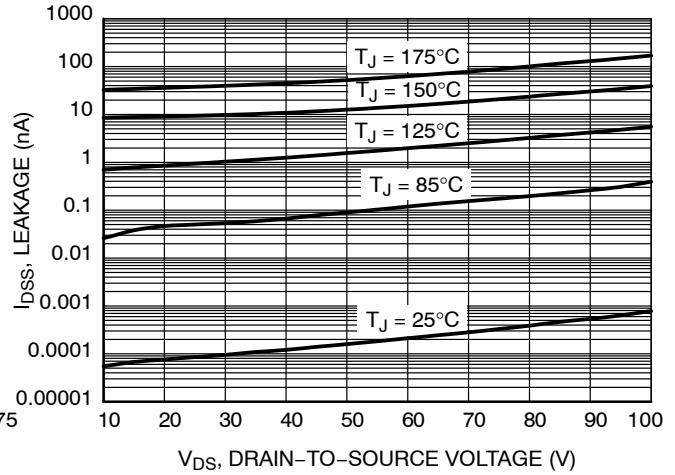


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

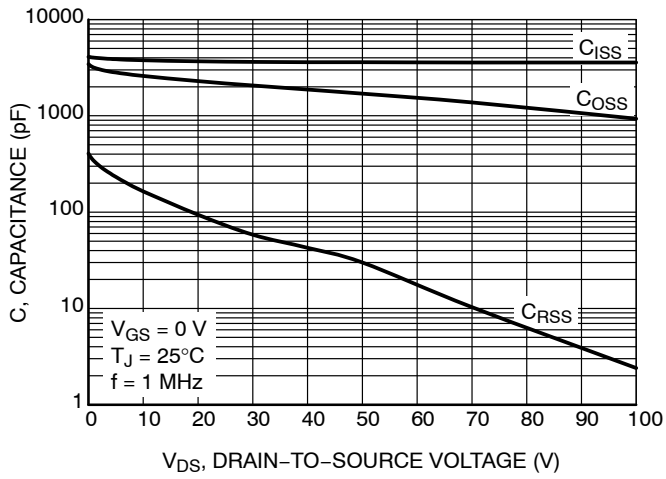


Figure 7. Capacitance Variation

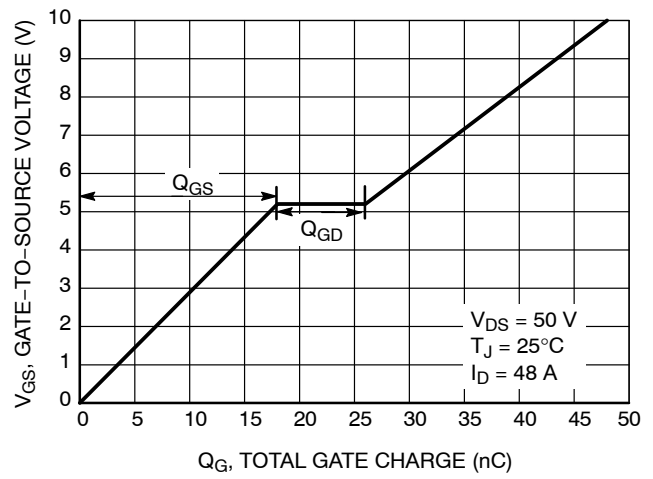


Figure 8. Gate-to-Source Voltage vs. Total Charge

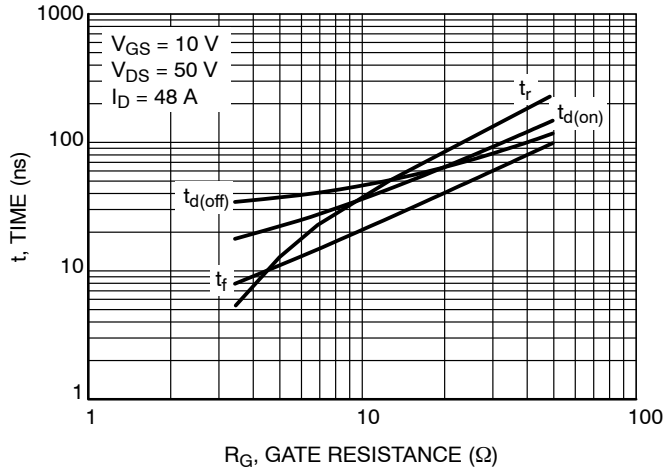


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

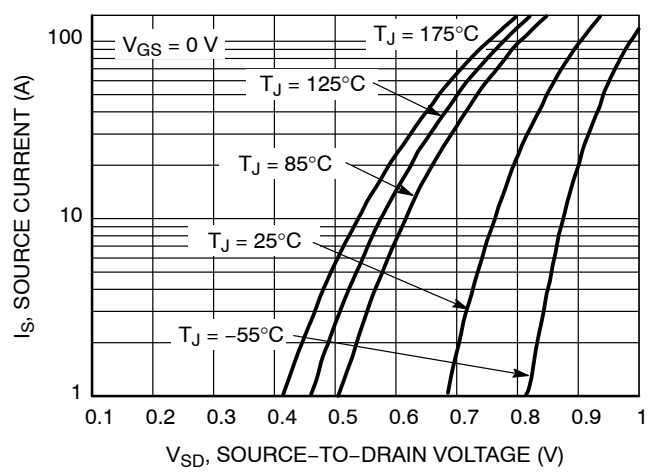


Figure 10. Diode Forward Voltage vs. Current

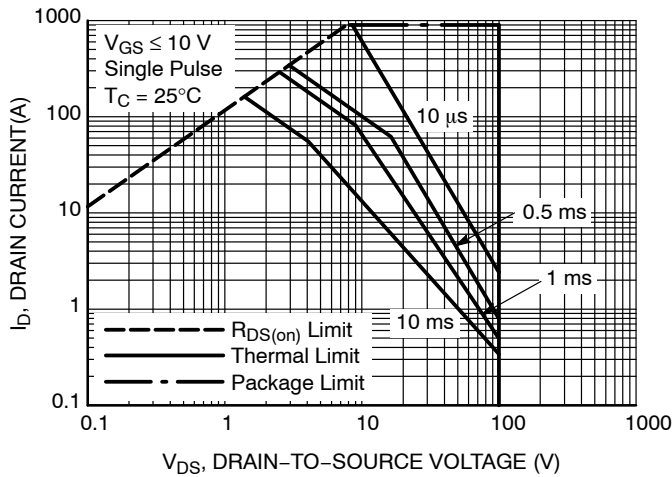


Figure 11. Maximum Rated Forward Biased Safe Operating Area

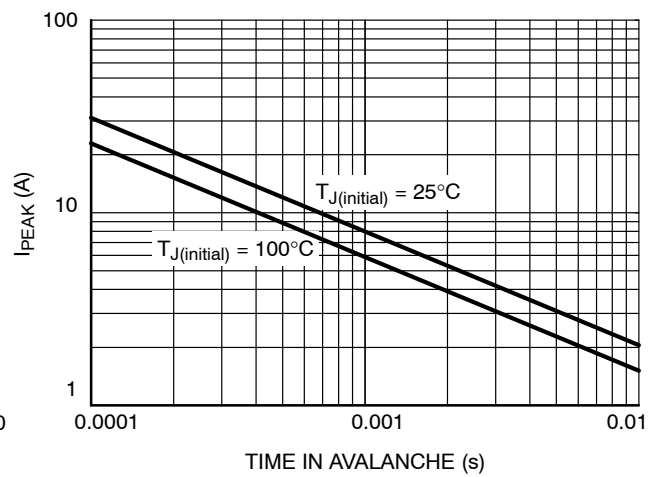


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

# NVMFWS004N10MC

## TYPICAL CHARACTERISTICS

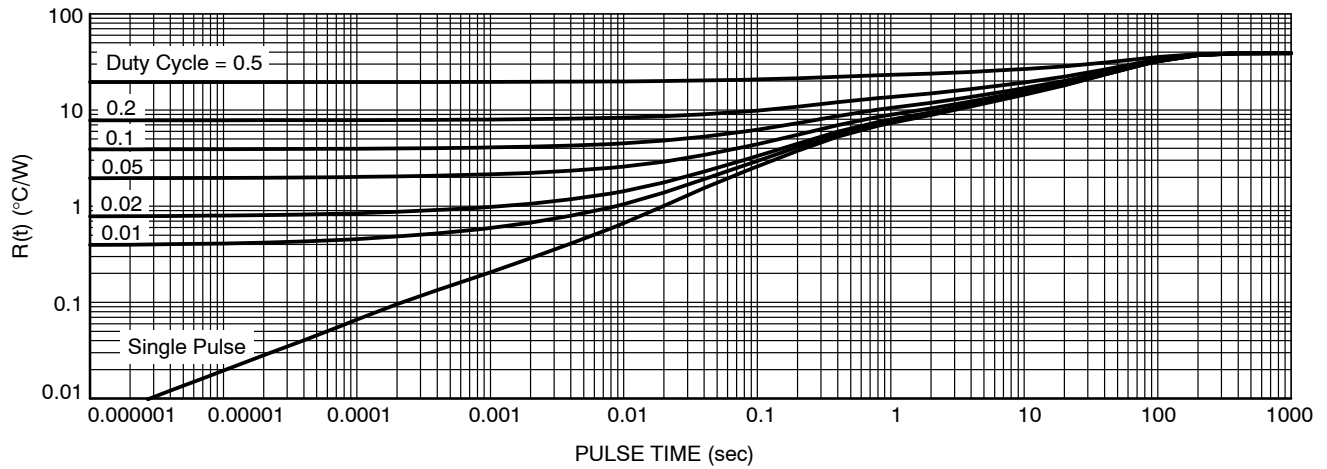


Figure 13. Thermal Characteristics

### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NVMFWS004N10MCT1G	004W10	Wettable Flank DFN5 (Pb-Free)	1500 / Tape & Reel

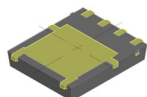
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®

ON

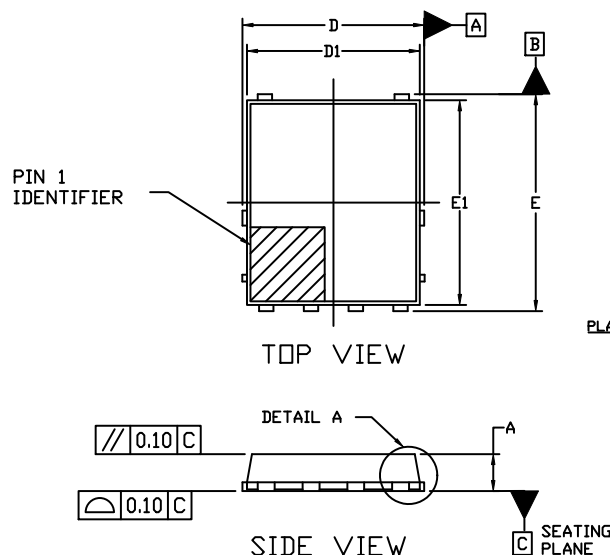


### DFNW5 5x6 (FULL-CUT SO8FL WF)

#### CASE 507BA

#### ISSUE A

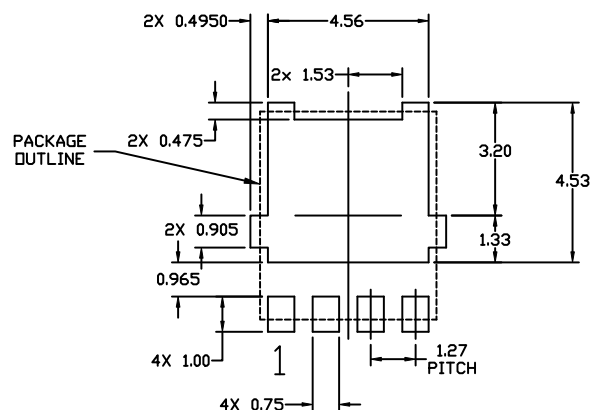
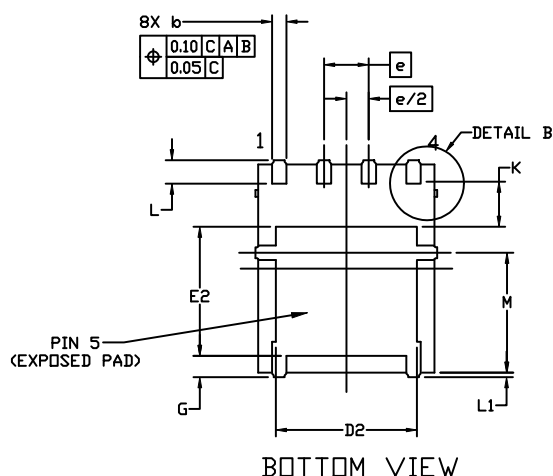
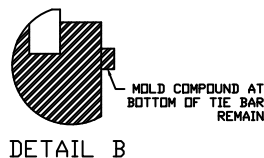
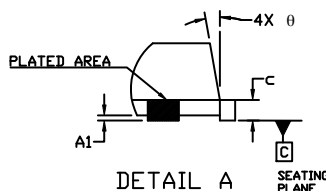
DATE 03 FEB 2021



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

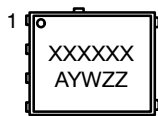
MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



### RECOMMENDED MOUNTING FOOTPRINT

- \* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 W = Work Week  
 ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DFNW5 5x6 (FULL-CUT SO8FL WF)	PAGE 1 OF 1

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