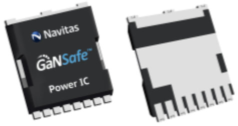
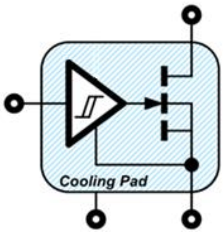
Navitas
Electrify Our World™
GaNSafe™
NV6512C
DATASHEET

GaNSafe™ Power IC

Bottom-cooled TOLL-4L
Top **Bottom**





Simplified Diagram

1. Features

- V_{DS} 650V continuous / 800V transient
- 55 mΩ $R_{DS(ON)\_\mathbf{MAX}\_25C}$ and 41 A $I_{DS(CONTINUOUS)}$
- TOLL-4L thermally-enhanced, bottom-cooled
- PWM input compatibility 10 to 18 V
- Paralleling capability up to 2x power ICs
- Zero reverse-recovery charge
- Turn-ON and Turn-OFF dV/dt programmability
- Up to 2 MHz operation
- Short Circuit Protection with 350 ns latency
- dV/dt immunity up to 100 V/ns
- 2kV ESD all Pins
- JEDEC and IPC-9701 Qualifications
- AEC-Q100 Grade 1 (ordering option)
- RoHS, Pb-free, REACH-compliant

2. Applications / Topologies

- AC-DC, DC-DC, CCM or CrM TP-PFC
- Optimized for synchronous half-bridge, full-bridge, 3-phase, or buck/boost operation
- Data Center CRPS, and Solar Inverter/ESS
- EV OBC & DC-DC converter, and motor drive

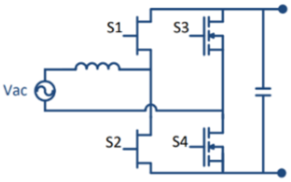
3. Description

The NV6512C is a thermally-enhanced bottom-cooled SMD version of the GaNFast™ power IC family, optimized for higher power systems using GaNSafe™ technology, making it the ideal choice for high-frequency, high-power-density, and high-efficiency power systems in data center, solar, industrial, and automotive segments.

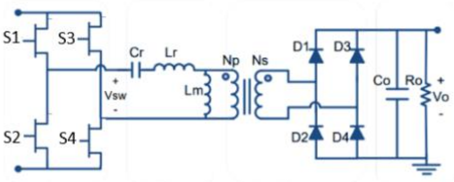
GaNFast power ICs integrate GaN FET(s) with gate drive to create an easy-to-use power stage building block.

GaNSafe technology further integrates critical protection and performance features that enable unprecedented reliability and robustness. The TOLL package ties this architecture together with industry-standard thermally-enhanced packaging, creating dependable solutions for world-class size/weight, efficiency, and cost.

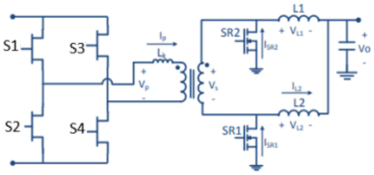
4. Typical Application Circuits



BTP PFC



CLLC or LLC



PSFB or DAB

5. Table of Contents

6. Absolute Maximum Ratings(Note 1) (with respect to Source, T_{CASE} = 25°C, unless specified)

Symbol	Parameter	Max	Units
$V_{DS(CONT)}$	Continuous Drain-to-Source voltage	-7 to +650	V
$V_{DS(TRAN)}$	Transient Drain-to-Source voltage (Note 2)	800	V
$I_{DS(CONT)}$	Continuous Drain current (T_{CASE} = 25 °C) (Note 3) Continuous Drain current (T_{CASE} = 100 °C, T_{JUNC} = 150 °C) (Note 3)	41 26	A
I_{DS_PULSE}	Pulsed Drain current (10 µs @ T_{JUNC} = 25 °C) (Note 3) Pulsed Drain current (10 µs @ T_{JUNC} = 150 °C) (Note 3)	83 38	A
V_{DRIVE_CONT}	Continuous input voltage measured between V_{DRIVE} and SK pins	-0.6 to 18	V
V_{DRIVE_TRANS}	Transient input voltage measured between V_{DRIVE} and SK pins (Note 4)	-2.0	V
dV/dt	Slew Rate on Drain-to-Source	100	V/ns
T_{JUNC}	Junction Temperature	-40 to +150	°C
T_{STOR}	Storage temperature	-55 to +150	°C

(1) Absolute Maximum Ratings are stress ratings, and subjecting devices to stresses beyond these ratings may cause permanent damage.

(2) $V_{DS\ (TRAN)}$ allows for surge ratings during ***non-repetitive*** events that are < 100 µs.

(3) Limited by Short Circuit Protection.

(4) Limited to 200 ns.

7. Recommended Operating Conditions (Note 5)

Symbol	Parameter	Min	Typ	Max	Units
V_{DRIVE_H}	Drive input pin voltage high	11	12 ~ 13	18	V
V_{DRIVE_L}	Drive input pin voltage low	-0.3	0	0.3	V
R_{DRIVE_ON}	Turn-ON V_{DRIVE} Pin series resistor	5	10	25	Ω
R_{DRIVE_OFF}	Turn-OFF V_{DRIVE} Pin series resistor	1	2	10	Ω

(5) Exposure to conditions beyond maximum recommended operating conditions for extended periods of time may affect device reliability.

8. ESD Ratings

Symbol	Parameter	Max	Units
HBM	Human Body Model (per JS-001-2014)	2,000	V
CDM	Charged Device Model (per JS-002-2014)	1,000	V

9. Thermal Resistance

Symbol	Parameter	Typ	Units
$R_{\theta\_JUNC\text{-}CASE}$	Junction-to-Case Thermal Resistance	0.60	°C/W

10. Electrical Characteristics

Conditions unless otherwise specified: V_{DS} = 400V, V_{DRIVE} = 15V, T_{CASE} = 25°C, I_{DS} = 13A, R_{DRIVE} = 5Ω

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Drive Pin Characteristics						
$I_{DRIVE\_OPERATING}$	V_{DRIVE} operating current		3.3		mA	V_{DRIVE} = 15V, F_{SW} = 300kHz, 50% D.C., V_{DS} = 0V
$I_{DRIVE\_LEAKAGE}$	V_{DRIVE} leakage current		1.5		mA	V_{DRIVE} = 15V
Switching Characteristics						
t_{ON}	Turn-ON propagation delay	24		35	ns	Fig 1,2 ; -40 °C $\le T_{CASE} \le$ +150 °C ; R_{DRIVE} = 1Ω
t_{OFF}	Turn-OFF propagation delay	7		13	ns	Fig 1,2 ; -40 °C $\le T_{CASE} \le$ +150 °C ; R_{DRIVE} = 1Ω
t_{ON_MIN}	Minimum valid V_{DRIVE} on-time pulse duration (first PWM ON pulse)	75			ns	R_{DRIVE} = 5Ω
t_{RISE}	Turn-OFF rise time		8		ns	Fig 1,2 ; R_{DRIVE} = 1Ω
t_{FALL}	Turn-ON fall time		7		ns	Fig 1,2 ; R_{DRIVE} = 10Ω
Short Circuit Protection (SCP)						
V_{DS_SCP}	$V_{DS(ON)}$ Short Circuit Detect Threshold	11.5	13.5		V	18V $\ge V_{DRIVE} \ge$ 11V, T_{JUNC} = -40 °C to +150 °C, verified by design
$t_{SCP\_DLY\_TURN\text{-}ON}$	Delay from Short Circuit Event to Soft Shut Down, into Turn-ON		350		ns	18V $\ge V_{DRIVE} \ge$ 11V, T_{JUNC} = -40 °C to +150 °C, verified by design
$t_{SCP\_DLY\_OPER}$	Delay from Short Circuit Event to Soft Shut Down, during Operation		50		ns	18V $\ge V_{DRIVE} \ge$ 11V, T_{JUNC} = -40 °C to +150 °C, verified by design
GaN FET Characteristics						
I_{DSS}	Drain-Source leakage current		2.0	100	µA	V_{DS} = 650 V, V_{DRIVE} = 0 V
I_{DSS}	Drain-Source leakage current		21		µA	V_{DS} = 650 V, V_{DRIVE} = 0 V, T_{JUNC} = 150 °C
$R_{DS(ON)}$	Drain-Source resistance		40	55	mΩ	V_{DRIVE} = 15V, I_{DS} = 13 A
$R_{DS(ON)}$	Drain-Source resistance		94		mΩ	V_{DRIVE} = 15V, I_{DS} = 13 A, T_{JUNC} = 150 °C
V_{SD}	Source-Drain reverse voltage		3.3		V	V_{DRIVE} = 0 V, I_{SD} = 13 A
I_{SD}	Source-Drain reverse current		66		A	V_{DRIVE} = 0V, V_{SD} = 7V, 50us pulse, based on $P_{DISSIPATION}$
Q_{OSS}	Output charge		59		nC	V_{DS} = 400 V, V_{DRIVE} = 0 V
Q_{RR}	Reverse recovery charge		Zero		nC	
C_{OSS}	Output capacitance		74		pF	V_{DS} = 400 V, V_{DRIVE} = 0 V
$C_{O(er)}$ (Note 6)	Effective output capacitance, energy related		99		pF	V_{DS} = 400 V, V_{DRIVE} = 0 V
$C_{O(tr)}$ (Note 7)	Effective output capacitance, time related		148		pF	V_{DS} = 400 V, V_{DRIVE} = 0 V
E_{ON}	Switching energy, Turn-ON		67		µJ	V_{DS} = 400 V, I_{DS} = 13 A, R_{DRIVE} = 10Ω
E_{OFF}	Switching energy, Turn-OFF		0.5		µJ	V_{DS} = 0 to 400 V, I_{DS} = 13 A, R_{DRIVE} = 2Ω

(6) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(7) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

11. Inductive Switching Test Circuit and Typical Waveforms

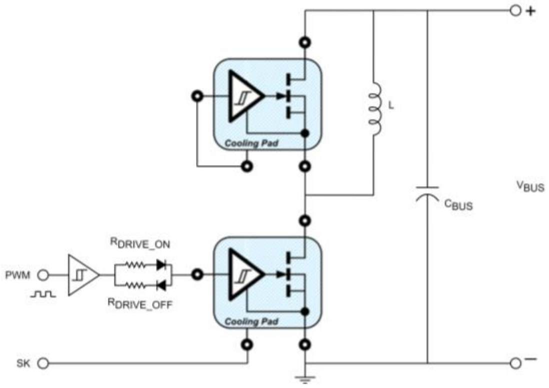


Figure 1. Inductive Switching Test Circuit

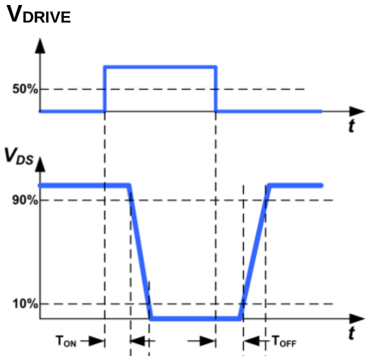


Figure 2. Prop Delay, Rise/Fall Time

12. Electrical Curves (GaN FET, T_{CASE} = 25 °C unless otherwise specified)

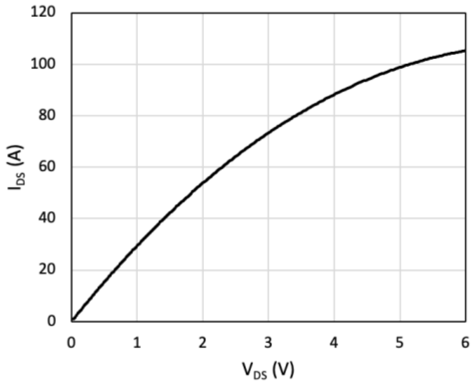


Fig. 3. I_{DS} vs. V_{DS}, T_{JUNC} = 25 °C

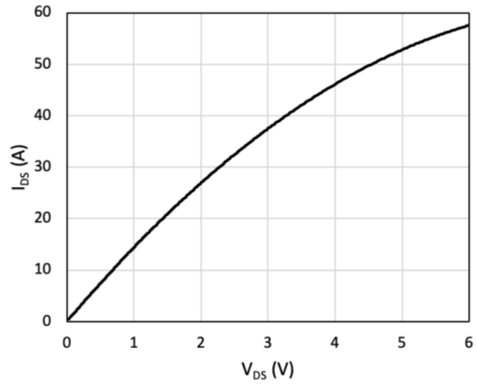


Fig. 4. I_{DS} vs. V_{DS}, T_{JUNC} = 150 °C

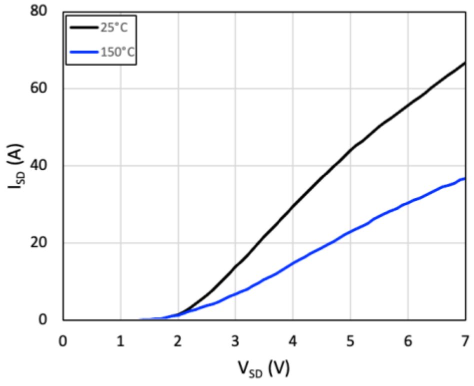


Fig. 5. I_{SD} vs. V_{SD}, T_{JUNC} = 25 °C, 150 °C

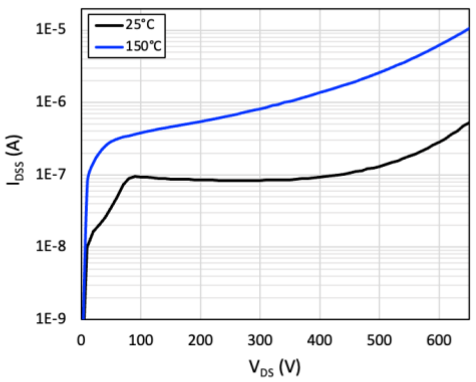


Fig. 6. I_{DSS} vs. V_{DS}, T_{JUNC} = 25 °C, 150 °C

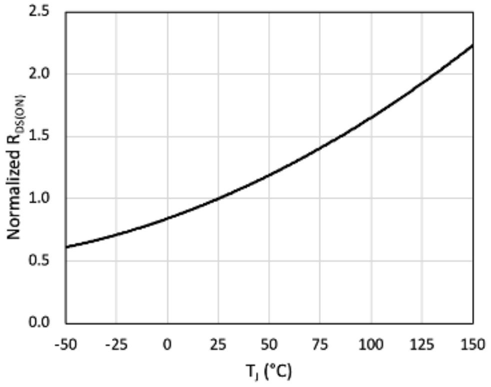


Fig. 7. Normalized R_{DSON} vs. T_{JUNC}

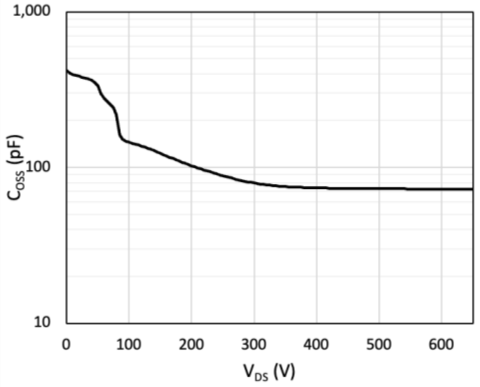


Fig. 8. C_{OSS} vs. V_{DS}

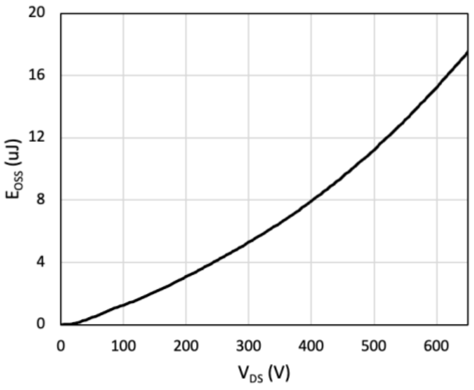


Fig. 9. E_{OSS} vs. V_{DS}

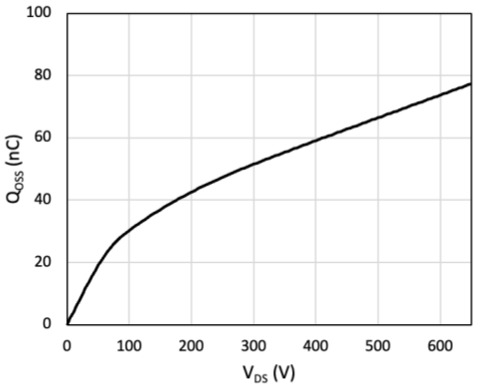


Fig. 10. Q_{OSS} vs. V_{DS}

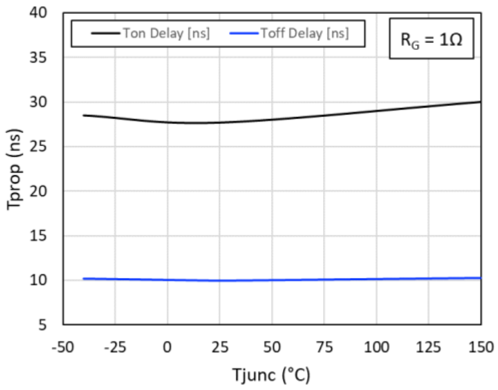


Fig. 11. Typ $t_{PROP\_ON,\ OFF}$ vs. T_{JUNC}

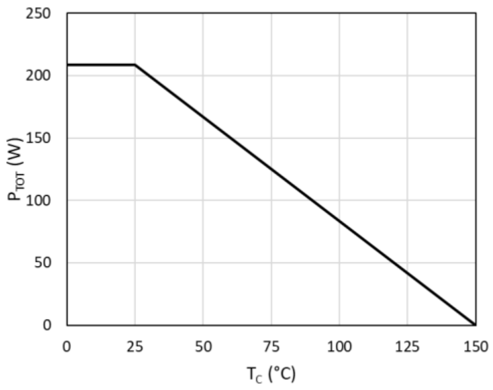


Fig. 12. $P_{DISSIPATION}$ vs. T_{CASE}

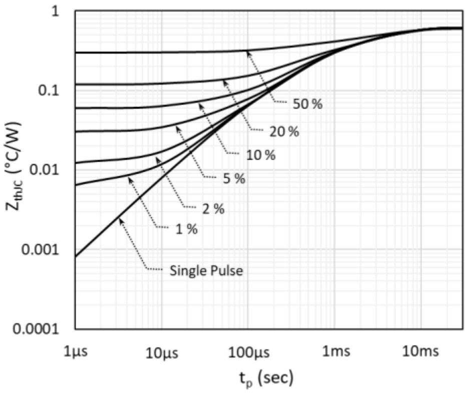


Fig. 13. Transient $R_{\Theta\_JUNC\text{-}CASE}$

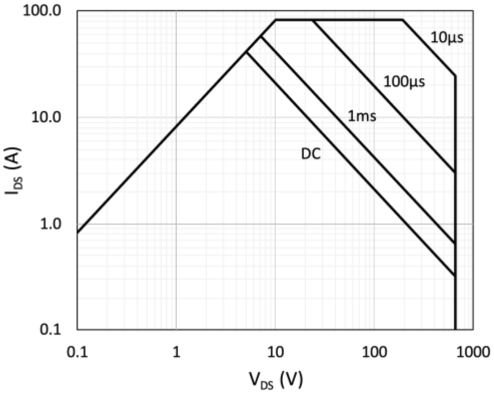


Fig. 14. Safe Operating Area, T_{CASE} = 25°C

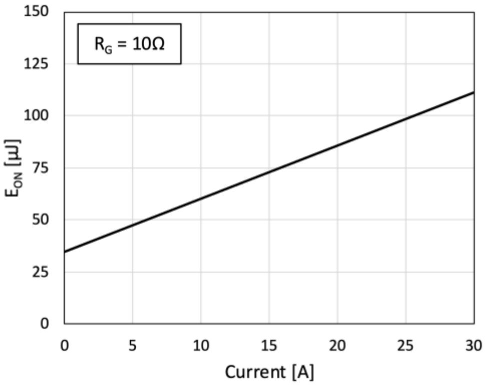


Fig. 15. E_{ON} vs. I_{DS}, T_{JUNC} = 25 °C

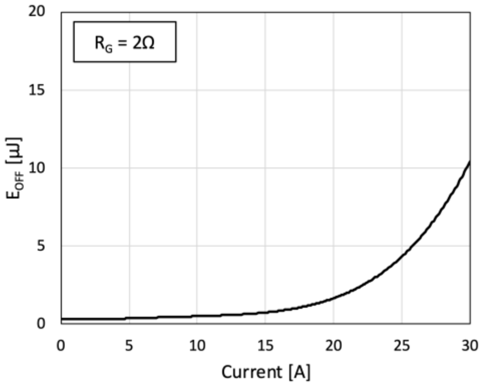


Fig. 16. E_{OFF} vs. I_{DS}, T_{JUNC} = 25 °C

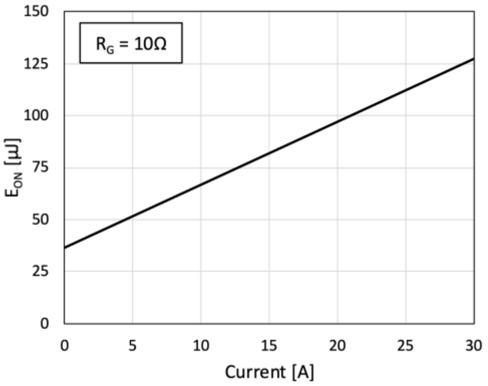


Fig. 17. E_{ON} vs. I_{DS}, T_{JUNC} = 125°C

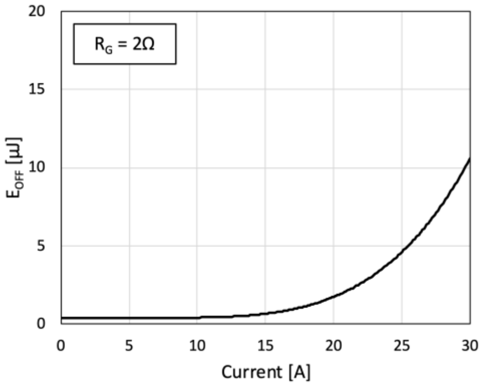


Fig. 18. E_{OFF} vs. I_{DS}, T_{JUNC} = 125°C

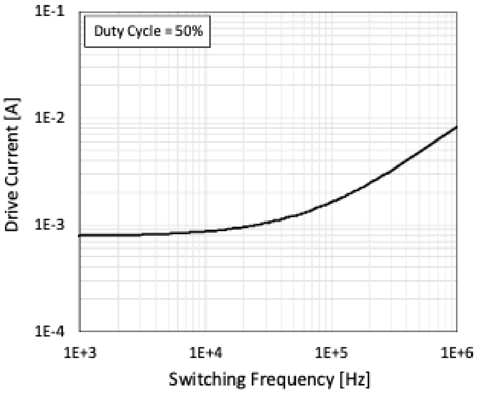
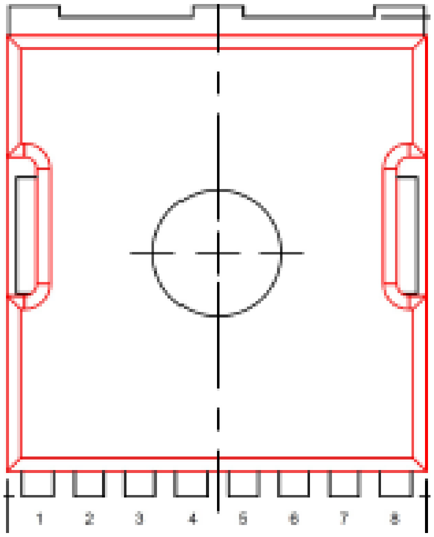


Fig. 19. I_{DRIVE} vs. Switching Frequency (F_{SW})

13. Pinout Table

Pin9 Drain Tab



Pin		I/O (Note 8)	Description
Number	**Symbol**		
1~6, Bottom Pad	Source	G	Source of power FET and Thermal Pad for Heatsink
7	SK	G	Reference for isolated PWM output (Kelvin return for V_{DRIVE})
8	V_{DRIVE}	I	Connect isolated PWM output to V_{DRIVE}
9 (Tab)	Drain	P	Drain of power FET

(8) G = Ground, I = Input, P = Power

14. Functional Description

14.1. GaNSafe Operation: Internally-regulated V_{GS} and Block Diagram

GaNSafe power IC's are the industry's first GaN power devices allowing high speed operation in an industry-standard 4-Pin package (Drain / Source / V_{DRIVE} / SK) ~ ***also providing regulated V_{GS} and protection & performance features!***

V_{DRIVE} Pin is a patent-pending multi-function input for BOTH isolated PWM signal AND internal bias power for the GaN power IC. GaNSafe is optimized for synchronous operation under all conditions (Start-Up and Steady-State). Achieving advanced capabilities in only 4 terminals requires an isolated PWM with ≥500mA output current and ≥10V (***absolute minimum***). Recommended V_{DRIVE} voltage should be ≥11V. Typical V_{DRIVE} voltage should be between 12V to 13V when using Bootstrap for HS device. Typical V_{DRIVE} voltage can be up to 15V when using isolated DC-DC supply for HS device.

Minimum On-Time: GaNSafe power ICs have an integrated 5V power supply fed by V_{DRIVE}, and Level Shift & Deglitch circuits. The t_{ON_MIN} (minimum valid on-time pulse at V_{DRIVE} pin) is 75ns (sect. 10).

Internally regulated V_{GS} turns-ON the GaN gate with optimized voltage and turns-OFF at 0V. Negative gate bias is NOT required since there is an internal Miller Clamp to maintain the GaN gate OFF during PWM OFF state.

V_{DS} Rating: During switching, the Drain toggles between Source voltage and V_{IN} (650V maximum). The Drain can withstand ***non-repetitive*** pulses up to 800V for <100 us [see sect. 6 for $V_{DS(TRAN)}$ rating]. The platform design must have appropriate commutation loop decoupling and adhere to voltage margin.

Isolated PWM IC: A dual PWM driver such as SI8273BBD-IS1 can be used (see Sect. 14.8 Ref Schematic), and Sect. 14.10 lists other PWM drivers that are recommended.

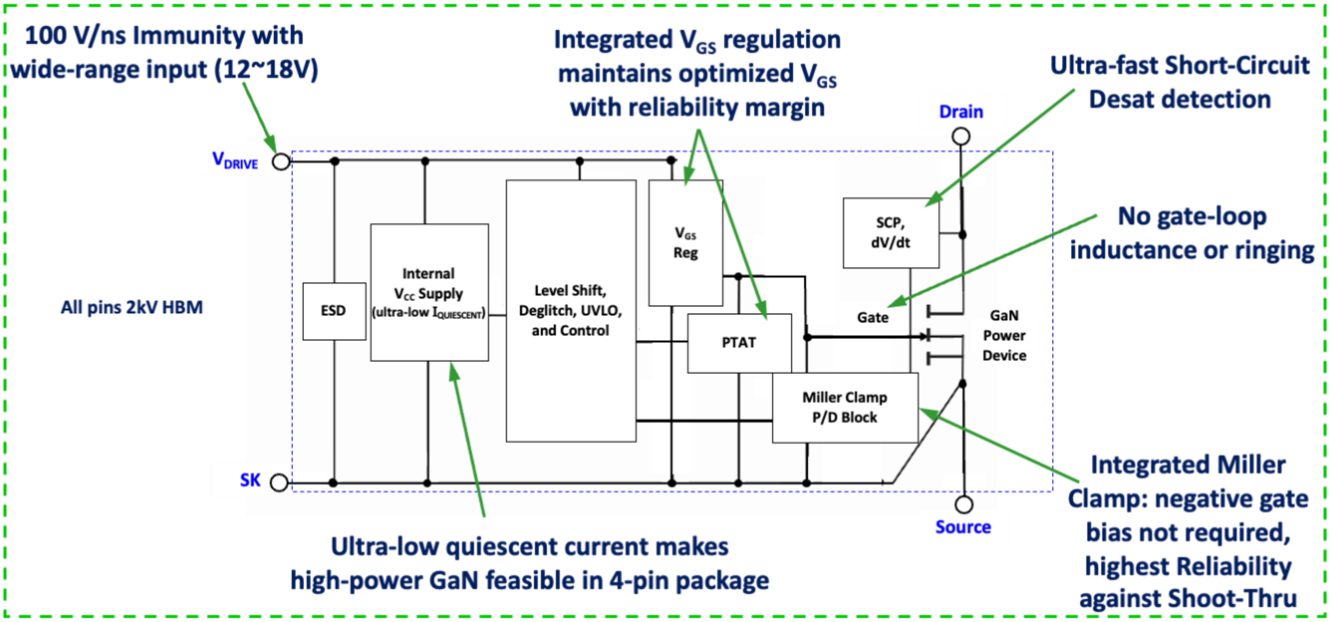


Figure 20. GaNSafe Block Diagram

14.2. Internal Gate Drive Power Loss

Internal gate drive power loss on GaNSafe power IC's can be projected by using I_{DRIVE} value from Fig. 19 (I_{DRIVE} vs. F_{SW}), interpolated between duty cycle curves, multiplied by V_{DRIVE} (i.e., I_{DRIVE} * V_{DRIVE}).

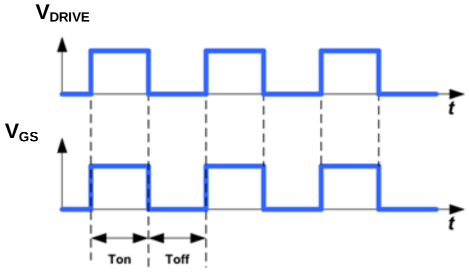
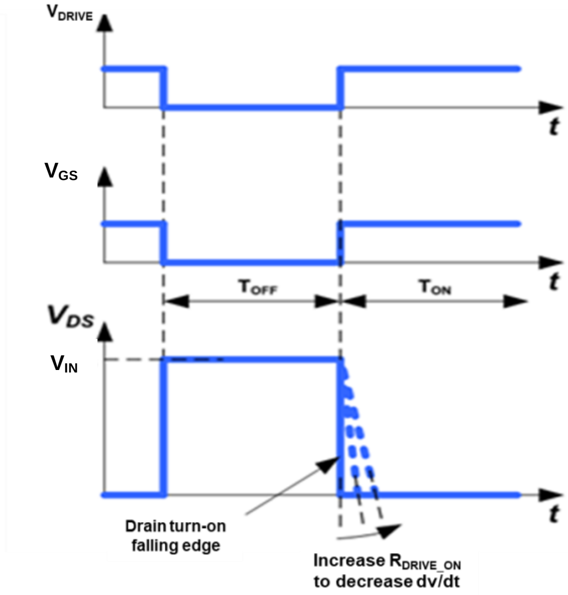


Figure 21. Normal Operating Mode Timing Diagram (V_{DRIVE} input vs. V_{GS})

14.3. Programmable Turn-ON and Turn-OFF dV/dt Control

During start-up or hard-switching condition, it may be desirable to limit slew rate (dV/dt) on the Drain. To program Turn-ON slew rate connect R_{DRIVE_ON} in series with V_{DRIVE} pin (as shown in sect. 14.8 reference schematic). Conversely, Turn-OFF slew rate is programmed using R_{DRIVE_OFF} series resistor value. These resistors ($R_{DRIVE\_ON,\ OFF}$) set the ***current*** of the internal gate drive circuit, therefore setting dV/dt.



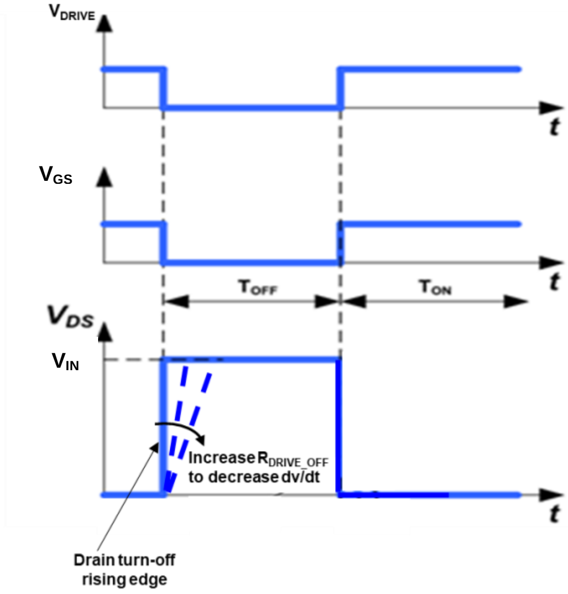


Figure 22. Turn-on dV/dt Slew Rate Control **Figure 23. Turn-OFF dV/dt Slew Rate Control**

14.4. Paralleling GaNSafe power IC's

GaNSafe power IC's can be paralleled up to a recommended maximum of **Qty2**, maintaining close T_{ON} and T_{OFF} matching of propagation delays. The following schematic revisions should be made:

- Add Kelvin-Source resistors in the return path from ***each*** SK Pin back to the external isolated PWM driver
- Adjust R_{DRIVE} value to assist T_{ON} / T_{OFF} matching

14.5. Short Circuit Protection

GaNSafe power ICs continuously monitor V_{DS} and trigger Short Circuit Protection (SCP) above V_{DS_SAT} trip point (listed in sect. 10). GaNSafe power ICs Turn-OFF via Soft Shutdown (S/D) after SCP is triggered, holding the GaN gate LOW on a cycle-by-cycle basis unless V_{DS_SAT} setpoint is CLEARED or until the system undergoes Power-ON Reset (POR).

V_{DS_SAT} Min/Max tolerances (listed in sect. 10) are designed to set SCP trip point $\geq$20% higher than the GaN power device saturation current, up to 150C. SCP latency is 350ns including Blanking Time during Turn-ON ***into*** a short circuit event, but SCP latency is 50ns when a short circuit event occurs during normal switching operation.

It is critical for GaN devices to have integrated SCP (Short Circuit Protection) due to GaN's shorter SCWT (Short Circuit Withstand Time) and the need for ultra-low latency on SCP operation. However, OTP (Over Temp) & OCP (Over Current) are typically implemented via system DSP.

14.6. Design for $V_{DS(CONT)}$ and $V_{DS(TRAN)}$

GaNSafe power ICs have been designed and tested to provide significant design margin for continuous and transient voltage conditions, for topologies typically used in high power operation up to 22kW. These voltage levels and recommended design margin can be analyzed using Fig. 24 below. When the GaNSafe power IC is switched off, energy stored in the output circuit causes V_{DS} overshoot (V_{SPIKE}), and after dissipation of the stored energy V_{DS} settles to the level of the bus voltage.

- For ***repetitive*** events, derating should be applied from $V_{DS(TRAN)}$ rating (800V) to $V_{DS(CONT)}$ rating (650V max) under the worst case operating conditions.
- It is recommended to design the system such that $V_{DS\text{-}OFF}$ is $\leq$ 520V (80% of $V_{DS(CONT)}$ rating).
- ***Non-repetitive events*** are infrequent, ***one-time*** conditions such as line surge, ESD, and lightning strike. No derating from 800V is needed for non-repetitive V_{SPIKE} durations < 100 µs.

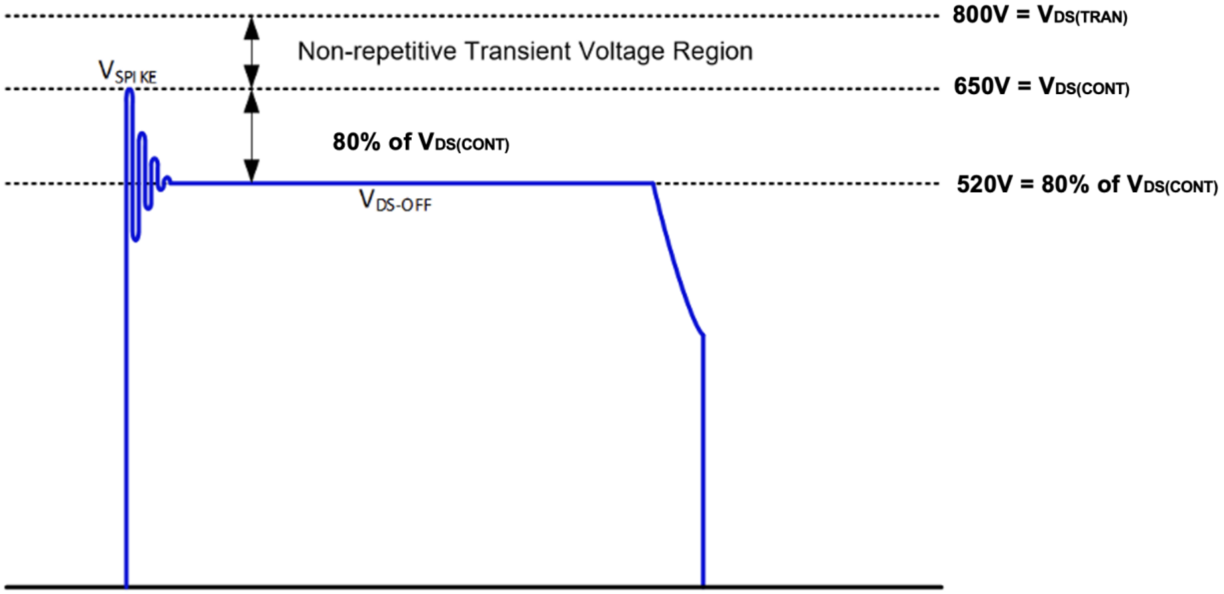


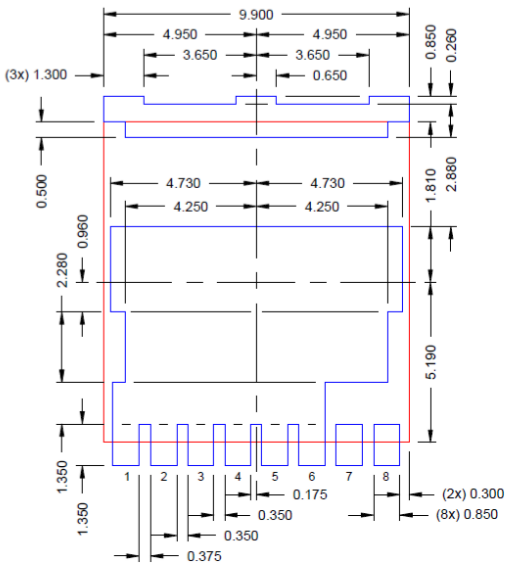
Figure 24. $V_{DS(CONT)}$ and $V_{DS(TRAN)}$

14.7. PCB Layout Guidelines and PCB Footprint

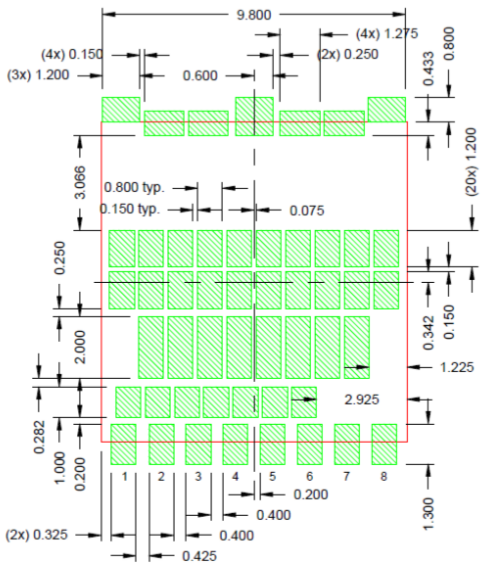
PCB layout is critical for thermal management, noise immunity, and proper operation of the power IC. The following rules should be followed carefully during the design of the PCB layout:

- Place IC filter and programming components **directly adjacent to the GaNSafe power IC**, and reference all these components to the SK pin.
- Place an 0402 site for MLCC between SK and V_{DRIVE} Pins (**directly adjacent to the pins**). This site may be stuffed with a 47pF MLCC if additional noise immunity on V_{DRIVE} Pin is desired.
- Observe the limits on **R_{DRIVE_ON} and R_{DRIVE_OFF} minimum values** in ROC Sect. 7.
- Do ***not*** run power SOURCE currents through SK pin!
- For best thermal management, place thermal vias in the source pad area to conduct the heat out through the bottom of the package and through the PCB board to other layers.
- Use large PCB thermal planes (connected with thermal vias to the source pad) and additional PCB layers to reduce IC temperatures as much as possible.

RECOMMENDED PCB LAND PATTERN*

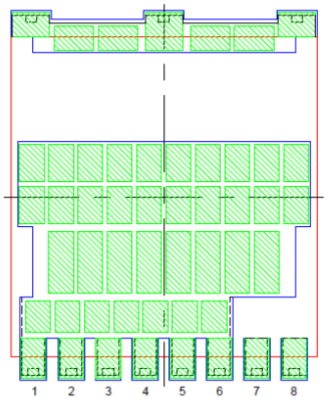


RECOMMENDED STENCIL DESIGN*

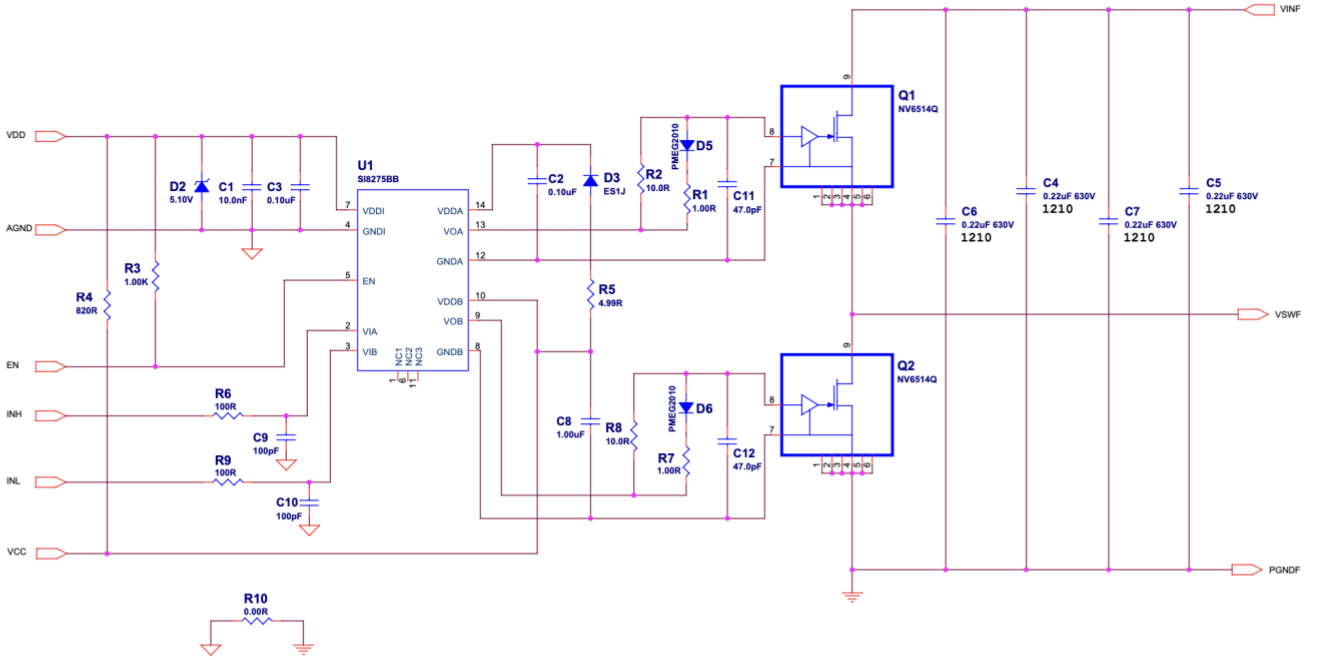


PKG, PCB LAND PATTERN AND STENCIL OVERLAY

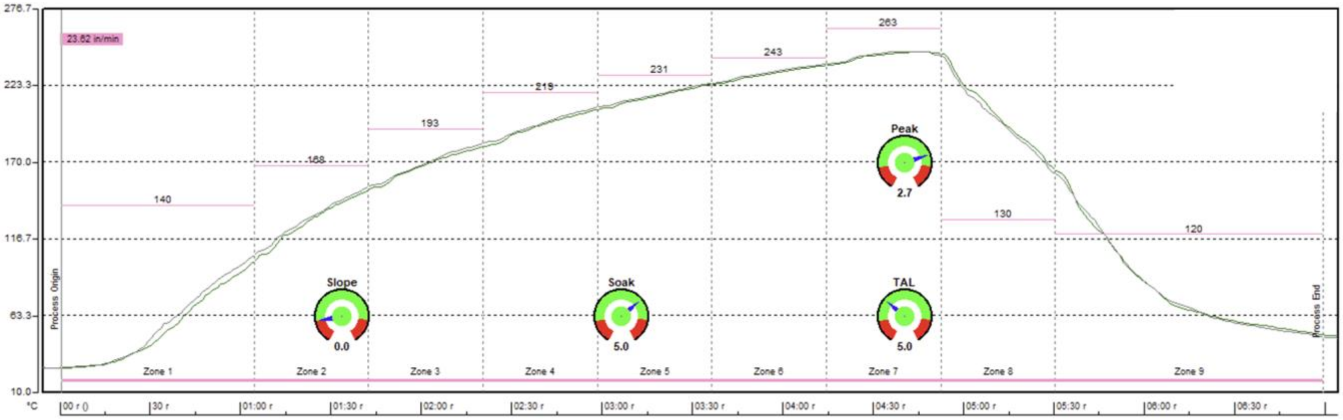
ALL DIMENSIONS ARE IN MILLIMETERS



14.8. Reference Schematic



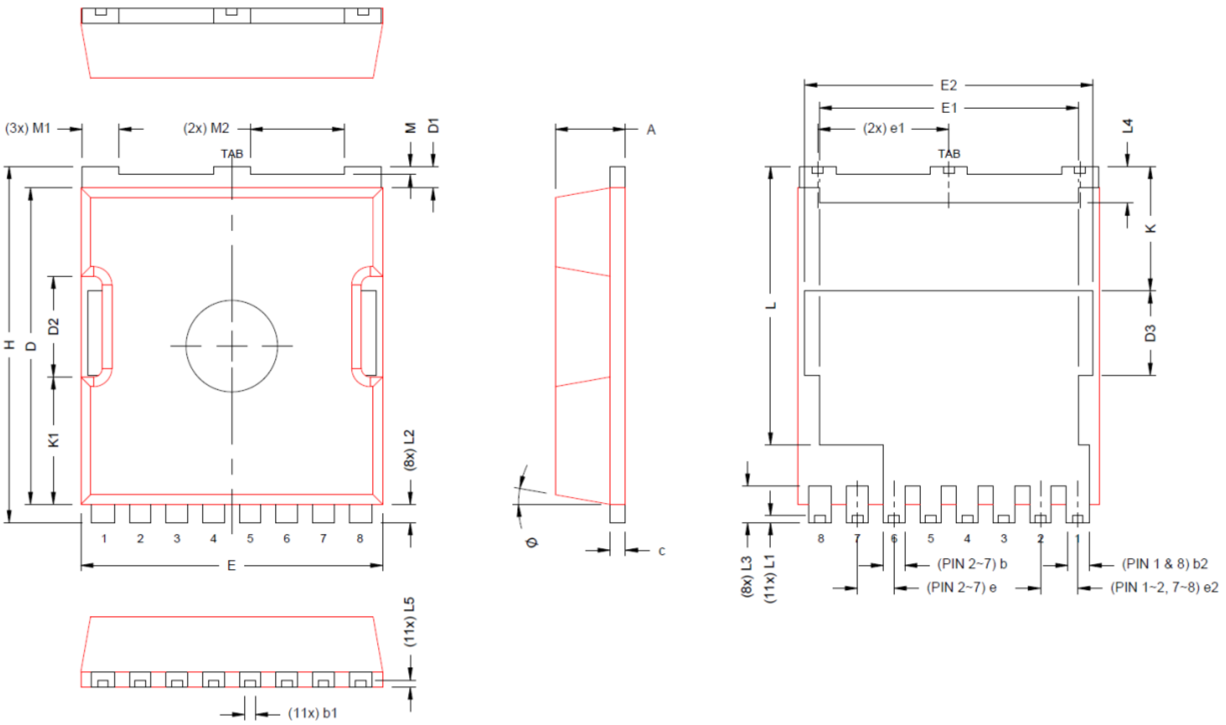
14.9. PCBA SMT IR Oven Profile (*guideline only*):



14.10. Recommended Isolator IC's:

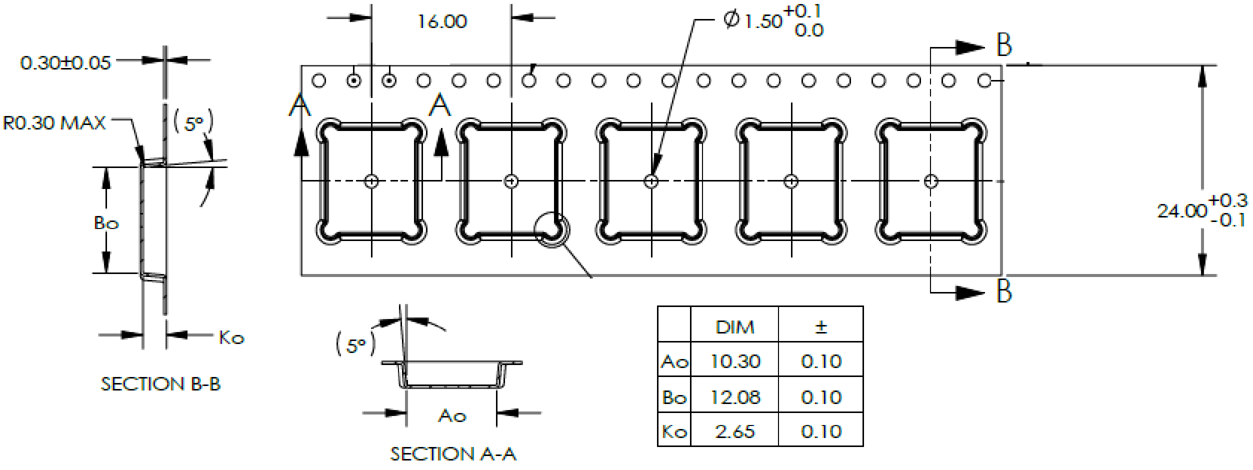
Supplier	Isolated P/N	UVLO Setpoint	CMTI (V/ns)	Drive Strength	Channels
SkyWorks (Si Labs)	SI8273BBD-IS1	VDDI: 1.85V VDDO: 8.0V	200	1.8A source/4A sink	Dual
SkyWorks (Si Labs)	SI8275BBD-IM1	VDDI: 1.85V VDDO: 8.0V	200	1.8A source/4A sink	Dual
NovoSense	NSI6602VB-Q1SWR	VDDI: 2.5V VDDO: 8.0V	150	6A source/8A sink	Dual
NovoSense	NSI6602B-Q1SWR	VDDI: 2.35V VDDO: 8.0V	150	4A source/6A sink	Dual
Infineon	2EDF9275F	VDDI: 2.85V VDDO: 4.2V	150	4A source/8A sink	Dual
Infineon	1EDB7275F	VDDI: 2.65V VDDO: 3.9V	300	5A source/9A sink	Single

15. Package Outline Dimensions:

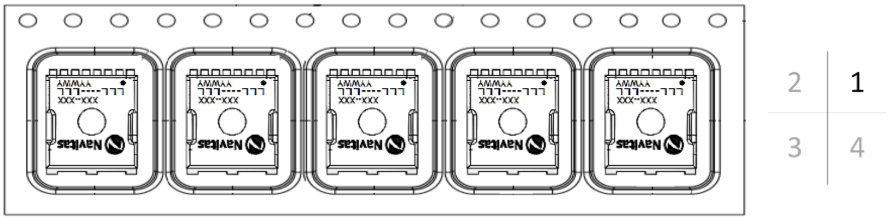


SYM	MIN	NOM	MAX
A	2.15	2.30	2.45
b	0.70	0.70	0.80
b1	–	0.35 REF.	–
b2	0.75	0.75	0.85
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	0.50	0.70	0.90
D2	–	3.30 REF.	–
D3	–	2.77 REF.	–
E	9.70	9.90	10.10
E1	–	8.50 REF	–
E2	–	9.46 REF.	–
e	1.15	1.20	1.25
e1	4.20	4.30	4.40
e2	1.175	1.225	1.275
H	11.48	11.68	11.88
K	–	4.08 REF.	–
K1	–	4.17 REF.	–
L	–	9.13 REF.	–
L1	–	0.23 REF.	–
L2	0.50	0.60	0.70
L3	1.10	1.20	1.30
L4	1.10	1.20	1.30
L5	–	0.23 REF.	–
M	0.16	0.26	0.36
M1	1.10	1.20	1.30
M2	3.00	3.10	3.20
Ø	8°	10°	12°

16. TnR Drawing and Socket Orientation



	DIM	±
Ao	10.30	0.10
Bo	12.08	0.10
Ko	2.65	0.10



* JEDEC Standard Orientation.

17. 20-Year Limited Product Warranty

A 20-year limited warranty applies to packaged Navitas GaNSafe power ICs in mass production, subject to the terms and conditions of Navitas' express limited product warranty (available at https://navitassemi.com/terms-conditions). The warranted specifications include only the MIN and MAX values listed only in Table 6 (Absolute Maximum Ratings), Table 8 (ESD Ratings), and Table 10 (Electrical Characteristics) of this datasheet. Typical (TYP) values or other specifications are not warranted.

18. Ordering Information

Part Number	Qualification	Package	MSL Rating	TnR Sizes/Qtys
NV6512C	JEDEC	TOLL-4L Bottom-cooled SMD	3	Standard (13" dia) Qty1,500
NV6512C-RA				Mini-Reel (7" dia) Qty340
NV6512CQ	AEC-Q100 Grade 1 -40 °C to +125 °C			Standard (13" dia) Qty1,500
NV6512CQ-RA				Mini-Reel (7" dia) Qty340

19. Revision History

Date	Status	Notes
Jan 19th, 2024	Final	• First Datasheet Publication
Jan 24th, 2024	Final	• Normalized product family R_{DSON} TempCo curve • Added Navitas 20-Year Limited Product Warranty
Feb 23rd, 2024	Final	• Updated POD (TOLL) and TnR Socket drawing & Pin1 orientation • Updated Electrical Characteristics table data & Fig. 19 curve • Updated $R_{\Theta\_J\text{-}C}$ table
Jul 1st, 2024	Final	• Updated section 14 Applications
Aug 1st, 2024	Final	• Updated V_{DRIVE} ratings on Pages 1, 3, 4, and 11
Sep 17th, 2024	Final	• Added T_{RISE} and T_{FALL} to the Electrical Characteristics table

Additional Information

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