NU1619: High Efficiency, High Integration Wireless Power Receiver/Transmitter

1 Features

- Integrated 28V high-efficiency synchronous rectifier
- Integrated Low-Dropout LDO to Provide Regulated Output Programmable V_{out} from 3.5V to 20V with 40mV step
- Programmable I_{out} regulation from 0.1A to 2.2A with 20mA step
- Local thermal loop to dynamically regulate output power
- Integrated full bridge inverter and PWM control
- Programmable FOD gain and offset
- 1.8V reference voltage output
- V5V supply path management
- Robust OVP, OCP, OTP, and SCP
- 10 Bits ADC for voltage, current and temperature measurement
- Integrated 32Bit MCU
- I^2C programmability
- In-system programmability
- Bi-directional communications ASK + FSK
- INT Output
- 54-WCSP 2.90mm x 4.04mm, 0.4mm pitch

2 Applications

- WPC 15W EPP Compliant Receiver with Maximum 40W Received Power
- WPC 5W BPP Compliant Transmitter with Maximum 10W Transmit Power
- Wireless Power Receiver for Smartphones, Power Bank
- Receiver with Custom Defined FSK and ASK Communication
- Wireless Power Receiver for Medical, Industrial and Consumer Equipment

3 Descriptions

NU1619 is a highly integrated and highly efficient wireless power receiver. It integrates a synchronous rectifier designed for a wide frequency range and a programable low drop-out regulator for the optimal system efficiency. The regulator can provide a wide range regulated voltage or current output; both can be programmable through an I2C interface. NU1619 can conduct bi-directional communication with a transmitter system through ASK and FSK. The communication is compliant with WPC.

NU1619 can also be operated as a transmitter (Tx) to charge another receiver. Only few external components are needed and maximum 10W power can be transferred.

NU1619's flexibility is provided by an on-chip 32Bit MCU which can customize and optimize the device for various applications and custom needs. The programmability includes output power, bidirectional communication scheme, system protection, status reporting and error reporting.

NU1619 also includes standard protection functions such as input under-voltage lockout, short-circuit protection, overvoltage protection and thermal shutdown. These provisions further enhance the reliability of the system solution.

The device is housed in a compact 2.90mm×4.04mm WCSP package.

Content

4 Pin Configuration and Functions

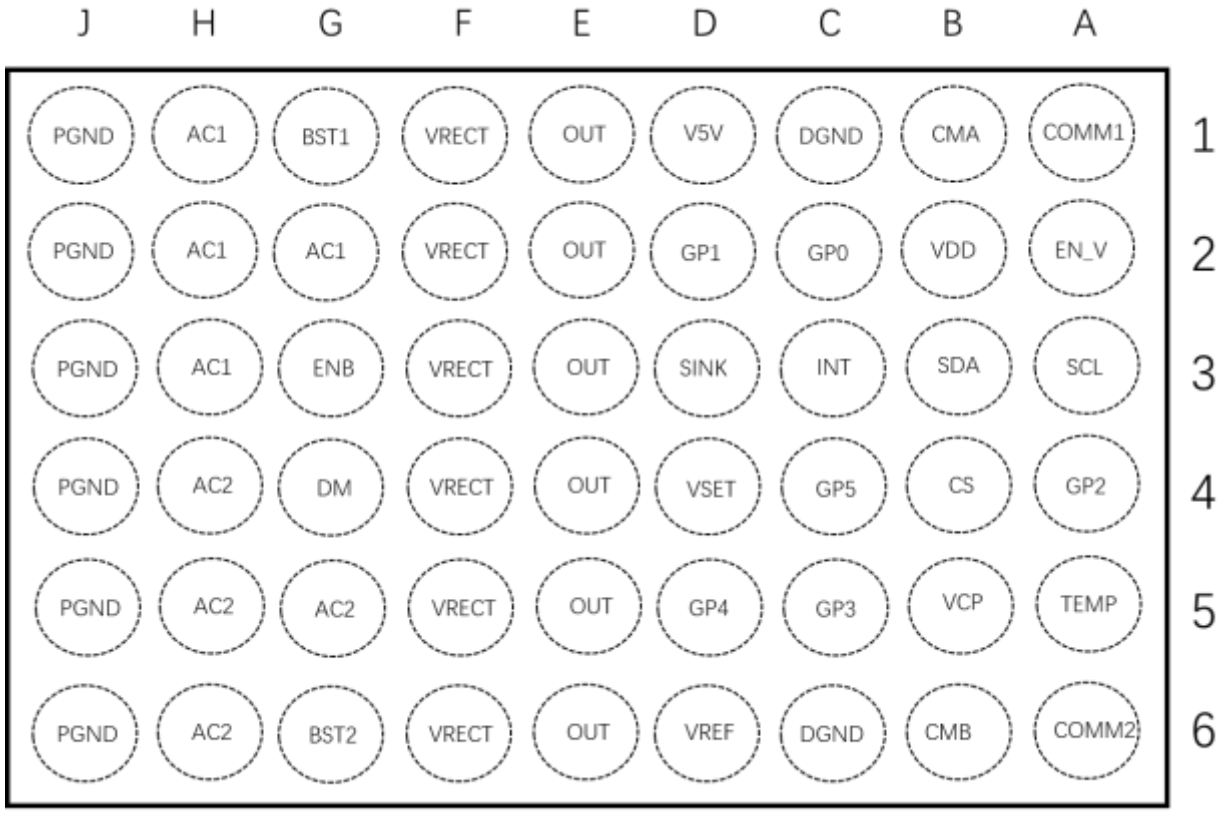


Figure 1. NU1619-WCSP Top View

Pin		I/O	Description
Name	No.		
COMM1/ COMM2	A1/ A6	O	Open-drain output used to communicate with the transmitter. Connect a capacitor between this pin and AC1/AC2.
CMA/ CMB	B1/ B6	O	Open-drain output used to communicate with the transmitter. Connect a capacitor between this pin and AC1/AC2.
DGND	C1/C6	GND	Digital Ground.
V5V	D1	P	5V LDO output for IC internal use. Connect a capacitor between this pin and DGND.
OUT	E1~E6	P	Regulated output voltage pin in Rx mode. Connect capacitor between this pin and ground. This will be power input pin in Tx mode.
VRECT	F1~F6	P	Output of the synchronous rectifier. Connect capacitor between this pin and ground.
BST1/ BST2	G1/ G6	I/O	Supply rail for the high-side gate driver. Connect a capacitor between this pin and AC1/AC2.
AC1	H1~H3, G2	P	AC input power. Connect to the resonant circuit of L and C.

AC2	H4~H6, G5	P	
PGND	J1~J6	GND	Power Ground.
EN_V	A2	I	Enable the external supply connected the VDD pin.
VDD	B2	P	The External power supply pin. When EN_V= high, this PIN will be connected to the internal circuit as the supply.
GP0	C2	I/O	General purpose logic IO pin.
GP1/ VPON/ADC1	D2	I/O	High power logic output pin can provide 30mA max current as push pull output. Analog input pin.
SCL	A3	I	I2C clock pin.
SDA	B3	I/O	I2C data pin. Open-drain output.
INT	C3	O	Interrupt output. Open-drain output.
SINK	D3	O	Open-drain output for controlling the rectifier clamp. Connect a resistor between this pin and the VRECT pin.
ENB	G3	I	Chip enable pin. Low logic active.
GP2	A4	O	General purpose logic Output PIN.
CS	B4	I	Tx mode current sense PIN.
GP5	C4	I/O	Reserved
VSET/ADC2	D4	I/O	General purpose analog IO PIN, and analog input
DM	G4	I	Tx mode demodulation input PIN.
TEMP/ADC3	A5	I	NTC input pin for external temperature sense. Connect NTC and a small cap in parallel between this pin and DGND.
VCP	B5	P	Driver supply of OUT LDO.
GP3	C5	O	General purpose logic Output PIN.
GP4/ADC0	D5	I/O	General purpose logic output PIN, and Analog input.
VREF	D6	O	Output 1.8V reference voltage.

5 Specifications

5.1 Absolute Maximum Ratings

Pins	Rating	Units
SCL, SDA, DM EN_V, V5V, VDD, TEMP, VSET, ENB, GP0~GP5	-0.3~6	V
VRECT, SINK, CMA, CMB, COMM1, COMM2, AC1, AC2	-0.3~30	V
VREF	-0.3~2.8	V
INT	-0.3~6	V
VCP	-0.3~35	V
VRECT to OUT	22	V
BST1, BST2	-0.3~AC1+6, AC2+6	V
OUT, CS	-0.3~22	V
Max Current on SINK	1	A
Max Current on COMM1/COMM2	1	A
Max Current on CM1A/CM2B	1	A
Max Current on AC1/AC2	5	A
Maximum OUT output current	2.5	A
Operating Junction Temperature, T_J	-40~125	°C
Ambient Operating Temperature, T_A	-40~85	°C
Storage Temperature, T_{stg}	-55~125	°C

5.2 ESD Ratings

Test Model	Pins	Ratings	UNIT
Human Body Model	All pins except CMA and CMB	+/-2000	V
	CMA, CMB pins	+/-1000	V
Charged Device Model	All pins	+/-500	V

5.3 Recommended Operating Condition

	Max	UNIT
OUT to PGND Voltage	20	V
OUT PIN Output Current	2.1	A

5.4 Package Thermal Ratings

		UNIT
Junction-to-ambient thermal resistance, $R_{\Theta JA}$	40	°C/W

5.5 Electrical Characteristics

V_{RECT}=19V, T_j=-40 °C to 125°C (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply						
V_{V5V}	V_{V5V} Under-voltage lock out threshold	V_{V5V} ramps up[a]	-5%	3.2	+5%	V
V_{V5V_HYS}	V_{V5V} Under-voltage lock out hysteresis voltage	V_{V5V} ramps down[a]		250		mV
$V_{RECT\_OVP\_HARD}$	Over-voltage threshold for safety	V_{RECT} ramps up	-5%	27	+5%	V
$V_{HYS\_OVP\_HARD}$	Over-voltage hysteresis for safety	V_{RECT} ramps down		0.35		V
$V_{RECT\_OVP\_SOFT}$	Soft Over-voltage threshold	V_{RECT} ramps up	-5%	18.7	+5%	V
$V_{HYS\_OVP\_SOFT}$	Soft Over-voltage hysteresis	V_{RECT} ramps down		0.5		V
V_{RECT_OVP1}	Over-voltage threshold level 1	V_{RECT} ramps up[b]	-5%	19.4	+5%	V
V_{HYS_OVP1}	Small Over-voltage hysteresis level 1	V_{RECT} ramps down[c]		0.3		V
	Big Over-voltage hysteresis leve1	V_{RECT} ramps down[c]		6		V
I_{Q_RECT}	Quiescent operating current into V_{RECT}	ENB=low, EN_V=low no load, no switching		5.5		mA
I_{SD_RECT}	Shutdown current into V_{RECT}	ENB=high, EN_V=low		2.6		mA
OUTPUT REGULATION (POWER DCDC)						
V_{OUT}	Output voltage range		3.5		20	V
V_{OUT_STEP}	Output voltage step	Vout=3.5V to 20V		20		mV
V_{OUT_REG}	Output voltage regulation	V_{RECT}=Vout+0.3V, V_{OUT}=18V, I_{OUT}=1A	17.46	18	18.54	V
		V_{RECT}=Vout+0.3V, V_{OUT}=12V, I_{OUT}=1A	11.64	12	12.36	
$I_{SENSE\_RX\_K}$	RX current sense gain	I_{OUT}=0.8A to 1.6A,		1.004		
$I_{SENSE\_RX\_OS}$	RX current sense offset	I_{OUT}=0.8A to 1.6A		1.637		mA
$I_{SENSE\_TX\_K}$	Tx current sense gain	I_{OUT}=0.8A to 1.6A,		1.008		
$I_{SENSE\_TX\_OS}$	TX current sense offset	I_{OUT}=0.8A to 1.6A		1.0		mA

I_{LIM_RANGE}	Current limit range		0.1		2.2	A
I_{LIM_STEP}	Current limit step			20		mA
I_{LIM_acc}	Current limit accuracy		-10%	0	10%	
External Power supply						
V_{UVLO_VDD}	V_{DD} Under-voltage lock out threshold	V_{DD} ramps up	-5%	3.2	+5%	V
$V_{UVLO\_VDD\_HYS}$	V_{DD} Under-voltage lock out hysteresis voltage	V_{DD} ramps down		250		mV
I_{Q_VDD}	Quiescent operating current into V_{DD}	ENB=low, EN_V=high		4.8		mA
I_{SD_VDD}	Shutdown current into V_{DD}	ENB=high, EN_V=low			1	uA
LOW POWER LDO						
V_{5V}	5V supplier	I_{V5V}=10mA	4.56	4.8	5.04	V
I_{5V}	5V current limit		30			mA
V_{REF}	Reference voltage	I_{REF}=1mA		1.8		V
I_{REF}	Reference current limit		10			mA
IO						
V_{HIGH_LOGIC}	ENB, INT, GP0, GP1, GP2, GP3, GP4, GP5, SCL, SDA		1.4			V
V_{LOW_LOGIC}	ENB, INT, GP0, GP1, GP2, GP3, GP4, GP5, SCL, SDA				0.6	V
R_{COMM}	COMM1/COMM2 switch on resistance			0.3		ohm
R_{CM}	CMA/CMB switch on resistance			0.3		ohm
R_{SINK}	SINK switch on resistance			0.4		ohm
Thermal Shutdown						
T_{OTP}	Over-temperature protection threshold			155		°C
T_{HYS_OTP}	Over-temperature protection hysteresis			30		°C

[a] V5V pin has two power supply channels: VDD or VRECT
[b] V_{RECT_OVP1} has eight settings value. The setting range is from 19.4V to 26.0V.
[c] V_{HYS_OVP1} has two options (small/big over-voltage hysteresis level).

6 Register Maps

6.1 General Purpose Registers (Read Only)

Address and Bit	Default Value	Default Function and Description
0x0008 [7:0]	0x00	ADC Channel TEMP_SNS[7:0]. TEMP pin voltage sense channel. $[VALUE]_{DEC}$ = 1023*1.8V*R_{NTC}/(R_9+ R_{NTC})/2.5V refer to *9.7 ADC*
0x0009 [7:0]	0x00	ADC Channel VOUT_SNS[7:0]. VOUT pin voltage sense channel. V_{OUT}=22.5V*$[VALUE]_{DEC}/256_{DEC}$
0x000A [7:0]	0x00	ADC Channel VRECT_SNS[7:0]. VRECT pin voltage sense channel. V_{RECT}=27.5V*$[VALUE]_{DEC}/256_{DEC}$
0x000B [7:0]	0x00	ADC Channel IOUT_SNS[7:0]. VOUT pin current sense channel. I_{OUT}=2.5A*$[VALUE]_{DEC}/256_{DEC}$
0x0020 [7:0] ~ 0x0024 [7:0]	0x00	Reserved

6.2 General Purpose Registers (Read/Write)

Address and Bit	Default Value	Default Function and Description
0x0000 [7:0] ~ 0x0007 [7:0]	0x00	Control registers, setting and control operation mode
0x000C [7:0]	0x00	Reserved
0x000E [7:0]	0x00	Reserved

6.3 Start-up Mode Control Registers (Read/Write)

The following is the control register for start-up mode selection.

Address and Bit	Default Value	Function and Description
0x000D [7:4]	0x0	Writing 0x2: enable TX mode
0x000D [3:0]	0x0	Reserved

6.4 Chip ID Registers (DTM Read Only)

The followings are chip ID registers which can only be read in Design Test Mode (DTM).

Address and Bit	Default Value	Description
0x0096 [7:0]	0x19	The second two characters of chip ID
0x0097 [7:0]	0x16	The first two characters of chip ID

7 Functional Block Diagram

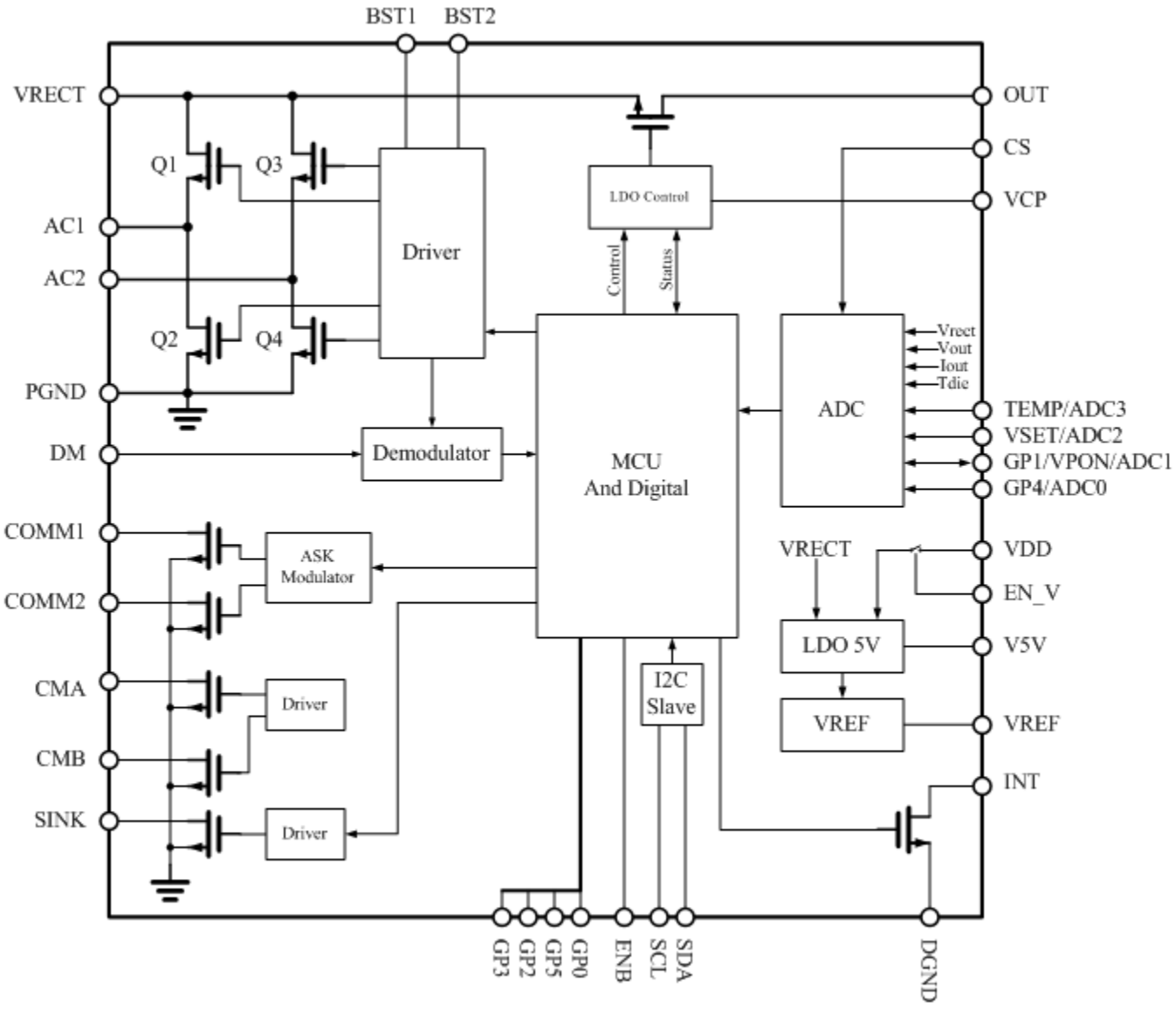


Figure 2. Function Block Diagram

8 Typical Characteristics

The following testing is using NU1020+NU1513 wireless transmitter EVM with MPA2 Tx Coil.

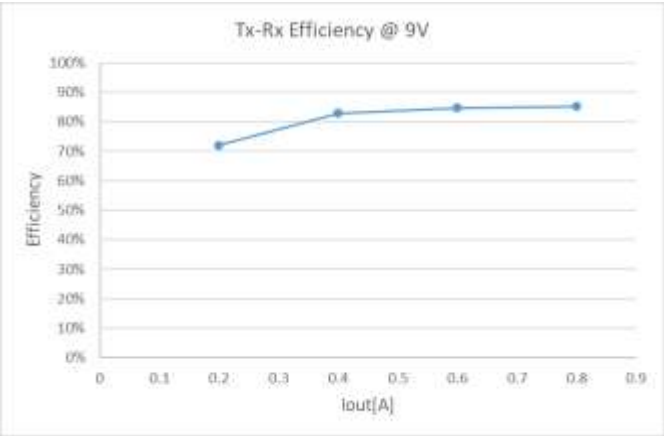


Figure 3. Efficiency: VOUT=9V

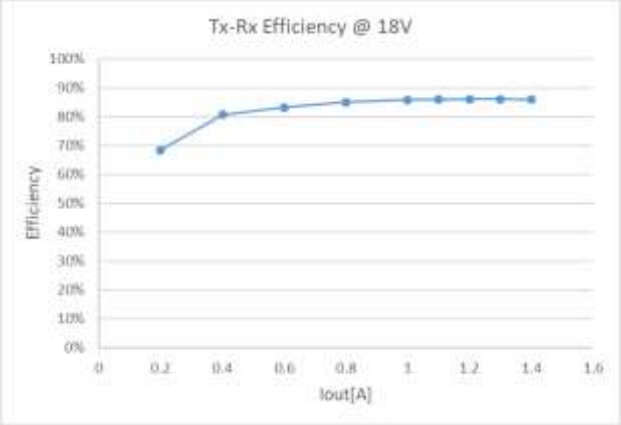


Figure 4. Efficiency: VOUT=18V

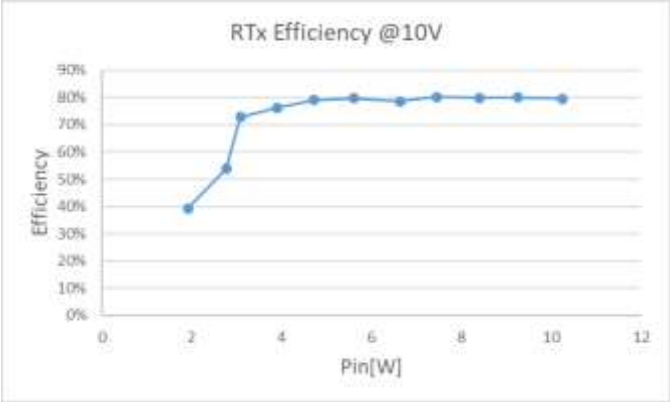


Figure 5. Reverse Charge Efficiency: VIN=10V

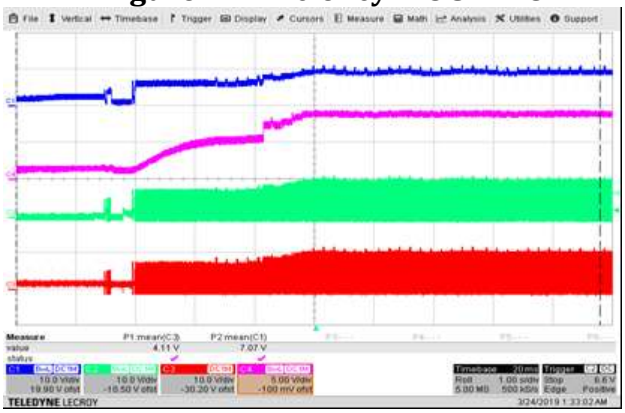


Figure 6. Start up: VOUT=9V

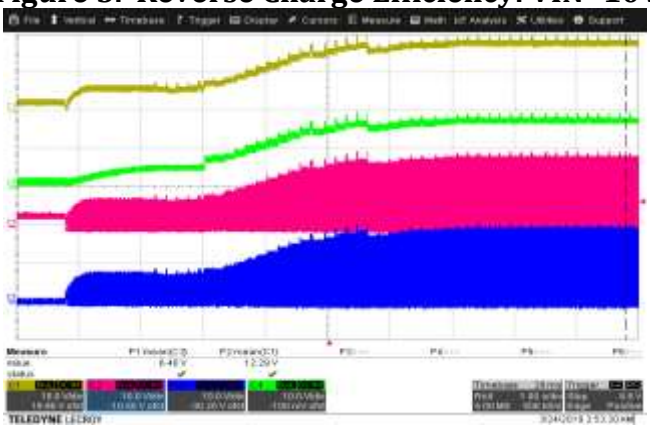


Figure 7. Start up: VOUT=18V

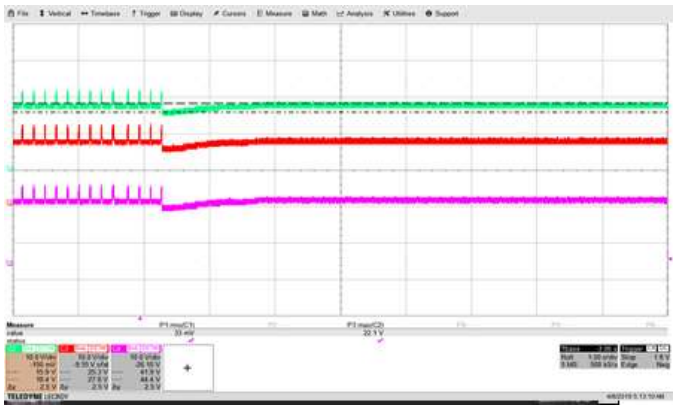


Figure 8. Transient Response: VOUT=18V, IOUT=0A to 0.5A

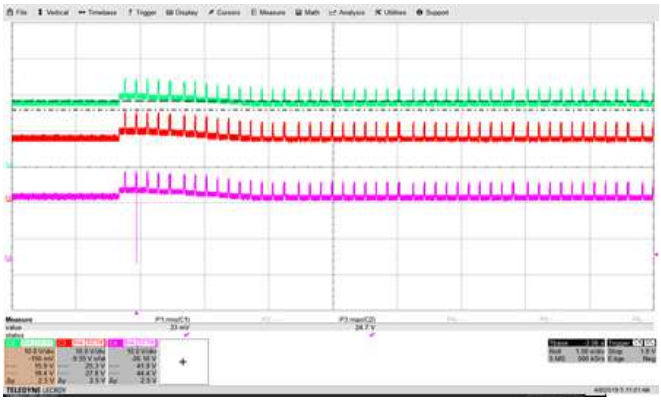


Figure 9. Transient Response: VOUT=18V, IOUT=0.5A to 0A

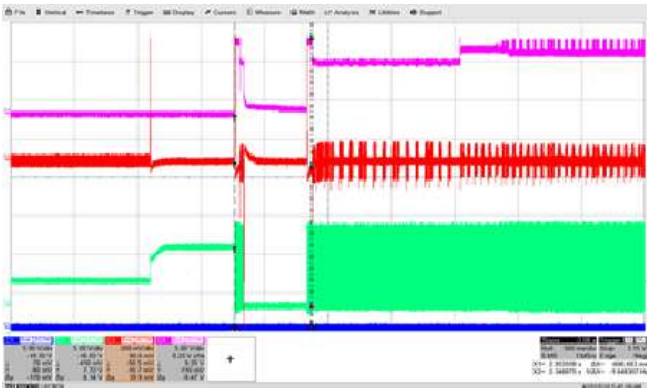


Figure 10. Tx mode Start up: VIN=10V

Note: (1) Figure 6~7: CH1-V_{RECT}; CH2-AC1; CH3-Comm; CH4-Vo
(2) Figure 8~9: CH1-NA; CH2-Vo; CH3- V_{RECT}; CH4-Sink
(3) Figure 10: CH1-NA; CH2-SW; CH3- DM; CH4- V_{RECT}
(4) The typical characteristics were tested at TA = 25°C, unless otherwise noted

9 Application Descriptions

9.1 System Overview

In a wireless power transfer system, the transmitter system generates magnetic field by feeding AC current into a transmitting coil. The magnetic field is coupled to a receiving side coil and the coupled energy is further maximized by matching the transmitter side impedance. The outputs of the resonant circuit are connected to the AC1 and AC2 pin of the IC which are the inputs to the on-chip synchronous rectifier. The rectifier output is an unregulated voltage connected to the VRECT pin of the IC. To provide a well-regulated voltage source or current source to the downstream circuit, an ultra-low dropout LDO is connected between the VRECT pin and the OUT pin.

The communication between the transmitter side (Tx) and receiver side (Rx) is needed to provide feedback on the power requirement from the receiver to the transmitter. NU1619 is equipped with bi-directional communication compliant with the WPC standard. The communication protocol can be customized for any proprietary systems. The Rx to Tx communication is implemented by turning on the COMM1 and COMM2 or CMA and CMB internal switches and inserting additional capacitance to the Rx resonant circuit. This modulation of Rx impedance can be detected on the Tx side as amplitude modulation of its coil voltage and current waveform. Tx to Rx communication is done through modulating the transmitting frequency. NU1619 is equipped with frequency measurement circuit to sense and decode the modulated frequency.

Protection is a critical requirement to wireless power receivers, especially the over-voltage protection on the VRECT pin. The coupling factor between Tx and Rx, hence the coupled energy between Tx and Rx, can change suddenly and significantly as the proximity between Rx and Tx coils is altered by end users without notice. When the coupled energy increases, the VRECT voltage can rise and potentially exceed its maximum voltage rating to cause IC damage. NU1619 incorporates comprehensive over-voltage protection against any transient conditions through the SINK pin.

9.2 Power Supply

When the receiving coil is placed in the magnetic field created by the transmitter analog ping, DC voltage is established on the VRECT pin through the body diode of the rectifier MOSFET initially. V5V follows VRECT voltage through an inner start up circuit. When V5V is above 3V, the 5V LDO, which provides IC internal bias voltage, is powered up to turn on internal circuit blocks, such as MCU, protection circuits and rectifier switches. In addition, the communication from Rx to Tx takes place to instruct Tx to deliver power. A capacitor of typical value of 10uF to 40uF should be placed at the VRECT pin to provide DC voltage to the IC.

When the receiving coil is removed from the magnetic field, or the transmitter is turned off, the voltage of the VRECT pin is discharged by the load connected to the OUT pin and IC operating current. If the V5V voltage drops below 2.8V, the IC enters the shutdown mode.

V5V can also be powered up with an external power supply from VDD pin, the power path is controlled by the EN_V pin. When VDD is above 3.2V, then set EN_V high, V5V follows VDD voltage

through an inner power path. When VDD drops below 3V or set EN_V to Low, the VDD power path will be turn off.

9.3 Synchronous Rectifier

The NU1619 has an integrated synchronous rectifier to ensure efficient AC-to-DC conversion, especially for the heavy output load. It has built in a reliable and efficient switch control algorithm to minimize the dead-time while eliminating the possibility of the shoot-through inside the rectifier.

The BST1 and BST2 pins are connected to the internal boost-strap circuit to provide supply rails to the high-side MOSFET Q1 and Q3.

9.4 Output LDO

The output voltage of the LDO can be programed through I^2C interface or an external resistor divider network connected to the VSET pin. The programmable voltage range is from 3.5V to 20V with 40mV step. The external resistors should be selected and the formula below:

$$R_2/(R_1+R_2) = 0.09*V_{O\_SET}/V_{REF}$$

Where R1 is between VSET and VREF, R2 is between VSET and DGND, V_{O_SET} (V) is the targeted output voltage and V_{REF}(V) is the reference voltage.

The output current limit of the LDO can also be programed through I^2C interface, the programmable current range is 0.1A to 2.2A with 20mA step.
The LDO is protected by the over-current protection. During the over-current protection, SINK switches are turned on to limit the coupled energy. And an interrupt will be triggered to MCU for more action.
LDO has a soft-start feature to prevent in-rush current caused by charging output capacitor during the startup. The soft start gradually turns on the LDO to control and limit its current.

9.5 Over-Voltage Protection

Since the feedback loop between Rx and Tx is inherently slow, the transmitter is unable to reduce the power output instantly when the overvoltage condition occurs on the receiver side. The delay can be in the range of tens or even hundreds of milli-seconds which is a long time enough to damage the IC. The over-voltage protection circuit engages immediately upon the occurrence of the over-voltage condition. The protection circuit will be creating a 'bleeding' resistor (One 620Ω resistors in 0805 packages is recommended) to the VRECT pin to dissipate the power through the resistor.

9.6 Over-Current Protection

NU1619 integrates a reliable over current protection circuit. Current of the LDO is sensed and compared to the over-current protection threshold (Iocp). If the current exceeds the threshold, the internal the over-current protection circuit is triggered, and LDO and PWM inputs will be turned off. The OCP threshold can be set through I²C.

9.7 ADC

NU1619 integrates an accurate 10bit ADC which takes inputs from internal signals such as VRECT voltage, output voltage and current. These signals are used to set the proper VRECT voltage through communication with the transmitter. Please refer to *Register Maps* to get more detail information.

NU1619 can monitor the external temperature through the TEMP pin, a filter capacitor and the value of 10nF is recommended connect with TEMP pin. The formula below shows the ADC value of the external temperature where the NTC is placed according to the R_{NTC} (to DGND) and R9 (to VREF):

$$ADC_{TEMP}\,[VALUE] = 1023*1.8V*R_{NTC}/(R_9+ R_{NTC})/2.5V$$

Show as Figure 11, ADC_{TEMP} is the ADC channel [VALUE] from TEMP PIN. 1.8V is the default output voltage of VREF PIN. 2.5V is the internal reference voltage of ADC.

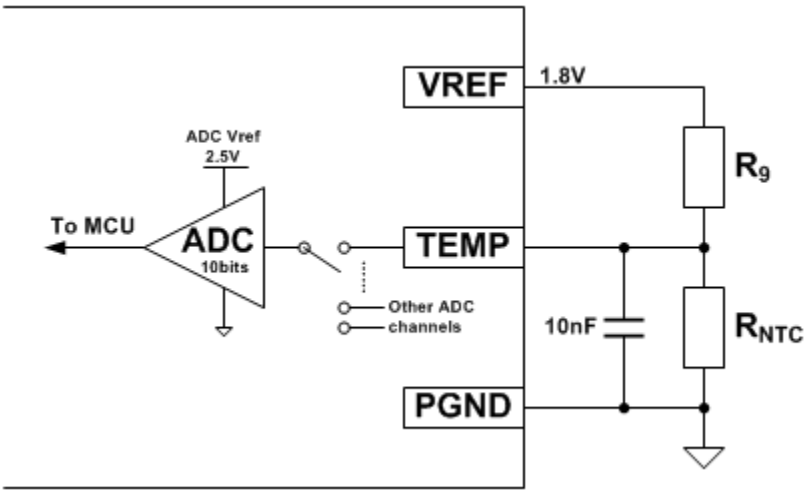


Figure 11. External temperature **ADC** reference circuit.

9.8 I²C, INT

NU1619 allows for the I²C communication with both SCL and SDA, see *Register Maps* for more information.

INT pin is an open-drain and LOW active pin. Connect a resistor (e.g. 5.1K) between this pin and V5V. This pin is pulled high during normal mode. Under over-current, over-voltage, short-circuit, over-temperature conditions or another interrupt, the INT pin is pulled low to indicate a fault condition. The fault mode can be read through the I²C interface.

9.9 Inverter control of Tx Mode

When NU1619 operates at Tx MODE, an internal PWM generator controls the Q1~ Q4 which operate as a full bridge inverter. For a typical WPC transmitter, the AC1 and AC2 are complementary in logic and have 50% duty cycle in the frequency range of 110KHz to 205KHz. When reaching 205KHz, the duty cycle can be reduced below 50% to further limit the power output.

The PWM controller can also be independently control the AC1 and AC2 duty cycle and frequency. This allowed Q1~ Q4 operate as a half bridge inverter

9.10 Digital Demodulation

A digital demodulation circuit is integrated inside NU1619. The DM pin is used as an analog input pin. The IC detects the envelope of the peak voltage of the connecting node (Vcoil) between the resonant inductor and capacitors, decodes the voltage signals, and sends out the decoded signals to MCU.

10 Layout Guidelines

Show as Figure 12 and Figure 13, Coil connects from both sides of IC to Pins AC1 and AC2, a ground is place at GND Pin. The decoupling Capacitor of Vrect and Vout placed near by IC, to minimize the power loop of Vrect to GND and Vout to GND.

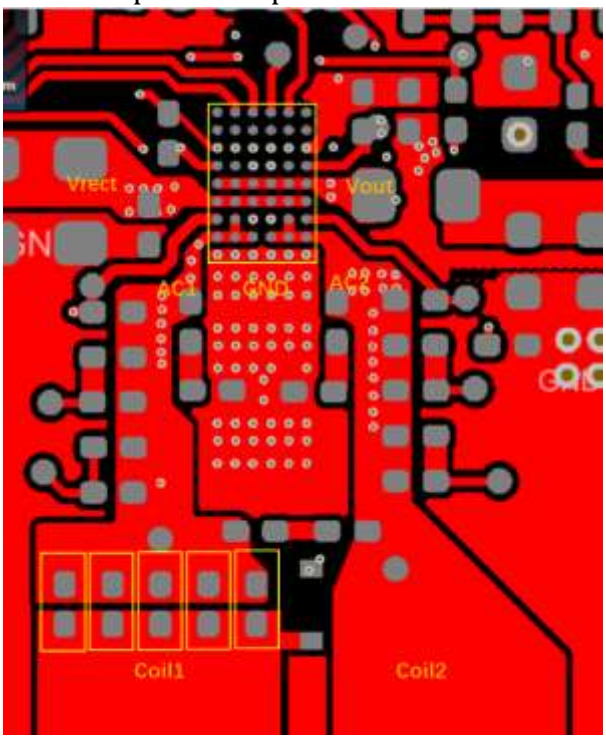


Figure 12: top layer

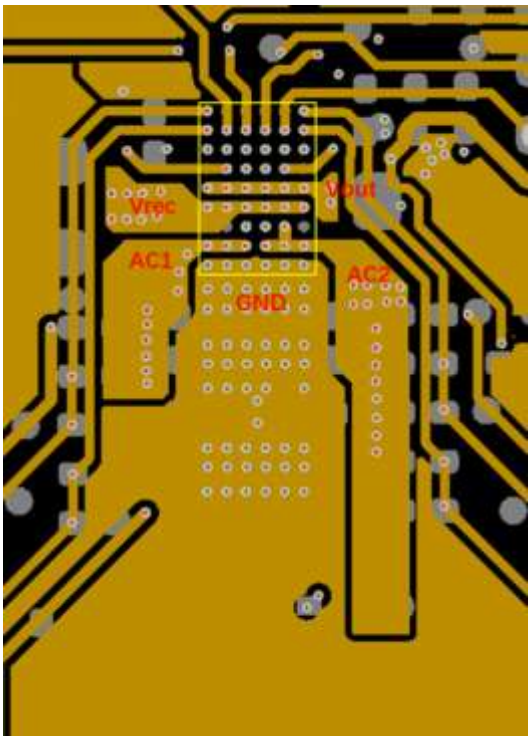


Figure 13: second layer

Show as Figure 14 and Figure 15, Power pin AC1, AC2, Vrect and Vout are connected by blind holes to top layer and the second layer, Show as green region.
Signal pin COMM1, COMM2, CMA, CMB, VCP, CS, SDA, VDD, GP4, VPON are connected by blind holes to top layer and the second layer, Show as Blue region.

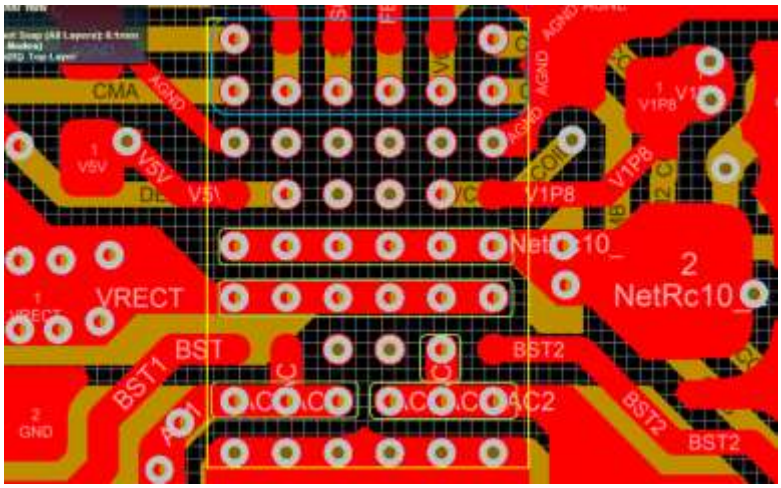


Figure 14: blind holes

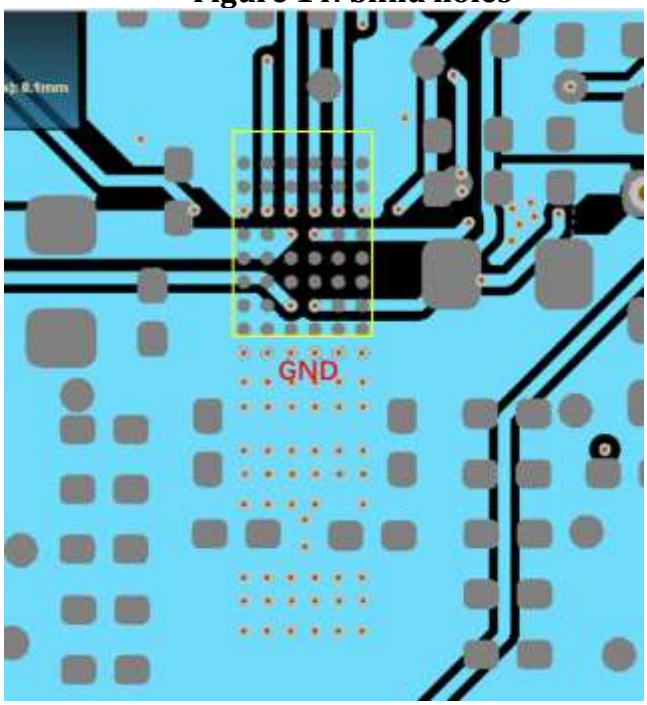


Figure 15: third layer

Show as Figure 16, bottom layer is Ground. There are a power GND and a signal GND, both GND are connect by a 0ohm resistor, the connect point is near Vout capacitor's negative node.

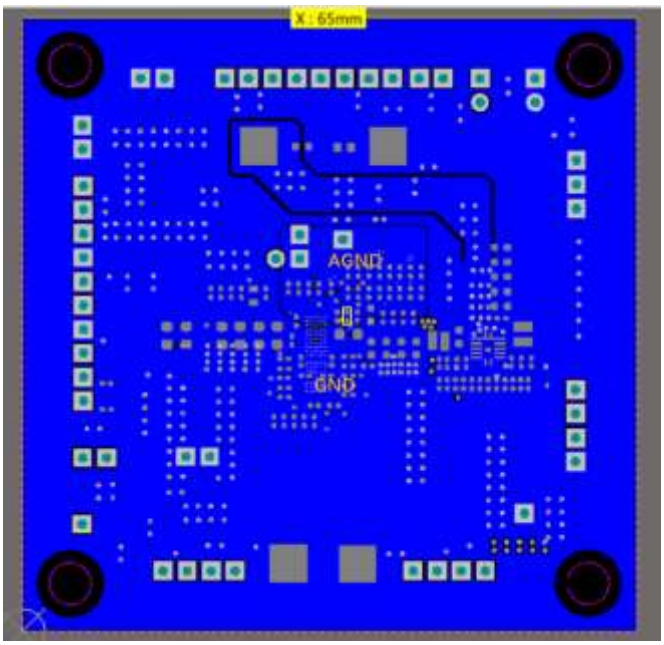
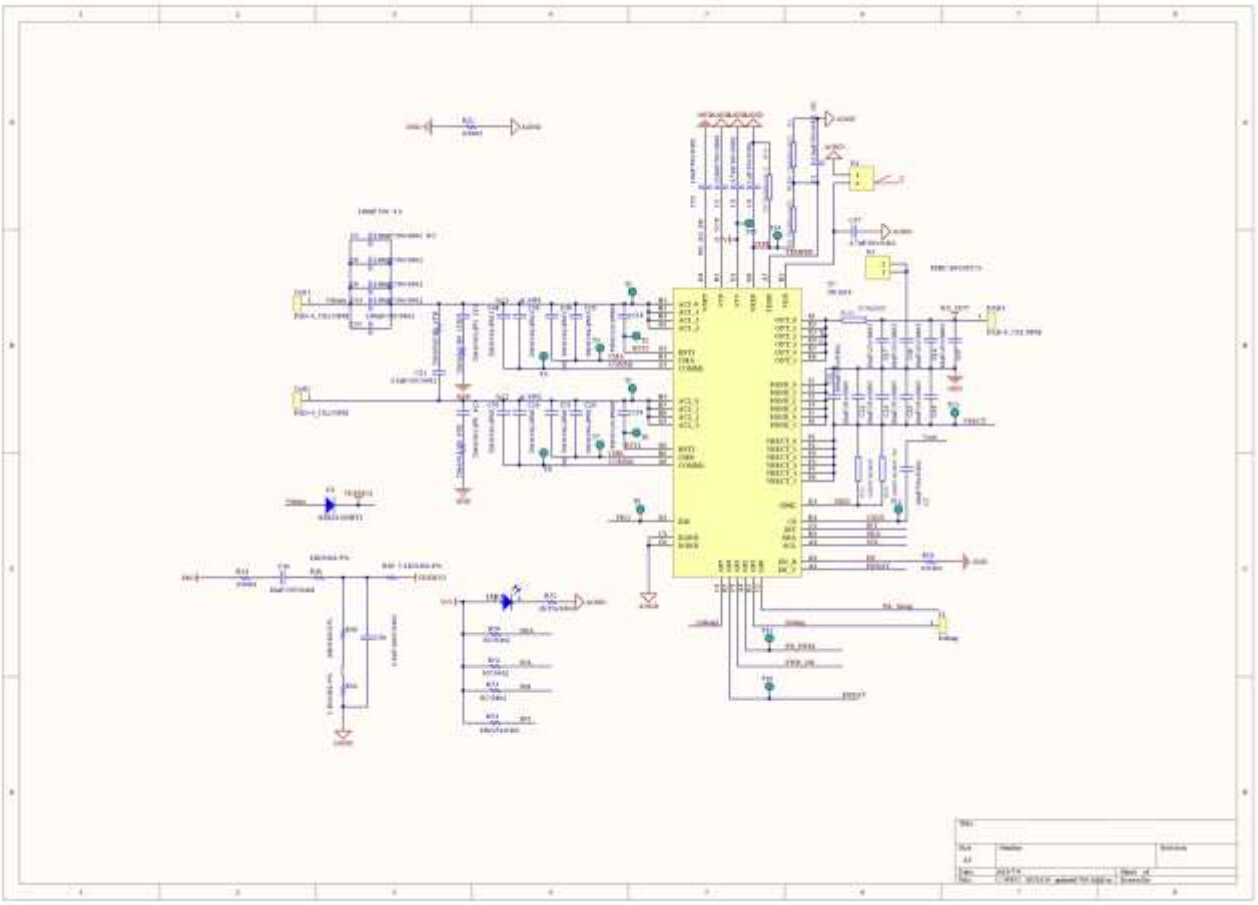


Figure 16: Bottom layer

Note: Make the resonant power routing loop as small as possible and keep away from another signal circuit.

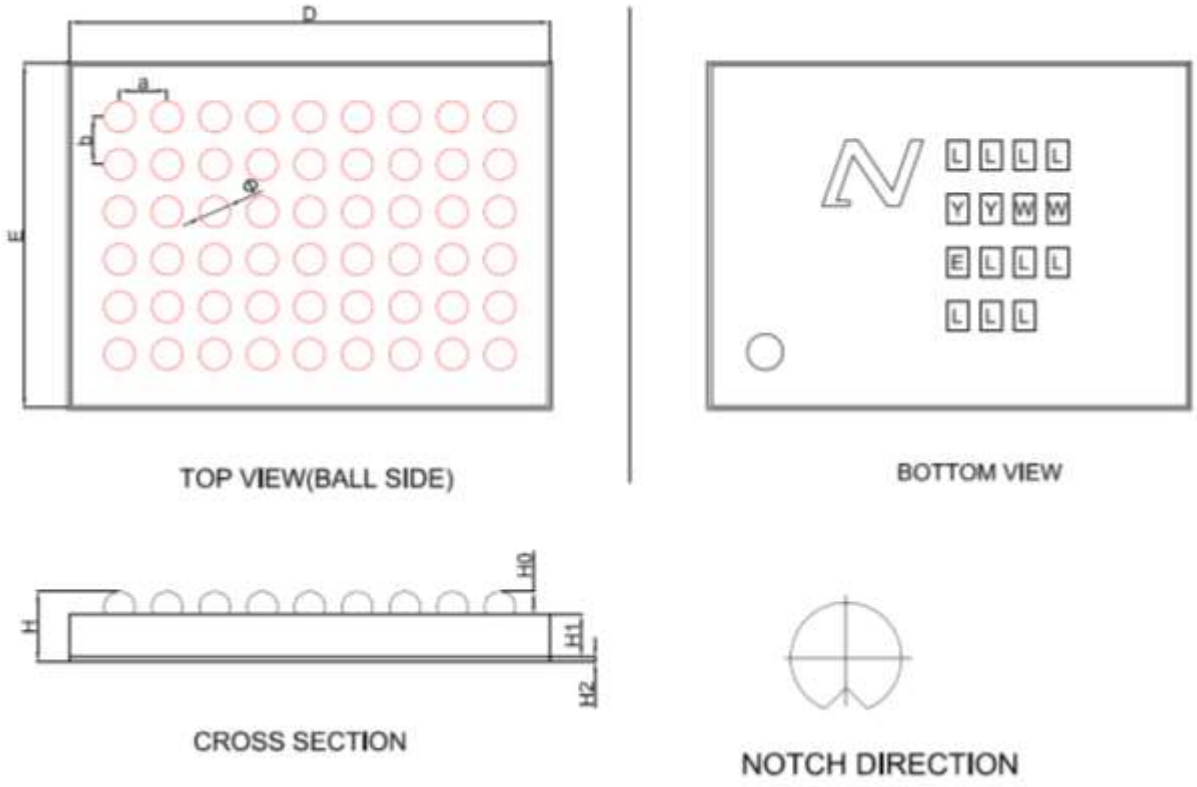
11 Typical Application Circuit



12 Package Information

Orderable Device	Status	Package Type	Package Drawing	Pins	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp©	Device Marking
NU1619WFFB	MP	WCSP	WFF	54	Green(RoHS & No Sb/Br	Cu/Sn Ag Cu	Level-2	-40 to 125	NU1619WFF

13 Mechanical Data



SYMBOL	ITEM	DATA(UM)
D*E	PACKAGE SIZE X*Y	4040*2900±25
Φ	BALL DIAMETER	260±30
a/b	BALL PITCH X/Y	400/400
N	BALL COUNT	54
H	PACKAGE HEIGHT	590±45
H0	BALL HEIGHT	195±30
H1	SI THICKNESS+PI	355±25
H2	DRY FILM	40