

MOSFET - Power, N-Channel, SUPERFET® III, FAST

650 V, 95 mΩ, 30 A

NTPF095N65S3H

Description

SUPERFET III MOSFET is **onsemi**'s brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III FAST MOSFET series helps minimize various power systems and improve system efficiency.

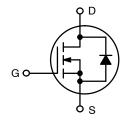
Features

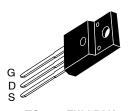
- $700 \text{ V} @ \text{T}_{\text{J}} = 150^{\circ}\text{C}$
- Typ. $R_{DS(on)} = 77 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. Q_g = 58 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 522 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter

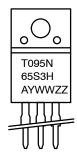
V _{DSS}	R _{DS(ON)} MAX	I _D MAX	
650 V	95 mΩ @ 10 V	30 A	





TO-220 FULLPAK CASE 221D

MARKING DIAGRAM



T095N65S3H = Specific Device Code A = Assembly Location

YWW = Date Code (Year and Week)
ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	DC	±30	V
		AC (f > 1 Hz)	±30	V
I _D	Drain Current	Continuous (T _C = 25°C)	30*	Α
		Continuous (T _C = 100°C)	18*	
I _{DM}	Drain Current	Pulsed (Note 1)	84*	А
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		284	mJ
I _{AS}	Avalanche Current (Note 2)		5.5	А
E _{AR}	Repetitive Avalanche Energy (Note 1)		2.08	mJ
dv/dt	MOSFET dv/dt Peak Diode Recovery dv/dt (Note 3)		120	V/ns
			20	
P_{D}	Power Dissipation	(T _C = 25°C)	40	W
		Derate Above 25°C	0.32	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		−55 to +150	°C
TL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Drain current limited by maximum junction temperature.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{ heta JC}$	Thermal Resistance, Junction to Case, Max.	3.07	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Shipping
NTPF095N65S3H	T095N65S3H	TO-220 FULLPAK (Pb-Free / Halogen Free)	1000 Units / Tube

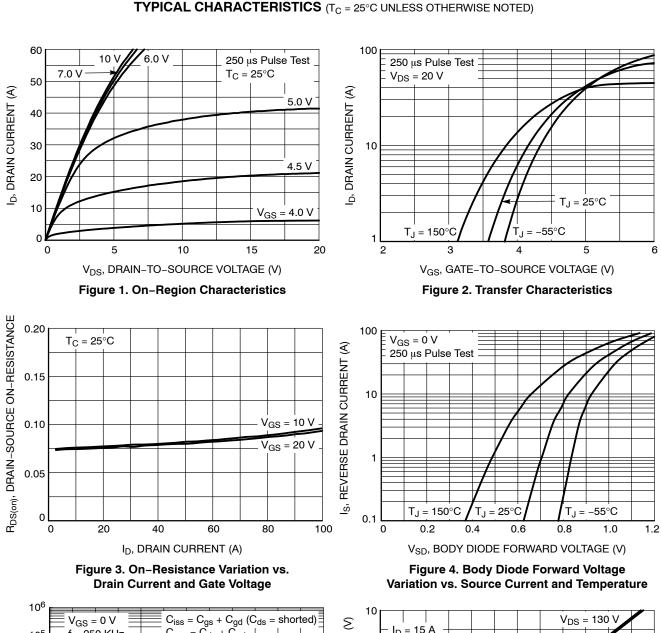
^{1.} Repetitive rating: pulse-width limited by maximum junction temperature. 2. $I_{AS} = 5.5 \text{ A}$, $R_G = 25 \Omega$, starting $T_J = 25^{\circ}\text{C}$. 3. $I_{SD} \le 15 \text{ A}$, $\text{di/dt} \le 200 \text{ A/}\mu\text{s}$, $V_{DD} \le 400 \text{ V}$, starting $T_J = 25^{\circ}\text{C}$.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARACT	ERISTICS		•	•		
BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V, } I_D = 1 \text{ mA, } T_J = 25^{\circ}\text{C}$	650			V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C		0.63		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V			1	μΑ
		V _{DS} = 520 V, T _C = 125°C		1.8		1
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA
ON CHARACTE	RISTICS			•		
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 2.8 \text{ mA}$	2.4		4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 15 A		77	95	mΩ
9FS	Forward Transconductance	V _{DS} = 20 V, I _D = 15 A		30		S
OYNAMIC CHA	RACTERISTICS		I			
C _{iss}	Input Capacitance	$V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}, f = 250 \text{ kHz}$		2833		pF
C _{oss}	Output Capacitance			43		pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		522		pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		75		pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 15 A, V _{GS} = 10 V (Note 4)		58		nC
Q _{gs}	Gate to Source Gate Charge			14		nC
Q _{gd}	Gate to Drain "Miller" Charge	(14616-4)		15		nC
ESR	Equivalent Series Resistance	f = 1 MHz		1.2		Ω
WITCHING CH	IARACTERISTICS		1		•	<u>L</u>
t _{d(on)}	Turn-On Delay Time			24		ns
t _r	Turn-On Rise Time	$V_{DD} = 400 \text{ V}, I_D = 15 \text{ A},$		7.4		ns
t _{d(off)}	Turn-Off Delay Time	$V_{DD} = 400 \text{ V, } I_{D} = 15 \text{ A,} \ V_{GS} = 10 \text{ V, } R_{g} = 4.7 \Omega \ (\text{Note 4})$		69		ns
t _f	Turn-Off Fall Time	, ,		2.4		ns
SOURCE-DRAI	N DIODE CHARACTERISTICS		ı			
I _S	Maximum Continuous Source to Drain Diode Forward Current				30	Α
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current				84	Α
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 15 A			1.2	٧
t _{rr}	Reverse Recovery Time	V _{DD} = 400 V, I _{SD} = 15 A,		367		ns
Q _{rr}	Reverse Recovery Charge	dl _F /dt = 100 A/μs		6.3		μС

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.



V_{GS}, GATE-SOURCE VOLTAGE (V) $C_{oss} = \bar{C_{ds}} +$ 10⁵ f = 250 KHz $C_{rss} = C_{gd}$ CAPACITANCE (pF) 10⁴ C_{iss} 10³ 10² $C_{o\underline{s}\underline{s}}$ Crss 10¹ 10⁰ 10^{-1} 100 200 300 400 500 600 0 V_{DS}, DRAIN-TO-SOURCE VOLTAGE (V)

Figure 5. Capacitance Characteristics

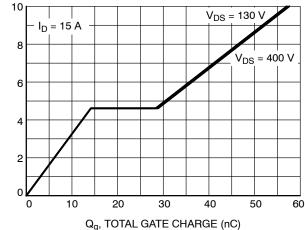


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (T_C = 25°C UNLESS OTHERWISE NOTED)

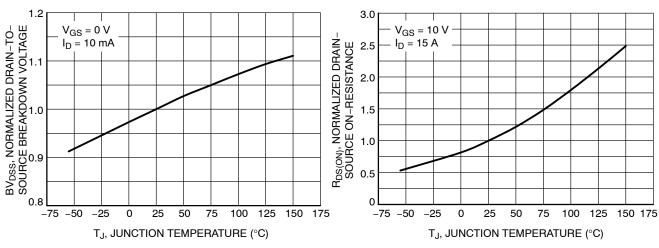


Figure 7. Breakdown Voltage Variation vs. Temperature

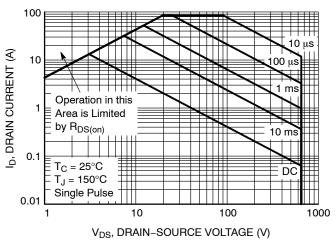


Figure 9. Maximum Safe Operating Area

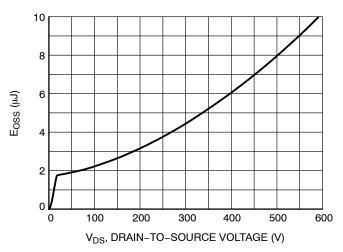


Figure 11. E_{OSS} vs. Drain to Source Voltage



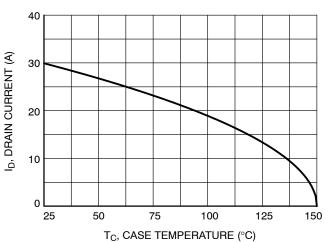


Figure 10. Maximum Drain Current vs. Case Temperature

TYPICAL CHARACTERISTICS (T_C = 25°C UNLESS OTHERWISE NOTED)

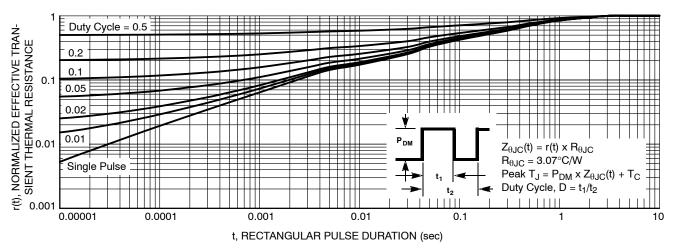


Figure 12. Transient Thermal Impedance

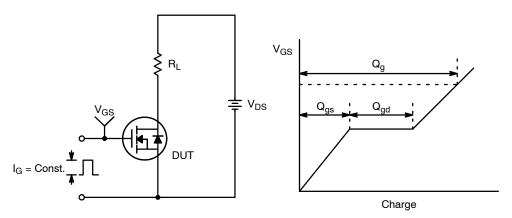


Figure 13. Gate Charge Test Circuit & Waveform

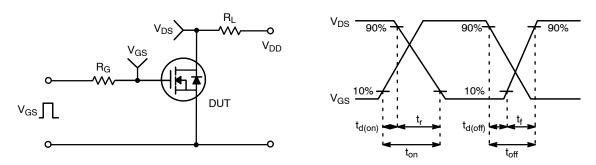


Figure 14. Resistive Switching Test Circuit & Waveforms

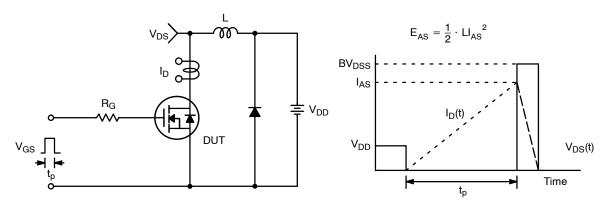


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

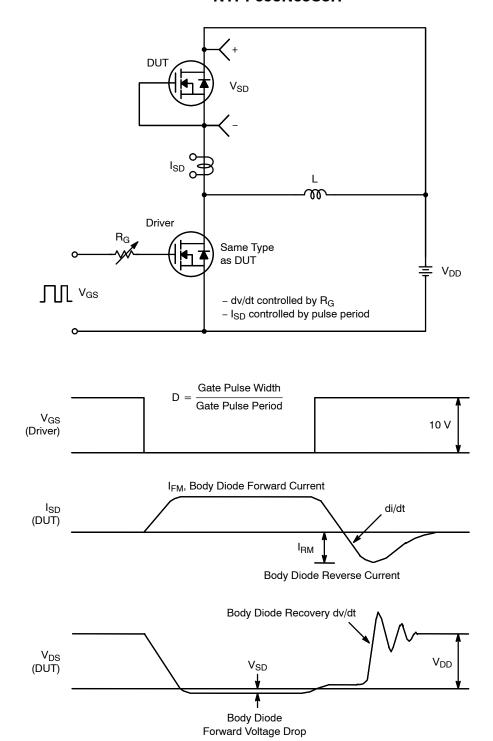


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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MECHANICAL CASE OUTLINE





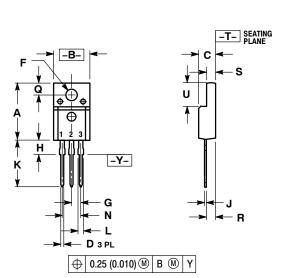
SCALE 1:1

TO-220 FULLPAK CASE 221D-03 ISSUE K

DATE 27 FEB 2009

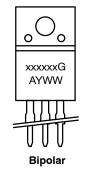
- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH
- 3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

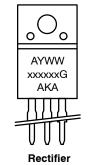
	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.617	0.635	15.67	16.12
В	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
Н	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88



MARKING DIAGRAMS







xxxxxx	= Specific Device Code	Α	= Assembly Location
G	= Pb-Free Package	Υ	= Year
Α	= Assembly Location	WW	= Work Week
Υ	= Year	XXXXXX	= Device Code
WW	= Work Week	G	= Pb-Free Package
		AKA	= Polarity Designator

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DESCRIPTION:	TO-220 FULLPAK		PAGE 1 OF 1	

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