NTMS4800N

Power MOSFET
30 V, 8 A, N−Channel, SOIC−8

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- SOIC−8 Surface Mount Package Saves Board Space
- This is a Pb−Free Device

Applications

- DC−DC Converters
- Printers

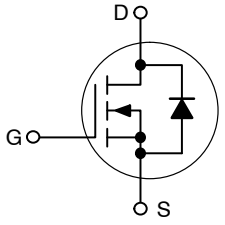
www.DataSheet4U.com

ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
30 V	20 mΩ @ 10 V	8 A
	27 mΩ @ 4.5 V	

N−Channel



MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	6.4	A
		T_A = 70°C		5.1	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	1.29	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		T_A = 25°C	I_D	4.9	A
		T_A = 70°C		3.9	
Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25°C	P_D	0.75	W
Continuous Drain Current $R_{\theta JA}$, t < 10 s (Note 1)		T_A = 25°C	I_D	8.0	A
		T_A = 70°C		6.4	
Power Dissipation $R_{\theta JA}$, t < 10 s (Note 1)		T_A = 25°C	P_D	2.0	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	32	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to +150	°C
Source Current (Body Diode)			I_S	2.0	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, V_{DD} = 30 V, V_{GS} = 10 V, I_L = 11 A_{pk}, L = 1.0 mH, R_G = 25 Ω)			E_{AS}	60.5	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for t = 10 s)			T_L	260	°C

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	97	°C/W
Junction−to−Ambient − t < 10 s (Note 1)	$R_{\theta JA}$	62.5	
Junction−to−Foot (Drain)	$R_{\theta JF}$	25	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	167	

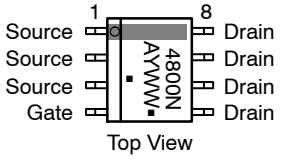
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 in sq pad, 1 oz Cu
2. Surface−mounted on FR4 board using the minimum recommended pad size

1

SO−8
CASE 751
STYLE 12

MARKING DIAGRAM/ PIN ASSIGNMENT



4800N = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMS4800NR2G	SOIC−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2009

www.DataSheet4U.com

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				26		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5		3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 7.5 A			12.5	20	mΩ
		V_{GS} = 4.5 V, I_D = 6.5 A			20	27	
Forward Transconductance	g_{FS}	V_{DS} = 1.5 V, I_D = 7.5 A			21		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 15 V			940		pF
Output Capacitance	C_{oss}				225		
Reverse Transfer Capacitance	C_{rss}				125		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 7.5 A			7.7		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.1		
Gate−to−Source Charge	Q_{GS}				3.3		
Gate−to−Drain Charge	Q_{GD}				3.2		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 7.5 A			15.2		nC
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 1.0 A, R_G = 6.0 Ω			9.4		ns
Rise Time	t_r				4.0		
Turn−Off Delay Time	$t_{d(off)}$				21		
Fall Time	t_f				6.5		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 2.0 A	T_J = 25°C		0.75	1.0	V
			T_J = 125°C		0.59		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 2.0 A			17.8		ns
Charge Time	t_a				8.3		
Discharge Time	t_b				9.5		
Reverse Recovery Charge	Q_{RR}				8.0		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	T_A = 25°C			0.66		nH
Drain Inductance	L_D				0.20		nH
Gate Inductance	L_G				1.5		nH
Gate Resistance	R_G				1.5	3.0	Ω

3. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

www.DataSheet4U.com

www.DataSheet4U.com

TYPICAL PERFORMANCE CURVES

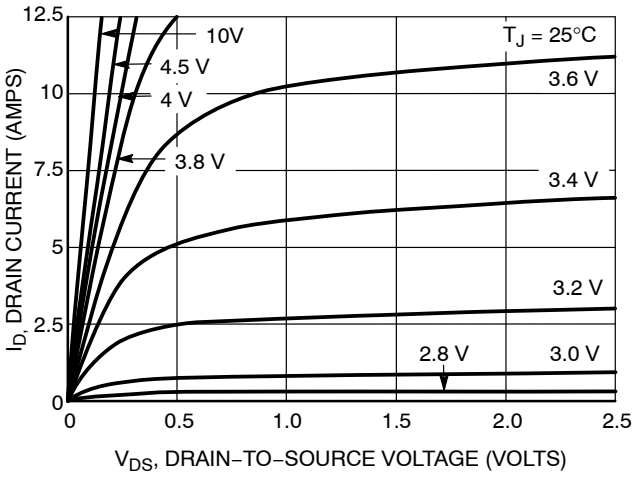


Figure 1. On−Region Characteristics

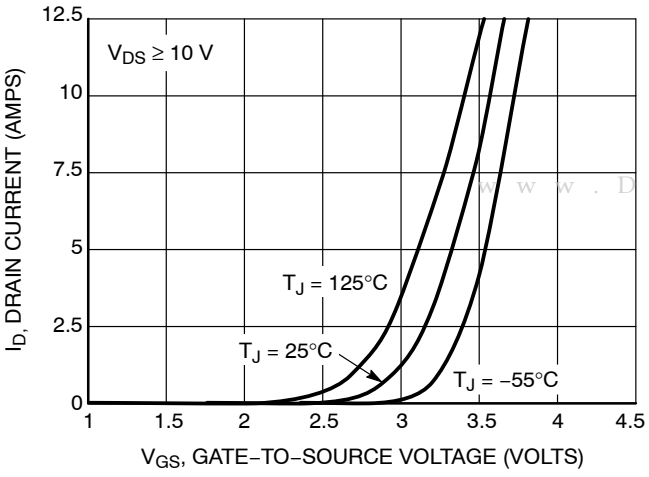


Figure 2. Transfer Characteristics

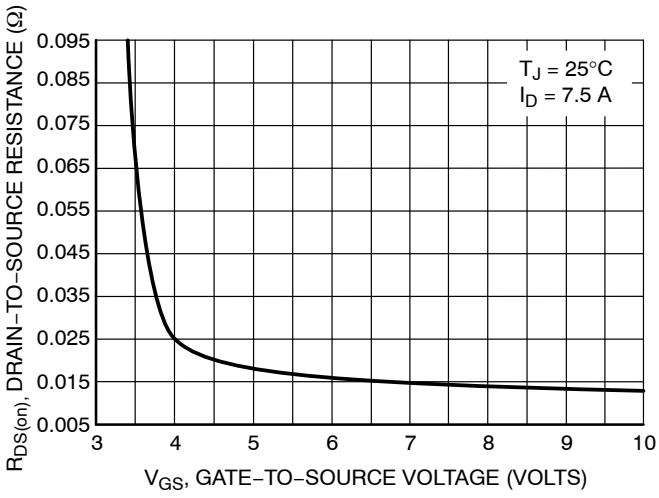


Figure 3. On−Resistance vs. Gate−to−Source Voltage

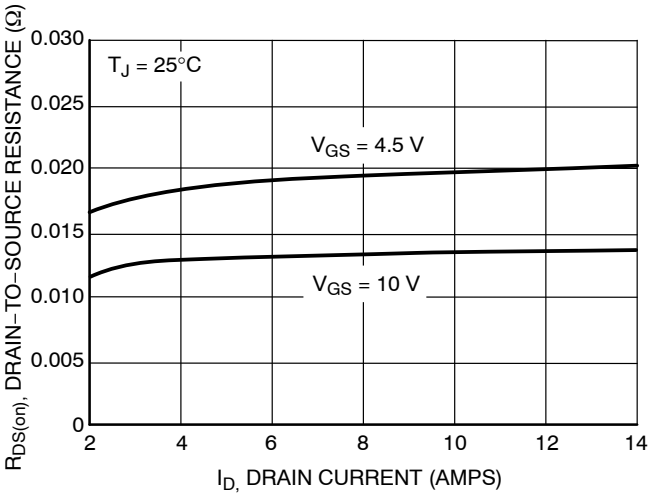


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

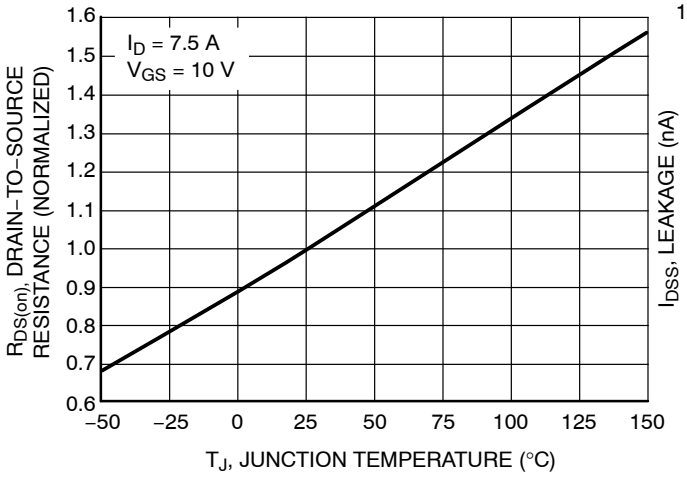


Figure 5. On−Resistance Variation with Temperature

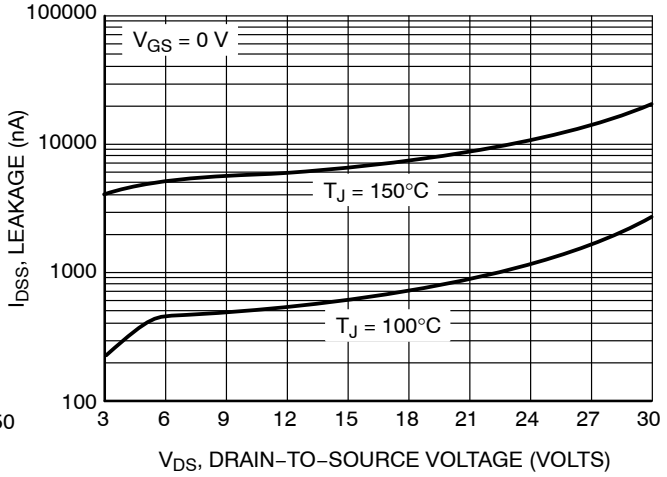


Figure 6. Drain−to−Source Leakage Current vs. Voltage

www.DataSheet4U.com

TYPICAL PERFORMANCE CURVES

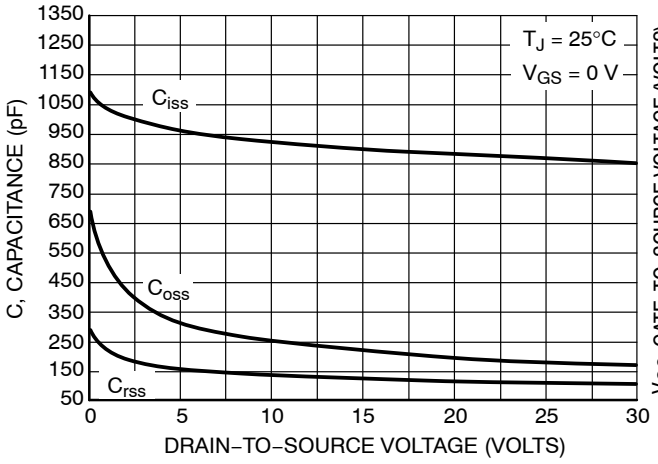
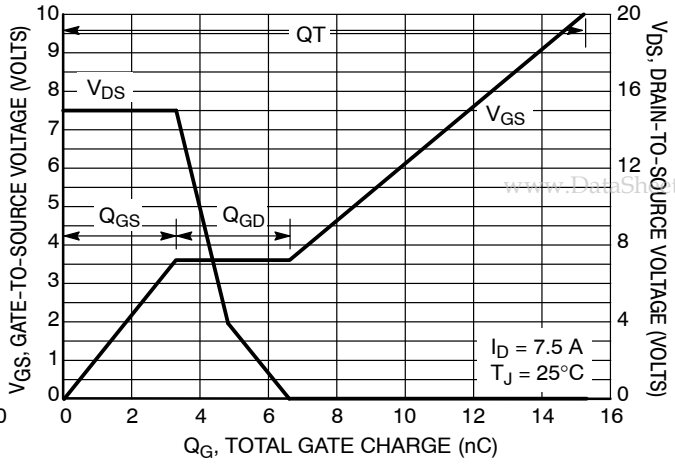


Figure 7. Capacitance Variation



www.DataSheet4U.com

Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge

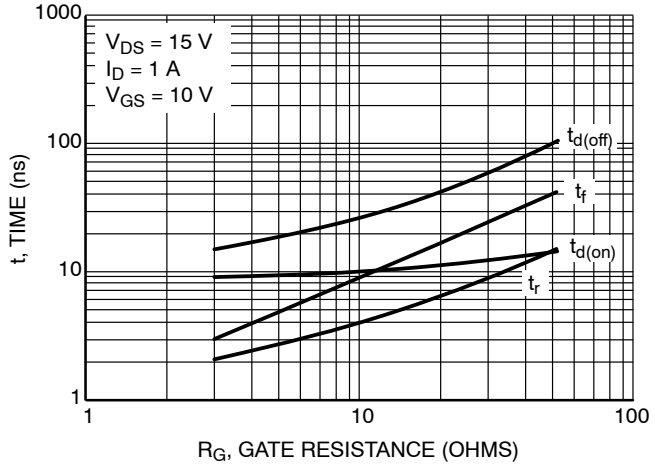


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

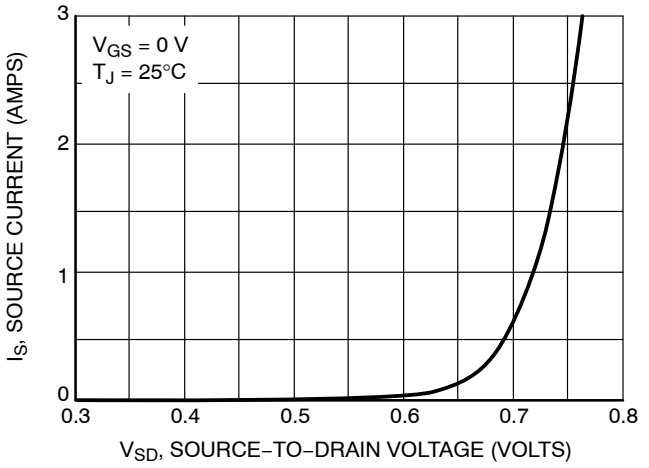


Figure 10. Diode Forward Voltage vs. Current

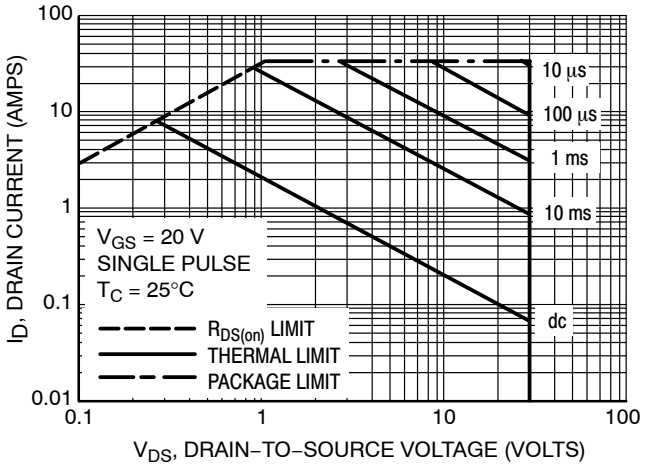


Figure 11. Maximum Rated Forward Biased Safe Operating Area

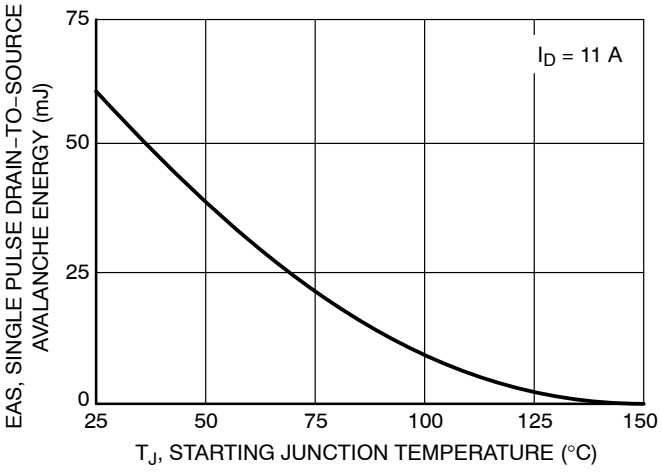
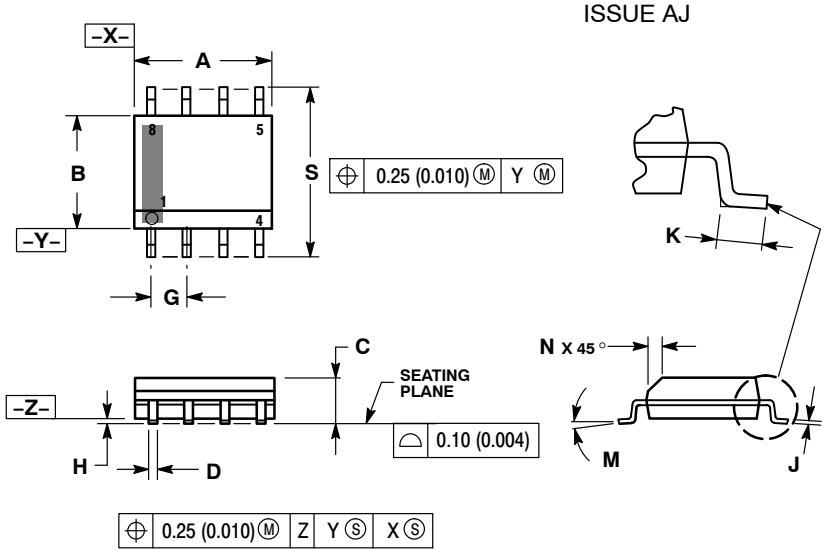


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

www.DataSheet4U.com

PACKAGE DIMENSIONS

SOIC−8
CASE 751−07
ISSUE AJ



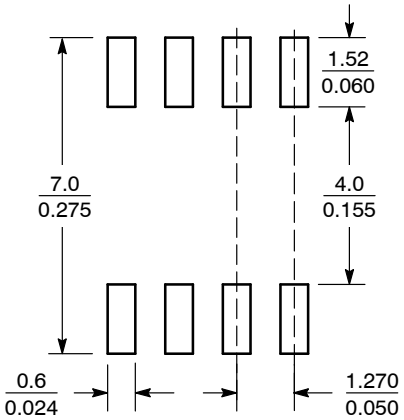
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

www.DataSheet4U.com

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

www.DataSheet4U.com