NTMS4503N

Power MOSFET

28 V, 14 A, N-Channel, SO-8

Features

- Low RDS(on)
- High Power and Current Handling Capability
- Low Gate Charge

Applications

- DC/DC Converters
- Motor Drives
- Synchronous Rectifier POL
- Buck Low-Side

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	28	V
Gate-to-Source Voltage - Continuous	V_{GS}	±20	V
Drain Current Continuous @ $T_a = 25^{\circ}C$ (Note 1) Continuous @ $T_a = 25^{\circ}C$ (Note 2) Continuous @ $T_a = 25^{\circ}C$ (Note 3) Single Pulse (tp = 10 μ s)	I _D	14 12 9.0 40	A
Total Power Dissipation $T_A = 25^{\circ}C \text{ (Note 1)}$ $T_A = 25^{\circ}C \text{ (Note 2)}$ $T_A = 25^{\circ}C \text{ (Note 3)}$	P _D	2.5 1.66 0.93	W
Operating and Storage Temperature	T _J , T _{stg}	-55 to 150	°C
$\begin{array}{l} \mbox{Single Pulse Drain-to-Source Avalanche} \\ \mbox{Energy - Starting T}_{\mbox{J}} = 25^{\circ}\mbox{C} \\ \mbox{(V_{DD} = 30 V, V_{GS} = 10 V, I_{L} = 12.2 A,} \\ \mbox{L} = 1.0 \mbox{ mH, R_{G} = 25 Ω)} \end{array}$	E _{AS}	75	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

THERMAL RESISTANCE RATINGS

Rating	Symbol	Value	Unit
Thermal Resistance Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2) Junction-to-Ambient (Note 3)	$R_{ hetaJA}$	50 75 135	°C/W

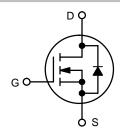
- 1. Surface–mounted on FR4 board using minimum recommended pad size (Cu area 0.412 in^2), t < 10 s.
- Surface-mounted on FR4 board using 1" pad size (Cu area 1.127 in²) steady state.
- Surface-mounted on FR4 board using minimum recommended pad size (Cu area 0.412 in²), steady state.



ON Semiconductor®

http://onsemi.com

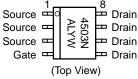
V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX (Note 1)
28 V	7.0 mΩ @ 10 V	14 A
20 V	8.8 mΩ @ 4.5 V	177



MARKING DIAGRAM/ PIN ASSIGNMENT



SO-8 CASE 751 STYLE 12



4503N = Specific Device Code A = Assembly Location

L = Wafer Lot Y = Year W = Work Week

ORDERING INFORMATION

Device	Shipping†	
NTMS4503NR2	SO-8	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTMS4503N

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

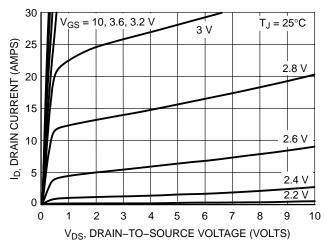
www.DataSheet4U.com

Characteristic	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		28	31	_	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /	-		-	22	-	mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	T _J = 25°C		_	-	1.0	μΑ
		$V_{GS} = 0 \text{ V}, V_{DS} = 24 \text{ V}$	T _J = 100°C	_	-	25	
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 V, V_{GS} =$		-	-	±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D = 2$	250 μΑ	1.0	-	2.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	-		_	-5.0	-	mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D =	: 14 A	_	7.0	8.0	mΩ
		V _{GS} = 4.5 V, I _D =	= 10 A	_	8.8	9.8	
Forward Transconductance	9FS	V _{DS} = 10 V, I _D =	: 14 A	_	30	-	S
CHARGES, CAPACITANCES AND GATE RE	SISTANCE						
Input Capacitance	C _{ISS}			_	2400	-	pF
Output Capacitance	C _{OSS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 16 A		_	1000	-	
Reverse Transfer Capacitance	C _{RSS}			_	375	-	
Total Gate Charge	Q _{G(TOT)}			-	23	-	nC
Threshold Gate Charge	Q _{G(TH)}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 16 \text{ V}, I_{D} = 10 \text{ A}$		_	2.0	-	
Gate-to-Source Charge	Q_{GS}			_	5.0	_	
Gate-to-Drain Charge	Q_{GD}			-	12	-	
SWITCHING CHARACTERISTICS, V _{GS} = V (Note 5)						
Turn-On Delay Time	t _{d(ON)}			-	18.5	_	ns
Rise Time	tr	$V_{GS} = 4.5 \text{ V}, V_{DD} = 16$	V, I _D = 10 A,	-	70	-	
Turn-Off Delay Time	t _{d(OFF)}	$V_{GS} = 4.5 \text{ V}, V_{DD} = 16 \text{ V}, I_{D} = 10 \text{ A},$ $R_{G} = 2.0 \Omega$		-	21	-	
Fall Time	t _f			-	23	_	
DRAIN-SOURCE DIODE CHARACTERISTIC	s						
Forward Diode Voltage	V_{SD}	V 0V 1 40 1	T _J = 25°C	-	0.82	1.2	V
		$V_{GS} = 0 \text{ V}, I_{S} = 10 \text{ A}$ $T_{J} = 125^{\circ}\text{C}$		-	0.65	-	
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, } d_{ISD}/d_t = 100 \text{ A/}\mu\text{s,}$ $I_S = 14 \text{ A}$		_	48	-	ns
Charge Time	T _a			_	23	-	1
Discharge Time	T _b			-	25	-	
Reverse Recovery Charge	Q_{RR}			-	25	-	nC

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

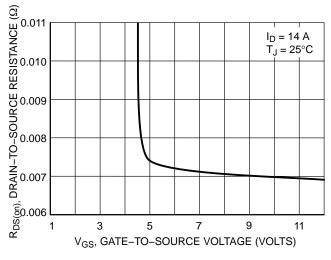
www.DataSheet4U.com



 $V_{DS} \ge 10 \text{ V}$ V_{D

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



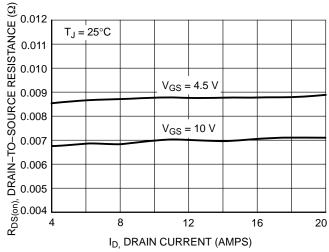
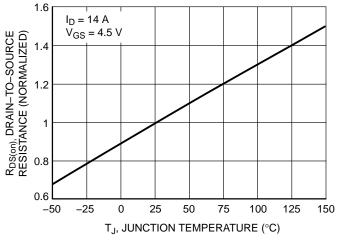


Figure 3. On-Resistance vs. Gate-to-Source Voltage

Figure 4. On–Resistance vs. Drain Current and Gate Voltage



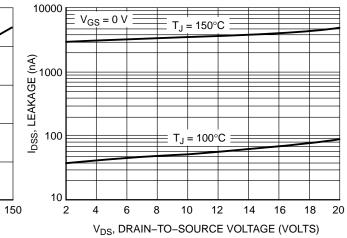
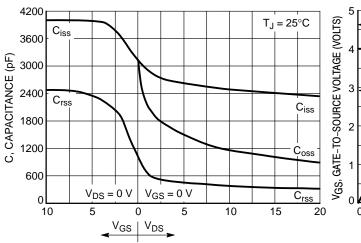


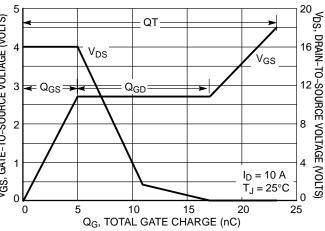
Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

www.DataSheet4U.com





GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge



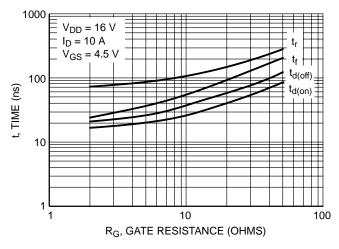


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

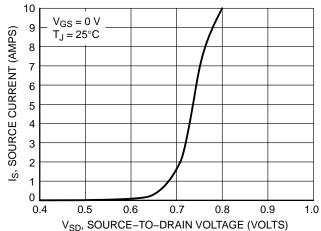
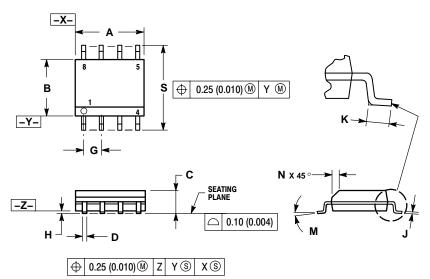


Figure 10. Diode Forward Voltage vs. Current

PACKAGE DIMENSIONS

www.DataSheet4U.com

SO-8 CASE 751-07 **ISSUE AA**



NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.

 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

 5. DIMENSION
- SIDE.

 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

	MILLIMETERS		INCHES			
DIM	MIN	MIN MAX MIN		MAX		
Α	4.80	5.00	0.189	0.197		
В	3.80	4.00	0.150	0.157		
c	1.35	1.75	0.053	0.069		
ם	0.33	0.51	0.013	0.020		
G	1.2	1.27 BSC		0 BSC		
H	0.10	0.25	0.004	0.010		
7	0.19	0.25	0.007	0.010		
K	0.40	1.27	0.016	0.050		
M	0 °	8 °	0 °	8 °		
N	0.25	0.50	0.010	0.020		
S	5.80	6.20	0.228	0 244		

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE

- DRAIN
- DRAIN DRAIN
- DRAIN

NTMS4503N

www.DataSheet4U.com

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com

Japan: ON Semiconductor, Japan Customer Focus Center 2–9–1 Kamimeguro, Meguro–ku, Tokyo, Japan 153–0051 Phone: 81–3–5773–3850

N. American Technical Support: 800-282-9855 Toll Free

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.